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(54) Title: HYBRID MEMORY AND MTJ BASED MRAM BIT-CELL AND ARRAY

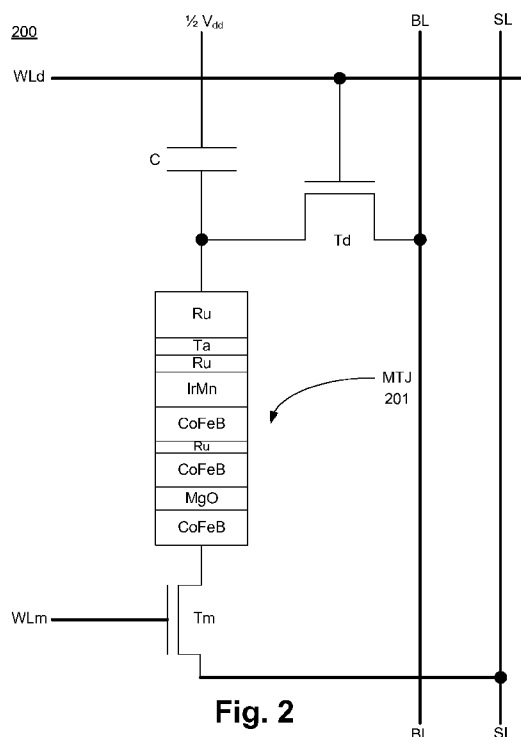


Fig. 2

(57) Abstract: Described is an apparatus for a hybrid eDRAM and MRAM memory cell comprising: a capacitor having a first terminal and a second terminal; a first transistor having a gate terminal coupled to a first word line (WL), a source/drain terminal coupled to bit line (BL), and drain/source terminal coupled to the first terminal of the capacitor; a resistive memory element having a first terminal and a second terminal, the first terminal of the resistive memory element device coupled to the first terminal of the capacitor; and a second transistor having a gate terminal coupled to a second WL, a source/drain terminal coupled to source line (SL), and drain/source terminal coupled to the second terminal of the resistive memory element device.



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