A FULLY DIGITAL PULSE WIDTH MODULATION MODULE

CROSS REFERENCE TO RELATED APPLICATION

[0001] This application claims the benefit of priority to Singapore patent application no. 10202400410P which was filed on 15 February 2024, the contents of which are hereby incorporated by reference in its entirety for all purposes.

TECHNICAL FIELD

[0002] This application relates to a fully digital pulse width modulation module for generating precise sub-nanosecond pulses in a linear manner and within a wide dynamic range.

BACKGROUND

[0003] Pulse width modulation (PWM) generators are widely used in various applications. A common type of PWM that is widely used are analog PWM generators. However, analog PWM generators typically require additional controls for biasing voltages or currents and often exhibit non-linear behavior and low resolution. This in turn affects the performance, integration, and design complexity of the PWM generator. Another type of PWM that is also commonly used are digital PWM generators which are able to integrate seamlessly with advanced technologies but such implementations typically rely on high-speed reference clocks, which limit their practical applicability.

[0004] The selection of PWM generator designs depends on the application's requirements and the system's complexity. One of the simplest approaches involves using a 555 timer integrated circuit (IC) configured in a stable mode, where the duty cycle of the output signal can be controlled by adjusting the resistor and capacitor values in the circuit. Another common method is to utilize microcontrollers, which often include built-in PWM modules that allow users to generate PWM signals on specific output pins with precise control over the duty cycle.

[0005] For more complex systems, such as those involving digital signal processing or high-speed control applications, PWM generators can be implemented using field-programmable gate arrays (FPGAs). FPGAs offer high customization and flexibility, enabling PWM generation through computing languages like VHDL or Verilog. In advanced applications, application-specific integrated circuit (ASIC)-based PWM generators provide additional

benefits, such as improved energy efficiency, reduced size and cost, enhanced reliability, and better overall performance.

[0006] PWM generators are widely used in industries that require precise pulse generation, particularly in quantum instrumentation, where accuracy is critical for controlling and manipulating quantum systems.

[0007] In quantum systems that require the detection of photons, the timing of quench and reset signals have to be precisely controlled and this is done to ensure efficient operation of photodetectors, such as single-photon avalanche diodes (SPADs), within such quantum systems. The quench signal is used to stop the avalanche multiplication process triggered by a photon detection event, while the reset signal reinitializes the detector's active region, clearing residual charge carriers or after-pulsing effects. For optimal performance, the quench signal must act immediately after a photon event to minimize dead time, and the reset signal must follow shortly after to prepare the detector for subsequent events. The pulse duration of these signals must be short and well-defined to prevent additional noise or unwanted effects, ensuring the detector operates with high efficiency and precision in demanding environments.

[0008] As a result, those skilled in the art are constantly looking for a fully digital control circuit capable of generating sub-nanosecond pulses with linear characteristics and a wide dynamic range, while being independent of high-speed reference clocks.

SUMMARY

[0009] In one aspect, the present application discloses a digital pulse width modulation (PWM) module. The PWM module comprises a PWM signal generator module configured to generate an output pulse signal having a predetermined width in response to receiving an input pulse signal. The PWM signal generator module comprises an edge detector module configured to generate a rising edge of the output pulse signal in response to detecting an edge of the input pulse signal, a coarse delay module configured to receive the rising edge signal, generate a periodic clock signal by propagating a signal through a feedback loop of delay elements, and provide a trigger to the edge detector module after a predetermined number of clock signals have been propagated through the feedback loop, whereby the edge detector module generates a falling edge of the output pulse signal upon receiving the trigger. The digital PWM module

also comprises a digital calibrator module coupled to the PWM signal generator module where the digital calibrator module is configured to adjust a frequency of the periodic clock signal generated by the coarse delay module based on a target frequency of the periodic clock signal, a reference clock frequency and a predetermined threshold of clock cycles.

[0010] In another embodiment of the one aspect, the digital PWM module further comprises a fine delay module positioned between the coarse delay module and the edge detector module. In embodiments of the disclosure, the fine delay module is configured to receive the trigger after the predetermined number of clock signals have been propagated through the feedback loop of the coarse delay module, the fine delay module comprising a plurality of fine-delay elements, each fine-delay element comprising: a fine-delay cell configured to introduce a fine delay to the received trigger, and a switch arranged in series with the fine-delay cell such that the fine-delay cell is selected when the switch is turned on, provide the fine-delayed trigger to the edge detector module, wherein the fine delay introduced by each of the fine-delay elements is shorter than a time period of the clock signal generated by the coarse delay module.

[0011] In another embodiment of the one aspect, the coarse delay module comprises a ring oscillator configured to generate the periodic clock signal by propagating the signal through a loop of delay elements, a counter communicatively coupled to the ring oscillator, the counter configured to count a number of loops of clock signals that propagated through the loop of delay elements, a comparator communicatively coupled to the counter, the comparator configured to compare a count of the counter with a predetermined delay value, and a digital register communicatively coupled to the comparator, the digital register configured to generate the trigger in response to the comparator matching the count of the counter with the predetermined delay value.

[0012] In another aspect, the present application discloses a method for forming a digital pulse width modulation (PWM) module. The disclosed method comprises the steps of forming a PWM signal generator module to generate an output pulse signal having a predetermined width in response to receiving an input pulse signal, whereby the forming of the PWM signal generator module comprises the steps of: forming an edge detector module to generate a rising edge of the output pulse signal in response to detecting an edge of the input pulse signal, forming a coarse delay module to receive the rising edge signal, generate a periodic clock signal

by propagating a signal through a feedback loop of delay elements, and provide a trigger to the edge detector module after a predetermined number of clock signals have been propagated through the feedback loop, whereby the edge detector module generates a falling edge of the output pulse signal upon receiving the trigger. The method also comprises the step of forming a digital calibrator module such that the digital calibrator module is coupled to the PWM signal generator module, whereby the digital calibrator module is formed to adjust a frequency of the periodic clock signal generated by the coarse delay module based on a target frequency of the periodic clock signal, a reference clock frequency and a predetermined threshold of clock cycles.

[0013] In another embodiment of this another aspect, the disclosed method further comprises the steps of forming a fine delay module, between the coarse delay module and the edge detector module, to receive the trigger after the predetermined number of clock signals have been propagated through the feedback loop of the coarse delay module, whereby the forming of the fine delay module comprises the steps of: forming a plurality of fine-delay elements, each fine-delay element comprising: a fine-delay cell configured to introduce a fine delay to the received trigger, and a switch arranged in series with the fine-delay cell such that the fine-delay cell is selected when the switch is turned on, provide the fine-delayed trigger to the edge detector module, wherein the fine delay introduced by each of the fine-delay elements is shorter than a time period of the clock signal generated by the coarse delay module.

[0014] In yet another embodiment of this another aspect, the disclosed method further comprises the steps of forming of the coarse delay module by forming a ring oscillator to generate the periodic clock signal by propagating the signal through a loop of delay elements, forming a counter communicatively coupled to the ring oscillator, the counter configured to count a number of loops of clock signals that propagated through the loop of delay elements, forming a comparator communicatively coupled to the counter, the comparator configured to compare a count of the counter with a predetermined delay value, and forming a digital register communicatively coupled to the comparator, the digital register configured to generate the trigger in response to the comparator matching the count of the counter with the predetermined delay value.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] Various embodiments of the present disclosure are described below with reference to the following drawings:

Figure 1 illustrates a block diagram of a single-photon avalanche diode (SPAD) detection system in accordance with embodiments of the present disclosure;

Figure 2a illustrates a circuit diagram of a programmable delay circuit as known to one skilled in the art;

Figure 2b illustrates a simplified RC model and expected delays between the input and output signals of the programmable delay shown in Figure 2a;

Figure 3 illustrates a simulated plot showing the simulated delay of a PMOS transistor as used in the programmable delay circuit when the PMOS transistor's biasing voltages are varied;

Figure 4a illustrates a circuit diagram for manipulating raw PWM signals using a shift register, multiplexer, and AND and OR logic gates as known to one skilled in the art;

Figure 4b illustrates the timing diagram that is used to drive the components illustrated in Figure 4a;

Figure 5 illustrates a block diagram showing the modules provided within the digital pulse width modulation (PWM) module in accordance with embodiments of the disclosure;

Figure 6 illustrates a block diagram showing the components provided within the PWM generator module in accordance with embodiments of the disclosure;

Figure 7 illustrates a block diagram showing the components provided within the coarse delay module in accordance with embodiments of the disclosure;

Figure 8 illustrates a block diagram showing the components provided within the fine delay module in accordance with embodiments of the disclosure;

Figure 9 illustrates an exemplary timing diagram that of the signals as they propagate through the PWM module in accordance with embodiments of the disclosure;

Figure 10 illustrated a flowchart that sets out the process or method for calibrating the PWM generator module using the digital calibrator module in accordance with embodiments of the disclosure;

Figure 11 illustrates simulated plots showing the variation in a width of the output pulse width when the loop calibration is varied under three different scenarios, typical-typical (TT) corner, under 27 ℃ and with a 1.2V supply voltage, slow-slow (SS) corner, under 40 ℃ and with a 1.08V, and fast-fast (FF) corner, under -40℃ and with 1.32V;

Figure 12 illustrates the programmed pulse width from the PWM signal generator module under an extreme scenario when loop and load calibration is performed, and when no calibration is performed; and

Figure 13 illustrates a process for forming the digital PWM module in accordance with embodiments of the disclosure.

DETAILED DESCRIPTION

[0016] The following detailed description is made with reference to the accompanying drawings, showing details and embodiments of the present disclosure for the purposes of illustration. Features that are described in the context of an embodiment may correspondingly be applicable to the same or similar features in the other embodiments, even if not explicitly described in these other embodiments. Additions and/or combinations and/or alternatives as described for a feature in the context of an embodiment may correspondingly be applicable to the same or similar feature in the other embodiments.

[0017] In the context of various embodiments, the articles "a", "an" and "the" as used with regard to a feature or element include a reference to one or more of the features or elements.

[0018] In the context of various embodiments, the term "about" or "approximately" as applied to a numeric value encompasses the exact value and a reasonable variance as generally understood in the relevant technical field, e.g., within 10% of the specified value.

[0019] As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items.

[0020] As used herein, "comprising" means including, but not limited to, whatever follows the word "comprising". Thus, use of the term "comprising" indicates that the listed elements are required or mandatory, but that other elements are optional and may or may not be present.

[0021] As used herein, "consisting of" means including, and limited to, whatever follows the phrase "consisting of". Thus, use of the phrase "consisting of" indicates that the listed elements are required or mandatory, and that no other elements may be present.

[0022] It should be noted that although the terms first, second and third are used herein to describe various elements, these elements should not be limited by these terms as these terms are meant to only distinguish one element from another element. Thus, the first element described herein could be termed as a second element without departing from this disclosure.

[0023] As used herein, a "periodic clock signal" is defined as a signal that oscillates between high and low states, wherein the period of the clock signal is determined by a configuration of a feedback loop of delay elements, specifically the number of delay elements in the feedback loop and the associated loads.

[0024] Further, one skilled in the art will recognize that certain functional units in this description have been labelled as modules, sub-modules or sets of processing elements throughout the specification. The person skilled in the art will also recognize that a module, a sub-module or a set of processing elements may be implemented as circuits, logic chips or any sort of discrete component. Still further, one skilled in the art will also recognize that a module, a sub-module or a set of processing elements may be implemented in software which may then be executed by a variety of processor architectures. In embodiments of the disclosure, a module, a sub-module or a set of processing elements may also comprise computer instructions, computations or executable code that may instruct a computer processor to carry out a sequence of events based on instructions received. The choice of the implementation of the modules, the sub-modules or the sets of processing elements is left as a design choice for a person skilled in the art and does not limit the scope of the claimed subject matter in any way.

[0025] Pulse width modulation (PWM) signal generators are widely used in various fields such as laser systems, radar and communication, time-domain measurement systems, medical devices, imaging and sensing systems, quantum instruments, etc. For example, quantum instruments require the generation of control signals with a wide pulse-width range (from nanoseconds to microseconds) and precise step resolutions to characterize various types of photon detectors effectively. An exemplary block diagram of a single-photon avalanche diode (SPAD) quench/reset system that is commonly used in the art is illustrated in Figure 1, where SPADs serve as photodetectors, converting incoming photons into electrical signals for further processing.

[0026] Specifically, Figure 1 illustrates system 100 for single-photon detection using SPAD 104 that is coupled with PWM application specific integrated circuit (ASIC) 119. PWM ASIC 119 is configured to generate and control quench 106 and reset 108 signals to ensure photon detection and recovery.

[0027] At an input stage, SPAD 104 functions as the photodetector and it converts incoming photons 102 into electrical signals by entering an avalanche state upon photon detection. To stop the avalanche process, quench signal 106 has to be applied to SPAD 104 via switch 110, while reset signal 108 resets the SPAD 104 via switch 112 for subsequent photon events. The timings of quench signal 106 and reset signal 108 have to be precisely managed to ensure proper detection of photons at SPAD 104.

[0028] When SPAD 104 detects a photon, it causes input signal 114 to be provided to comparator 115. If input signal 114 exceeds a predetermined threshold 115, comparator 115 then provides input pulse signal 118 to PWM ASIC 119, triggering the generation of the quench and reset signals. PWM ASIC 119 is configured to produce pulses with a wide range of widths, supporting applications where flexible and accurate timing is essential.

[0029] A commonly used programmable delay circuit that operates by adjusting analog biasing voltages is illustrated in Figure 2a. In this configuration, the input initially remains at ground voltage, allowing NMOS transistor N1 to discharge capacitor C_P to ground. When a positive step voltage is applied at the input, capacitor C_P charges based on the source-drain resistance of PMOS transistor P1. The gate terminal of PMOS transistor P1 is accessible to the user, enabling programmable resistance adjustments. This adjustment allows the resistance to be set very small for short delays or very large for extended delays. A simplified RC model and the expected input-output delays for this programmable delay circuit are illustrated in Figure 2b.

[0030] However, this approach faces challenges due to the non-linear behavior of the source-drain resistance of PMOS transistor as a function of the biasing voltage. This non-linearity limits the practicality of the system, especially in precision-demanding applications such as quantum systems. Simulation results, performed using the GlobalFoundries 55nm process at room temperature with typical transistors, are illustrated in Figure 3. While the plot

in Figure 3 shows that the circuit is able to achieve a broad pulse width range of up to 1 ms, the delay exhibits a dramatic increase as the biasing voltage is adjusted, further highlighting the limitations of this approach in achieving linear and predictable delay behavior.

[0031] In another approach, those skilled in the art have proposed a digital PWM generator circuit that manipulates raw PWM signals using a combination of a shift register, multiplexer, AND logic gate, and OR logic gate as illustrated in Figure 4a. In this system, the raw PWM signal is fed into the shift register, and the multiplexer is programmed to select a specific delay time for the PWM signal. The delay time, however, is constrained to be a multiple of the reference clock period, ignoring the delays introduced by the logic circuits themselves. Once delayed, the raw and delayed PWM signals are processed through logic circuits to generate the final output signal. The timing diagram, as illustrated in Figure 4b, demonstrates that the raw and delayed PWM signals can be combined via an AND gate to produce a shortened PWM signal or via an OR gate to produce a stretched pulse width.

[0032] While this approach provides basic delay control, its resolution and delay quality are heavily dependent on the frequency of the reference clock (e.g., 240 MHz), which is limited by current technology. Additionally, the pulse width range scales linearly with the number of multiplexers and shift registers, leading to substantial hardware overheads when generating a broad range of PWM signals. A further limitation arises from the use of an external clock, which forces the rising and falling edges of the generated pulses to be synchronized with the clock signal. This restriction makes the system unsuitable for applications such as single-photon detection, where the rising and falling edges of the pulses must be asynchronous and triggered by real-time events like photon arrivals.

[0033] A digital PWM module that solves the problems of the systems described above is illustrated in Figure 5. Specifically, digital PWM module 500 is designed in accordance with embodiments of the disclosure, and it comprises PWM signal generator module 502 that is configured to generate an output pulse signal when it is triggered by an input pulse, e.g., an input pulse from a SPAD detector, and also comprises digital calibrator module that incorporates a self-calibration mechanism to compensate process, voltage, and temperature (PVT) variations associated with components provided within PWM signal generator module 502.

[0034] PWM signal generator module 502 comprises two main components: coarse delay module 503 and fine delay module 504. Coarse delay module 503 is configured to introduce a programmable delay to a signal propagating within the PWM signal generator module 502 while fine delay module 504 is configured to refine the delay applied to the propagating signal with smaller, high-resolution adjustments to ensure precise control of output signal 514's pulse width. Together, the coarse and fine delay modules generate the final output signal 514 with the desired pulse characteristics.

[0035] Digital calibrator module 506 comprises control logic 507 and counter 508. Control logic 507 configures the timing parameters for both the coarse and fine delay modules, while the counter 508 measures and adjusts the delay introduced by the system. Digital calibrator module 506 dynamically compensates for PVT variations to ensure that PWM signal generator module 502 is able to precisely generate output signal 514 with the desired characteristics. Lastly, reference clock signal 512 is provided to digital PWM module 500 to ensure that the components contained therein operate in a synchronized manner.

[0036] Figure 6 illustrates PWM signal generator module 502 that is designed in accordance with embodiments of the disclosure to produce programmable pulse widths with high precision and flexibility. When input pulse or signal 510 is received by edge detector circuit 602, edge detector circuit 602 will generate step signal 603, i.e., a rising edge of output pulse signal 514, and step signal 603 will trigger a delay generation process performed by coarse delay module 503.

[0037] Coarse delay module 503 comprises of three key components: ring oscillator 604, counter 606, and comparator 608. These key components work together to introduce a programmable delay to a signal propagating within ring oscillator 604 when ring oscillator 604 is triggered. In operation, ring oscillator 604 generates a periodic clock signal by propagating a signal through a feedback loop of delay elements. The frequency of the clock signal is adjustable through the configuration of delay elements within the feedback loop and the period of the clock signal is defined as the amount of time it takes a signal to propagate through the feedback loop of ring oscillator 604. Input port 605 may be used to receive signals provided by digital calibrator module 506 to adjust the frequency of the clock signal.

[0038] This clock signal produced by ring oscillator 604 in turn drives counter 606, which counts the oscillation cycles. Comparator 608 then matches the counter 606's output to user-defined inputs to generate a delayed trigger signal. In embodiments of the disclosure, the user-defined inputs may be provided to comparator 608 through input port 609. Through this approach, coarse delay module 503 enables a wide dynamic range of delays to be selected by creating a linear delay proportional to the oscillator's period and the user-defined inputs.

[0039] Once counter 606's output matches with comparator 608's input, a delay trigger signal may be provided to fine delay module 504, which may further refine the delay with picosecond-level precision, based on additional user inputs. Fine delay module 504 may also be configured to provide the delayed trigger signal directly to edge coupler 610 if it determines that no additional delays are required to be introduced to the trigger signal. In embodiments of the disclosure, the delayed trigger signal may be directly provided to edge coupler 610, effectively bypassing fine delay module 504. In embodiments of the disclosure, fine delay module 504 may be designed such that a delay introduced by this module is equal or less than a period of a clock signal generated by ring oscillator 604.

[0040] When edge coupler 610 receives the delayed trigger signal, edge coupler 610 will generate a down-step signal, i.e., a falling edge of output pulse signal 514, thereby completing the process of generating output pulse 514. A notable feature of PWM signal generator module 502 is that the internally generated clock signal from ring oscillator 604 is reconfigurable, asynchronous, and highly precise. This asynchronous behavior is crucial for applications where the triggering events may be random, such as the detection of single photons.

[0041] Figure 7 illustrates a block diagram showing the components provided within coarse delay module 503 in accordance with embodiments of the disclosure. Specifically, coarse delay module 503 comprises Nand-logic gate 702, ring oscillator 604, counter 606, comparator 608, and register 712. Ring oscillator 604 includes a feedback loop that is made up of delay elements 708a, 708b, ..., 708n and programmable switches 706a, 706b, ..., 706n (up to n number of elements and switches), allowing the delay characteristics of the feedback loop to be adjusted. Each delay element further comprises a loading element 704a, 704b, ..., 704n (up to n number of elements) that can be selectively added or removed using switches 706. In operation, ring

oscillator 604 is triggered by trigger signal 603, via Nand-logic gate 702, to generate periodic clock signal 709 that is provided to counter 606, which counts the number of clock cycles generated by the ring oscillator. It should be noted that the frequency of the oscillator, i.e., the frequency or period of the clock signal can be adjusted by configuring the number of active delay elements and loads in the feedback loop.

[0042] As counter 606 receives clock signal 709, the counter's output Q_0–Q_{11} is sequentially increased and compared with user-defined inputs 710 B_0–B_{11} in comparator 608. When the counter's value matches the user-defined delay value 710, comparator 608 outputs a logic-high signal. This signal is provided to register 712, which generates delayed trigger signal 714.

[0043] In embodiments of the disclosure, each of delay elements 708n may comprise, but are not limited to, an inverter chain configured to introduce propagation delays or RC delay cells, each of programmable switches 706n may comprise transmission gates, MOSFET switches or MEMS switches, and loading elements 704n may each comprise capacitive loads or a bank of capacitive loads that are coupled to a bank of switches controllable by digital calibrator module. Furthermore, register 712 may comprise D flip-flops that is configured to utilize reference clock signal 512 to synchronize the generation of delayed trigger signal 714 with other modules in the digital PWM module 500.

[0044] Figure 8 illustrates a plurality of fine-delay elements that are provided within fine delay module 504. Specifically, fine delay module 504 is configured to refine the timing of the delayed trigger signal with high precision. In operation, fine delay module 504 receives delayed trigger signal 714 and propagates it through a series of fine-delay elements where each fine-delay element comprises a fine-delay cell (802a, 802b, 802c, ..., 802n) configured to introduce a fine delay to delayed trigger signal 714, and a programmable switch (804a, 804b, 804c, ..., 804n) arranged in series with the fine-delay cell to allow selective bypassing of specific fine-delay cells to dynamically adjust the total delay provided by fine delay module 504. This selective control enables fine-tuning of the delay that is to be introduced to delayed trigger signal 714 to sub-nanosecond precision. The fine-delayed trigger signal may then be provided to edge coupler 610 through output port 814 in accordance with embodiments of the disclosure. In other embodiments of the disclosure, if it is determined that delayed trigger signal 714 is to propagate through fine delay module 504 without any additional delays being introduced,

module 504 may utilize programmable switch 801 to direct delayed trigger signal 714 to output port 814.

[0045] Figure 9 illustrates a timing diagram showing how an input signal 510 is processed within PWM signal generator module 502 to generate a pulse 514 with a specific width. Input signal 510 triggers the PWM signal generator module 502 by causing the generation of a rising edge of output signal 514 and the generation of a trigger signal (not shown) that propagates through coarse and fine delay modules 503 and 504 respectively. It can be seen that upon receiving the trigger signal, ring oscillator 604 generates periodic clock signals 709 with a selectable oscillation period, such as 16 ns. Comparator 608 continuously compares the count of the oscillator's cycles with a user-defined value to determine when the desired delay has been reached. Once a match occurs, comparator 608 signals the register to produce the delayed trigger signal 902.

[0046] Delayed trigger signal 902 is then provided to fine delay module 504 which proceeds to refine the timing of the delay further by adding fine-grained delays to achieve sub-nanosecond accuracy. In this example, fine delay module 504 was configured to adjust the total delay by +0.25 ns, before the fine-delayed trigger signal 904 is provided to edge coupler 610. Upon receiving the fine-delayed trigger signal 904, edge coupler 610 then generates a falling edge of output signal 514 resulting in the generation of the required programmed pulse width, which in this example corresponds to a pulse width of 16.25 ns.

[0047] As mentioned in the previous sections, digital calibrator module 506 is configured to dynamically compensate for PVT variations to ensure that PWM signal generator module 502 is able to precisely generate output signal 514 with the desired characteristics. A process for calibrating PWM signal generator module 502 is disclosed in Figure 10 in accordance with embodiments of the disclosure.

[0048] Process 1000 begins at step 1002, where parameters such as the target frequency of the periodic clock signal (e.g., 1 GHz), a reference clock frequency (e.g., 20 MHz clock), a predefined threshold of clock cycles, and the initial values for the loop count (e.g., number of delay cells in the feedback loop) and load count (e.g., number of loads) are defined. Once this

initial setup process has been completed, process 1000 proceeds to activate the ring oscillator to begin the initial generation of clock signals. This takes place at step 1004.

[0049] At step 1006, process 1000 measures the number of clock cycles generated by the oscillator during the specified interval (e.g., 50ms as obtained from the reference clock frequency) and compares this count to the predetermined threshold of clock cycles (e.g., 50,000 cycles which is calculated as the ratio of the specified interval of 50ms to the oscillator's target period 1ns). At step 1008, if process 1000 determines that the count does not exceed the threshold, the number of loops in the oscillator is incremented at step 1010, and process 1000 returns to step 1006 and repeats steps 1006 and 1008 until the threshold is exceeded. When this happens, process 1000 proceeds to step 1012 and decrements the loop count by one. Once this is done, process 1000 transitions to the fine calibration phase. In embodiments of the disclosure, the number of loops in the oscillator may be adjusted by switching on or off the programmable switches within the delay elements of the ring oscillator's feedback loop.

[0050] At step 1014, process 1000 measures the number of clock cycles generated by the oscillator during the specified interval (e.g., 50ms as obtained from the reference clock frequency) and compares this count to the predetermined threshold of clock cycles (e.g., 50,000 cycles which is calculated as the ratio of the specified interval to the oscillator's target period 1ns). At step 1016, if process 1000 determines that the count does not exceed the threshold, the number of loads in the oscillator is incremented at step 1018, and process 1000 returns to step 1014 and repeats steps 1014 and 1016 until the threshold is exceeded. When this happens, process 1000 proceeds to step 1020 and decrements the load count by one. In embodiments of the disclosure, the load count may be adjusted by increasing or decreasing the load capacitance in the delay elements of the ring oscillator's feedback loop.

[0051] Process 1000 then ends as process 1000 would have concluded that the frequency adjustments have fulfilled the required threshold, ensuring the oscillator operates reliably under varying conditions.

[0052] Simulation

[0053] The effectiveness of the digital PWM module designed in accordance with embodiments of the disclosure was validated through post-layout simulations based on GlobalFoundries's 55nm process. Figure 11 illustrates how the calibration of the ring oscillator affects the pulse width of the output signal when the calibration targets a 1ns pulse width under three different scenarios where the process, voltage and temperature were varied:

- Typical-Typical (TT): Simulated at 27°C with a 1.2V supply voltage.
- Slow-Slow (SS): Simulated at 40°C with a 1.08V supply voltage.
- Fast-Fast (FF): Simulated at -40°C with a 1.32V supply voltage.

[0054] These scenarios represent significant environmental and process variations that can cause substantial offsets in the output signal's pulse width. Although the PVT variations result in significant offset of the pulse width, after loop and load calibration, the real pulse width is close to 1ns, as close as picoseconds.

[0055] Figure 12 illustrates three plots that show the effectiveness of the calibration process performed by the digital calibrator module in correcting the pulse width of a PWM signal generator module that had been configured to generate a pulse having a width of 149ns. The simulation for all three plots were made under the assumption that the PWM signal generator module was experiencing an extreme PVT scenario: slow-slow (SS) corner, 40°C, and 1.08V.

[0056] The plots show the improvement in the accuracy of the pulse's width after the loop calibration and load calibration steps have been carried out. In particular, when no calibration steps were carried out, the simulated pulse had a width of 236.549 ns, which represents a +48.7% offset from the expected value of 149 ns. This large deviation may be attributed to the effects of process, voltage, and temperature variations. After a loop calibration step was carried out, it can be seen that the simulated pulse's width was reduced to 158.300 ns, significantly closer to the target of 149 ns, with an error of +6.2%. This loop calibration step was found to have introduced coarse corrections by adjusting the oscillator's loop count. After a load calibration step, it can be seen that simulated width of the pulse became 49.316 ns, bringing the error down to just +0.2%, effectively matching the expected output of 149 ns.

[0057] A flowchart showing a process 1300 for forming a digital PWM module in accordance with embodiments of the disclosure is illustrated in Figure 13. Process 1300 begins at step 1302 with process 1300 forming a PWM generator module to generate an output pulse signal having a predetermined width in response to receiving an input pulse signal. The formation of the PWM generator module causes process 1300 to form an edge detector module to generate a rising edge of the output pulse signal in response to detecting an edge of the input pulse signal and this takes place at step 1304. At step 1306, process 1300 then forms a coarse delay module to receive the rising edge signal, generates a periodic clock signal by propagating a signal through a feedback loop of delay elements, and provides a trigger to the edge detector module after a predetermined number of clock signals have been propagated through the feedback loop, whereby the edge detector module generates a falling edge of the output pulse signal upon receiving the trigger. Process 1300 then proceeds to step 1308 to form a digital calibrator module such that the digital calibrator module is coupled to the PWM signal generator module, whereby the digital calibrator module is formed to adjust a frequency of the periodic clock signal generated by the coarse delay module based on a target frequency of the periodic clock signal, a reference clock frequency and a predetermined threshold of clock cycles.

[0058] In embodiments of the disclosure, process 1300 forms a fine delay module, between the coarse delay module and the edge detector module, to receive the trigger after the predetermined number of clock signals have been propagated through the feedback loop of the coarse delay module, whereby the forming of the fine delay module comprises the steps of: forming a plurality of fine-delay elements, each fine-delay element comprising: a fine-delay cell configured to introduce a fine delay to the received trigger, and a switch arranged in series with the fine-delay cell such that the fine-delay cell is selected when the switch is turned on; provide the fine-delayed trigger to the edge detector module, wherein the fine delay introduced by each of the fine-delay elements is shorter than a time period of the clock signal generated by the coarse delay module.

[0059] In embodiments of the disclosure, process 1300 forms the coarse delay module by forming a ring oscillator to generate the periodic clock signal by propagating the signal through a loop of delay elements, forming a counter communicatively coupled to the ring oscillator, the

counter configured to count a number of loops of clock signals that propagated through the loop of delay elements, forming a comparator communicatively coupled to the counter, the comparator configured to compare a count of the counter with a predetermined delay value, and forming a digital register communicatively coupled to the comparator, the digital register configured to generate the trigger in response to the comparator matching the count of the counter with the predetermined delay value.

[0060] In embodiments of the disclosure, each delay element in the loop of delay elements of the ring oscillator comprises a delay cell, a loading capacitor and a switch, wherein the loading capacitor and the switch are arranged in parallel with respect to the delay cell.

[0061] In embodiments of the disclosure, the digital calibrator module is configured to adjust the frequency of the periodic clock signal by obtaining the predetermined threshold of the clock cycles based on the reference clock frequency and the target frequency of the periodic clock signal; and iteratively increasing a number of delay elements in the loop of delay elements of the ring oscillator until a number of clock signals generated by the ring oscillator during the predetermined time interval meets or exceeds the predetermined threshold of the clock cycles.

[0062] In embodiments of the disclosure, the digital calibrator module is configured to further refine the adjusted frequency of the periodic clock signal by iteratively increasing a number of loads in each delay element in the loop of delay elements of the ring oscillator until the number of clock signals generated by the ring oscillator during the predetermined time interval meets or exceeds the predetermined threshold of the clock cycles.

[0063] In embodiments of the disclosure, the digital calibrator module is configured to determine the number of fine-delay elements in the fine delay module by obtaining a predetermined fine-delay threshold, and iteratively increasing a number of fine-delay elements in the fine delay module until a total delay introduced by the fine delay module meets or exceeds the predetermined fine-delay threshold. Each delay element may be electrically coupled to a bank of capacitors via a bank of switches that are controlled by the digital calibrator module and/or the switch of each delay element may be controlled by the digital

calibrator module. In embodiments of the disclosure, the switch of each fine-delay element may be controlled by the digital calibrator module.

[0064] Numerous other changes, substitutions, variations, and modifications may be ascertained by the skilled in the art and it is intended that the present application encompass all such changes, substitutions, variations, and modifications as falling within the scope of the appended claims.

CLAIMS:

1. A digital pulse width modulation (PWM) module comprising:

a PWM signal generator module configured to generate an output pulse signal having a predetermined width in response to receiving an input pulse signal, the PWM signal generator module comprising:

an edge detector module configured to generate a rising edge of the output pulse signal in response to detecting an edge of the input pulse signal;

a coarse delay module configured to receive the rising edge signal, generate a periodic clock signal by propagating a signal through a feedback loop of delay elements, and provide a trigger to the edge detector module after a predetermined number of clock signals have been propagated through the feedback loop,

whereby the edge detector module generates a falling edge of the output pulse signal upon receiving the trigger; and

a digital calibrator module coupled to the PWM signal generator module, the digital calibrator module configured to adjust a frequency of the periodic clock signal generated by the coarse delay module based on a target frequency of the periodic clock signal, a reference clock frequency and a predetermined threshold of clock cycles.

2. The digital PWM module according to claim 1 further comprising a fine delay module positioned between the coarse delay module and the edge detector module, the fine delay module configured to:

receive the trigger after the predetermined number of clock signals have been propagated through the feedback loop of the coarse delay module, the fine delay module comprising:

a plurality of fine-delay elements, each fine-delay element comprising:

a fine-delay cell configured to introduce a fine delay to the received trigger, and a switch arranged in series with the fine-delay cell such that the fine-delay cell is selected when the switch is turned on;

provide the fine-delayed trigger to the edge detector module,

wherein the fine delay introduced by each of the fine-delay elements is shorter than a time period of the clock signal generated by the coarse delay module.

3. The digital PWM module according to claims 1 or 2, wherein the coarse delay module comprises:

a ring oscillator configured to generate the periodic clock signal by propagating the signal through a loop of delay elements;

a counter communicatively coupled to the ring oscillator, the counter configured to count a number of loops of clock signals that propagated through the loop of delay elements;

a comparator communicatively coupled to the counter, the comparator configured to compare a count of the counter with a predetermined delay value; and

a digital register communicatively coupled to the comparator, the digital register configured to generate the trigger in response to the comparator matching the count of the counter with the predetermined delay value.

4. The digital PWM module according to claim 3, wherein each delay element in the loop of delay elements of the ring oscillator comprises a delay cell, a loading capacitor and a switch, wherein the loading capacitor and the switch are arranged in parallel with respect to the delay cell.

5. The digital PWM module according to claim 3, wherein the digital calibrator module is configured to adjust the frequency of the periodic clock signal by:

obtaining the predetermined threshold of the clock cycles based on the reference clock frequency and the target frequency of the periodic clock signal; and

iteratively increasing a number of delay elements in the loop of delay elements of the ring oscillator until a number of clock signals generated by the ring oscillator during the predetermined time interval meets or exceeds the predetermined threshold of the clock cycles.

6. The digital PWM module according to claim 5, wherein the digital calibrator module is configured to further refine the adjusted frequency of the periodic clock signal by:

iteratively increasing a number of loads in each delay element in the loop of delay elements of the ring oscillator until the number of clock signals generated by the ring oscillator during the predetermined time interval meets or exceeds the predetermined threshold of the clock cycles.

7. The digital PWM module according to claim 2, wherein the digital calibrator module is configured to determine the number of fine-delay elements in the fine delay module by:

obtaining a predetermined fine-delay threshold; and

iteratively increasing a number of fine-delay elements in the fine delay module until a total delay introduced by the fine delay module meets or exceeds the predetermined fine-delay threshold.

8. The digital PWM module according to claim 5, wherein each delay element is electrically coupled to a bank of capacitors via a bank of switches that are controlled by the digital calibrator module.

9. The digital PWM module according to claim 4, wherein the switch of each delay element is controlled by the digital calibrator module.

10. The digital PWM module according to claim 7, wherein the switch of each fine-delay element is controlled by the digital calibrator module.

11. A method for forming a digital pulse width modulation (PWM) module, the method comprising:

forming a PWM signal generator module to generate an output pulse signal having a predetermined width in response to receiving an input pulse signal, whereby the forming of the PWM signal generator module comprises the steps of:

forming an edge detector module to generate a rising edge of the output pulse signal in response to detecting an edge of the input pulse signal;

forming a coarse delay module to receive the rising edge signal, generate a periodic clock signal by propagating a signal through a feedback loop of delay elements, and provide a trigger to the edge detector module after a predetermined number of clock signals have been propagated through the feedback loop,

whereby the edge detector module generates a falling edge of the output pulse signal upon receiving the trigger; and

forming a digital calibrator module such that the digital calibrator module is coupled to the PWM signal generator module, whereby the digital calibrator module is formed to adjust a frequency of the periodic clock signal generated by the coarse delay module based on a target

frequency of the periodic clock signal, a reference clock frequency and a predetermined threshold of clock cycles.

12. The method according to claim 11 further comprising the steps of:

forming a fine delay module, between the coarse delay module and the edge detector module, to:

receive the trigger after the predetermined number of clock signals have been propagated through the feedback loop of the coarse delay module, whereby the forming of the fine delay module comprises the steps of:

forming a plurality of fine-delay elements, each fine-delay element comprising:

a fine-delay cell configured to introduce a fine delay to the received trigger, and a switch arranged in series with the fine-delay cell such that the fine-delay cell is selected when the switch is turned on;

provide the fine-delayed trigger to the edge detector module,

wherein the fine delay introduced by each of the fine-delay elements is shorter than a time period of the clock signal generated by the coarse delay module.

13. The method according to claims 11 or 12, wherein the forming of the coarse delay module comprises the steps of:

forming a ring oscillator to generate the periodic clock signal by propagating the signal through a loop of delay elements;

forming a counter communicatively coupled to the ring oscillator, the counter configured to count a number of loops of clock signals that propagated through the loop of delay elements;

forming a comparator communicatively coupled to the counter, the comparator configured to compare a count of the counter with a predetermined delay value; and

forming a digital register communicatively coupled to the comparator, the digital register configured to generate the trigger in response to the comparator matching the count of the counter with the predetermined delay value.

14. The method according to claim 13, wherein each delay element in the loop of delay elements of the ring oscillator comprises a delay cell, a loading capacitor and a switch, wherein the loading capacitor and the switch are arranged in parallel with respect to the delay cell.

15. The method according to claim 13, wherein the formed digital calibrator module is configured to adjust the frequency of the periodic clock signal by:

obtaining the predetermined threshold of the clock cycles based on the reference clock frequency and the target frequency of the periodic clock signal; and

iteratively increasing a number of delay elements in the loop of delay elements of the ring oscillator until a number of clock signals generated by the ring oscillator during the predetermined time interval meets or exceeds the predetermined threshold of the clock cycles.

16. The method according to claim 15, wherein the digital calibrator module is configured to further refine the adjusted frequency of the periodic clock signal by:

iteratively increasing a number of loads in each delay element in the loop of delay elements of the ring oscillator until the number of clock signals generated by the ring oscillator during the predetermined time interval meets or exceeds the predetermined threshold of the clock cycles.

17. The method according to claim 12, wherein the digital calibrator module is configured to determine the number of fine-delay elements in the fine delay module by:

obtaining a predetermined fine-delay threshold; and

iteratively increasing a number of fine-delay elements in the fine-delay module until a total delay introduced by the fine delay module meets or exceeds the predetermined fine-delay threshold.

18. The method according to claim 15, wherein each delay element is electrically coupled to a bank of capacitors via a bank of switches that are controlled by the digital calibrator module.

19. The method module according to claim 14, wherein the switch of each delay element is controlled by the digital calibrator module.

20. The method according to claim 17, wherein the switch of each fine-delay element is controlled by the digital calibrator module.