



INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification ⁶ : H04N 5/44, 5/46		A1	(11) International Publication Number: ✓ WO 98/27721
			(43) International Publication Date: 25 June 1998 (25.06.98)
(21) International Application Number: ✓ PCT/US97/22854		(81) Designated States: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, GH, HU, ID, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, TJ, TM, TR, TT, UA, UG, US, UZ, VN, YU, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG).	
(22) International Filing Date: ✓ 15 December 1997 (15.12.97)			
(30) Priority Data: ✓ 96402785.8 ✓ 18 December 1996 (18.12.96) EP (34) Countries for which the regional or international application was filed: FR et al.			
(71) Applicant (for all designated States except US): THOMSON CONSUMER ELECTRONICS, INC. [US/US]; 10330 North Meridian Street, Indianapolis, IN 46290-1024 (US). ✓		Published With international search report.	
(72) Inventors; and			
(75) Inventors/Applicants (for US only): CHRISTOPHER, Todd [US/US]; 1402 South Kitley Avenue, Indianapolis, IN 46203 (US); CANFIELD, Barth, Alan [US/US]; 10421 Indian Lake Boulevard North Drive, Indianapolis, IN 46236 (US). 3 PATTON, Steven, Wayne [US/US]; 7747 South Louthan Street, Littleton, CO 80120 (US). ✓			
(74) Agents: TRIPOLI, Joseph, S. et al.; GE & RCA Licensing Management Operation Inc., P.O. Box 5312, Princeton, NJ 08543 (US).			

(54) Title: MEMORY ARCHITECTURE FOR A MULTIPLE FORMAT VIDEO SIGNAL PROCESSOR **✓**

(57) Abstract

A video decoder (10) transcodes video data from various input formats to a predetermined output format. Input data may be standard definition (NTSC or PAL) data or MPEG2 compressed data. Standard definition data are rearranged into block format to be compatible with the decoder's (10) single display processor (40). The display processor selectively processes and conveys either MPEG2 format data or non-MPEG2 format data to a display device. A block based frame memory (20) stores MPEG2 and non-MPEG2 pixel block data, as well as standard definition data in raster line format during processing.

