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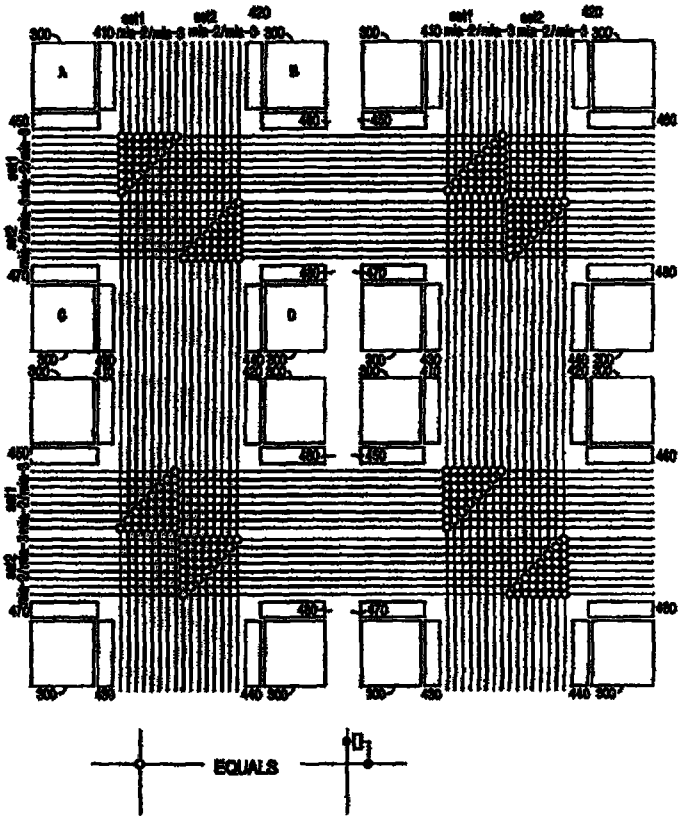
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(54) Title: FLOOR PLAN FOR SCALABLE MULTIPLE LEVEL INTERCONNECT ARCHITECTURE

(57) Abstract

A programmable logic device which incorporates an innovative routing hierarchy consisting of the multiple levels of routing lines, connector tab networks and turn matrices, enables an innovative, space saving floor plan to be utilized in an integrated circuit implementation, and is particularly efficient when an SRAM is used as the configuration bit. This floor plan is a scalable block architecture in which each block connector tab networks (410, 420, 430, 440, 450, 460, 470, 480) of a 2x2 block grouping (A, B, C) is arranged as a mirror image along the adjacent axis relative to each other. Furthermore, the bidirectional input/output lines are provided as the input/output means for each block (300) are oriented only in two directions (instead of the typical north, south, east and west directions) such that the block connector tab networks for adjacent blocks face each other in orientation. This orientation and arrangement permits blocks (300) to share routing resources. In addition, this arrangement enables a 4x4 block grouping to be scalable.



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