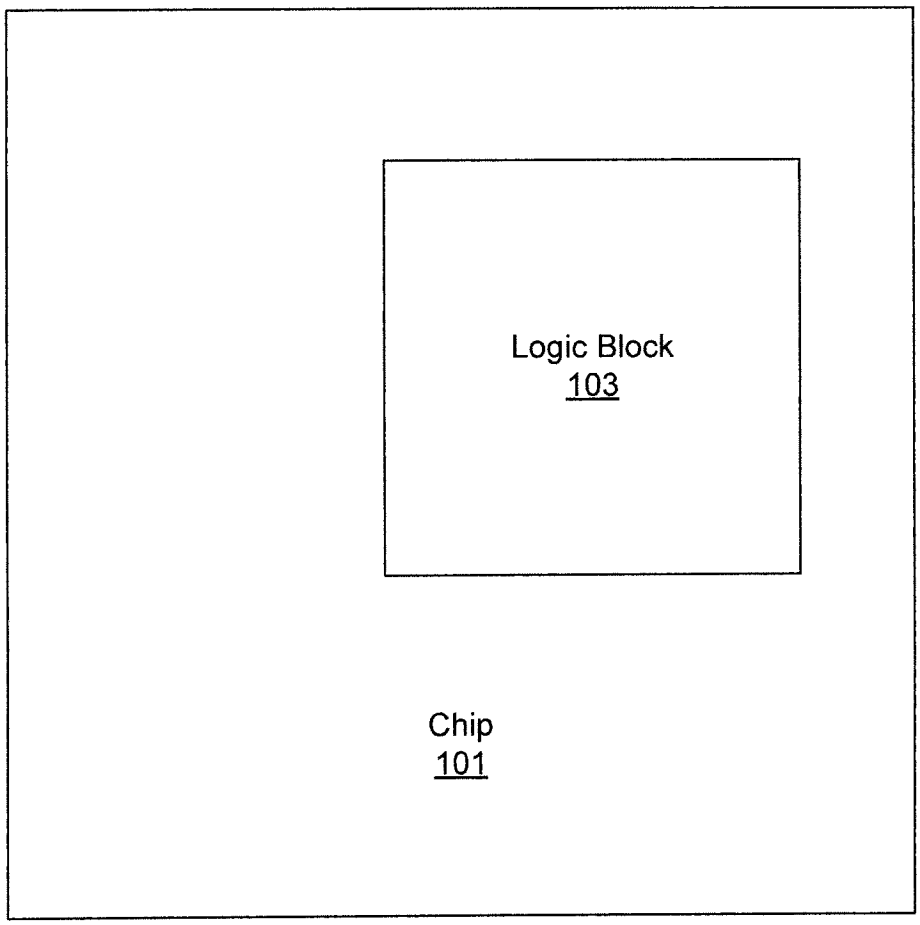


Fig. 1A

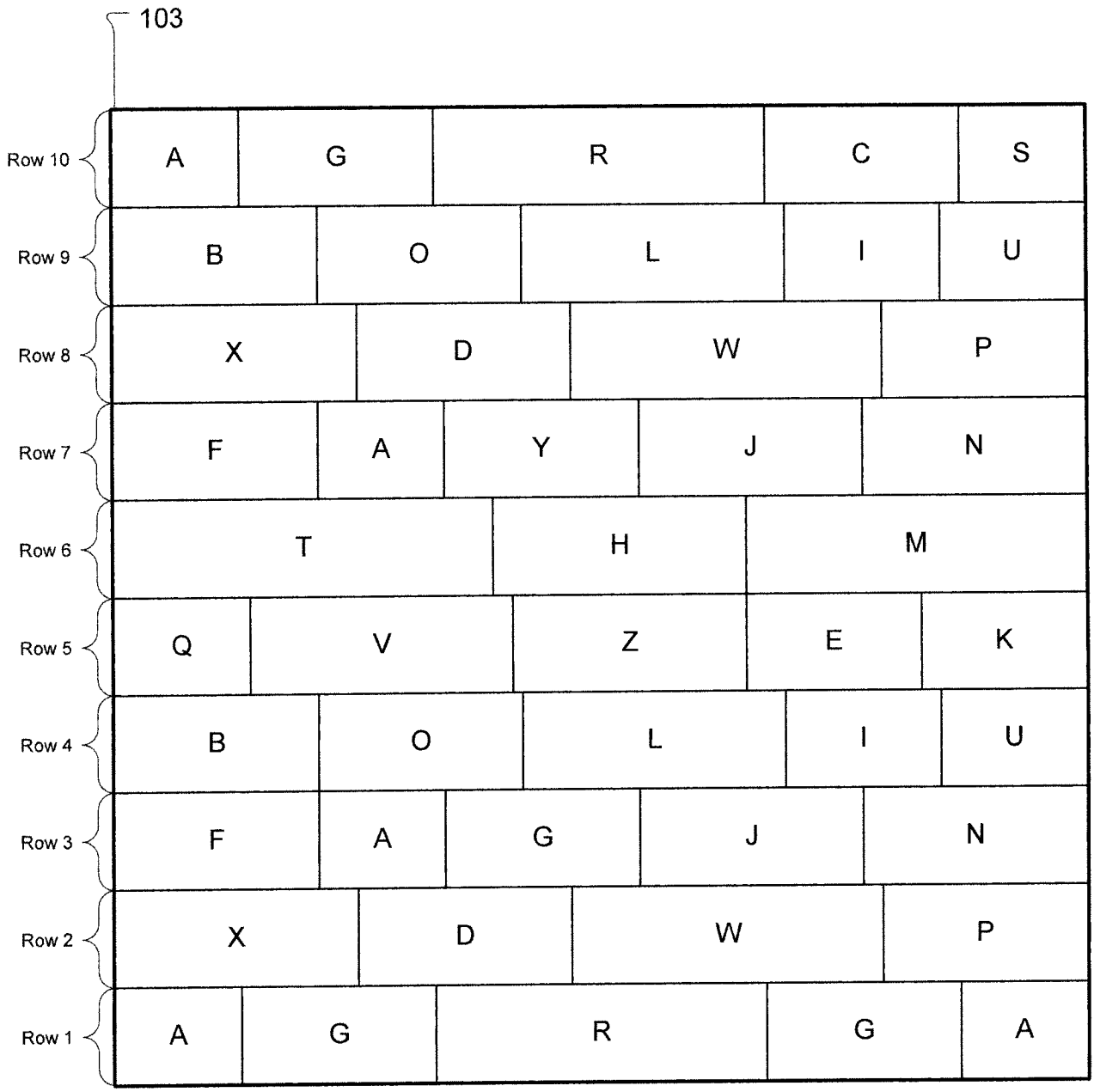

103
Row 10
A G R C S
Row 9
B O L I U
Row 8
X D W P
Row 7
F A Y J N
Row 6
T H M
Row 5
Q V Z E K
Row 4
B O L I U
Row 3
F A G J N
Row 2
X D W P
Row 1
A G R G A

Fig. 1B

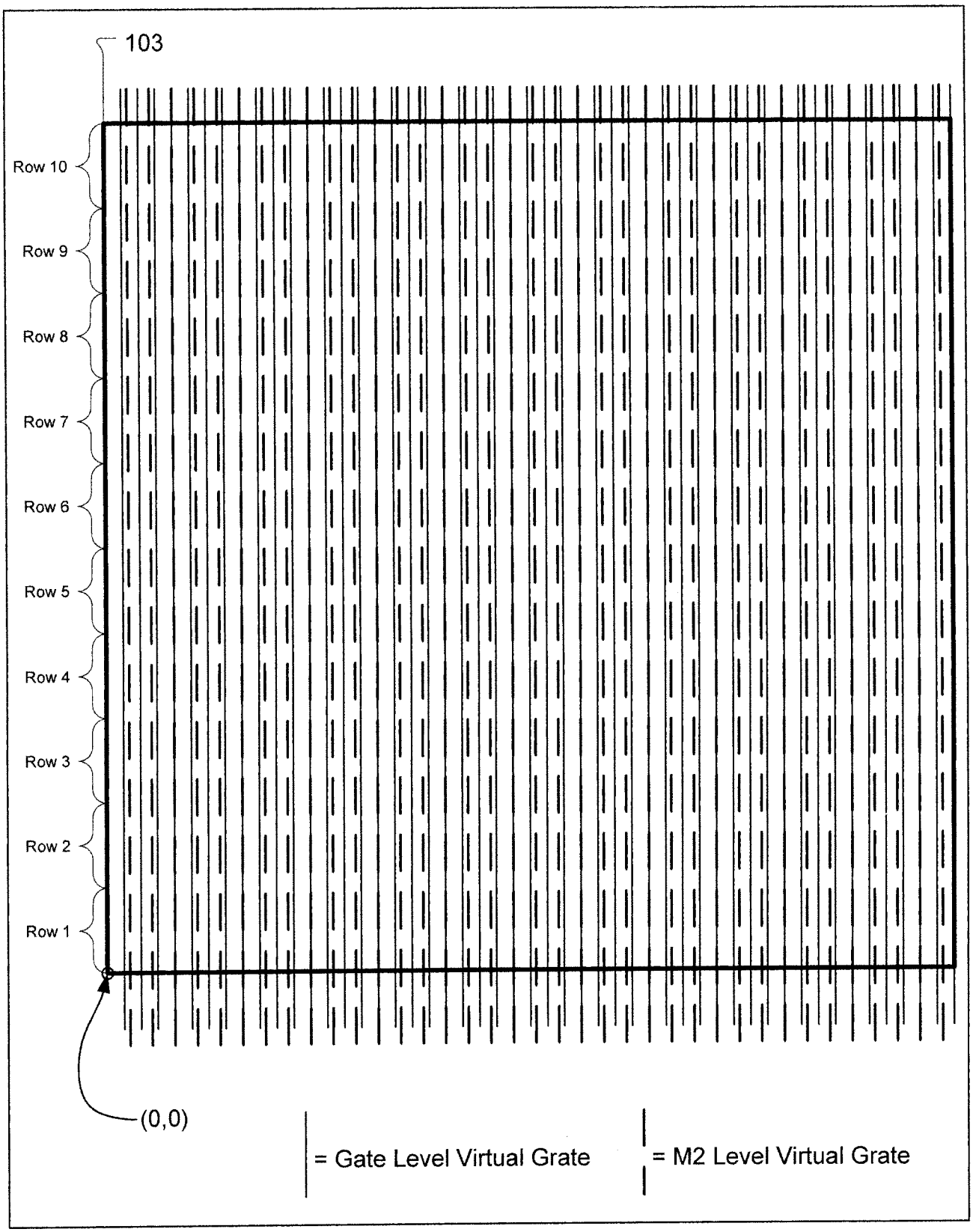

103
Row 10
Row 9
Row 8
Row 7
Row 6
Row 5
Row 4
Row 3
Row 2
Row 1
(0,0)
= Gate Level Virtual Grate
= M2 Level Virtual Grate

Fig. 2A

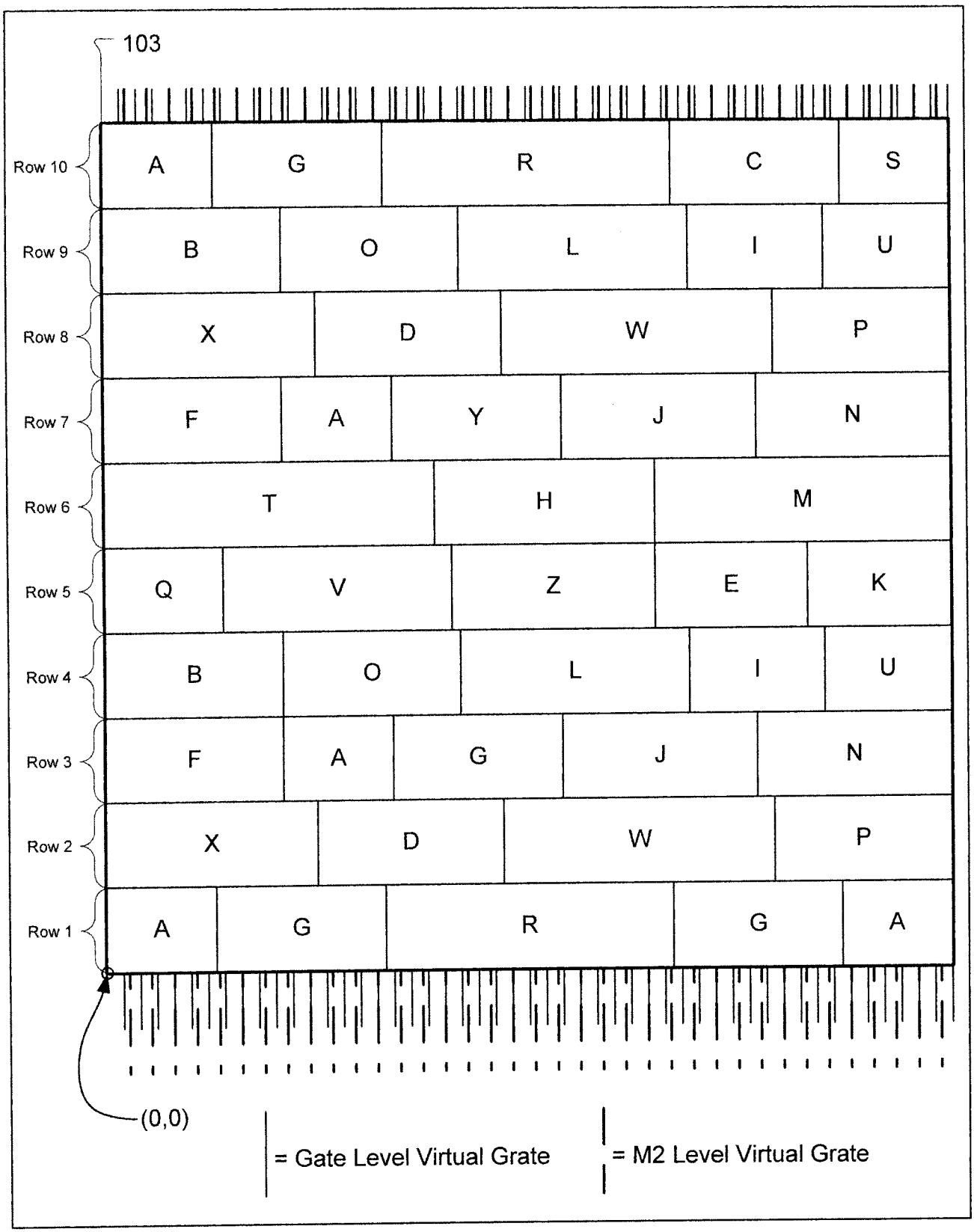

103
Row 10
A G R C S
Row 9
B O L I U
Row 8
X D W P
Row 7
F A Y J N
Row 6
T H M
Row 5
Q V Z E K
Row 4
B O L I U
Row 3
F A G J N
Row 2
X D W P
Row 1
A G R G A
(0,0)
= Gate Level Virtual Grate
= M2 Level Virtual Grate

Fig. 2B

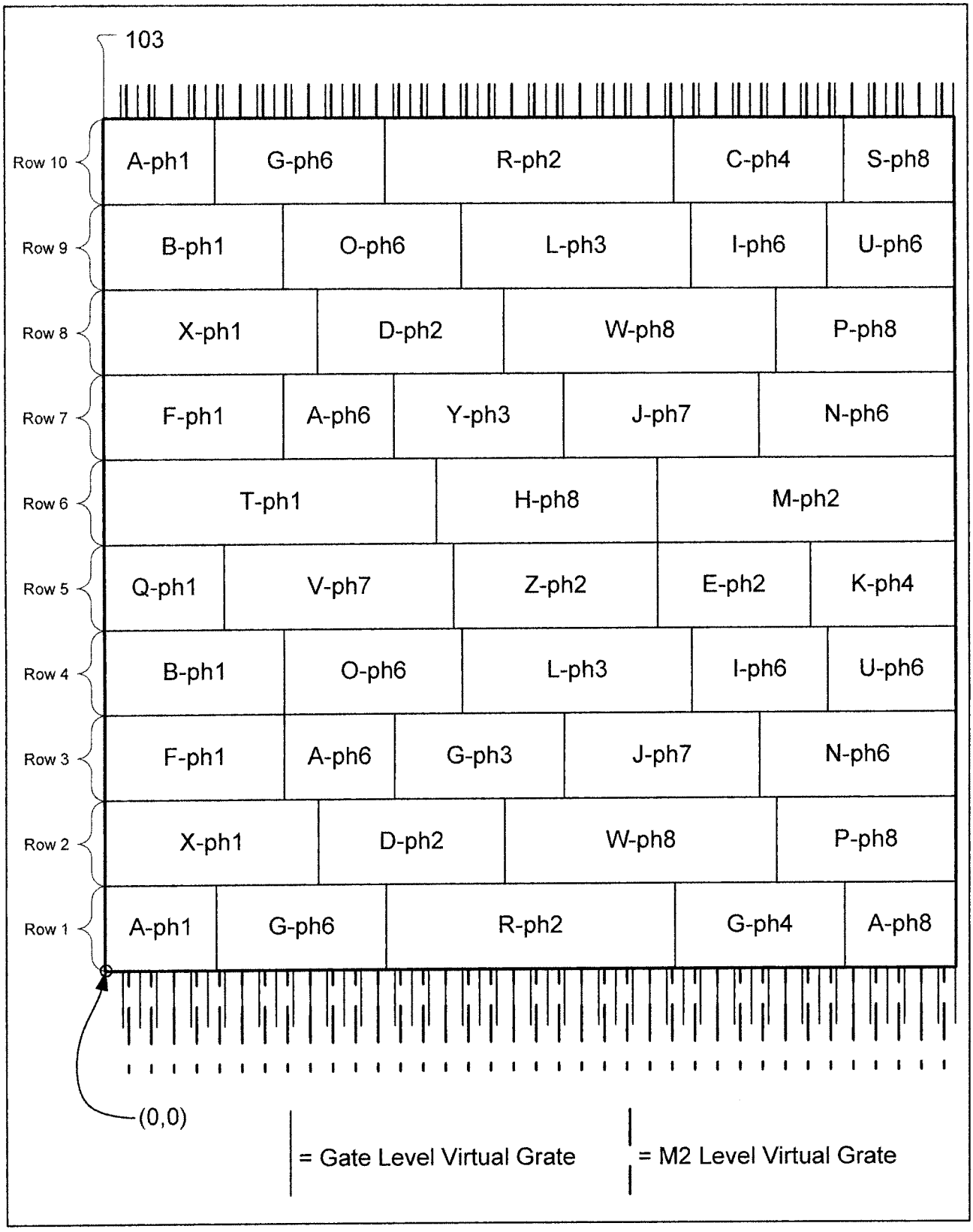

103
Row 10
A-ph1
G-ph6
R-ph2
C-ph4
S-ph8
Row 9
B-ph1
O-ph6
L-ph3
I-ph6
U-ph6
Row 8
X-ph1
D-ph2
W-ph8
P-ph8
Row 7
F-ph1
A-ph6
Y-ph3
J-ph7
N-ph6
Row 6
T-ph1
H-ph8
M-ph2
Row 5
Q-ph1
V-ph7
Z-ph2
E-ph2
K-ph4
Row 4
B-ph1
O-ph6
L-ph3
I-ph6
U-ph6
Row 3
F-ph1
A-ph6
G-ph3
J-ph7
N-ph6
Row 2
X-ph1
D-ph2
W-ph8
P-ph8
Row 1
A-ph1
G-ph6
R-ph2
G-ph4
A-ph8
(0,0)
= Gate Level Virtual Grate
= M2 Level Virtual Grate

Fig. 2C

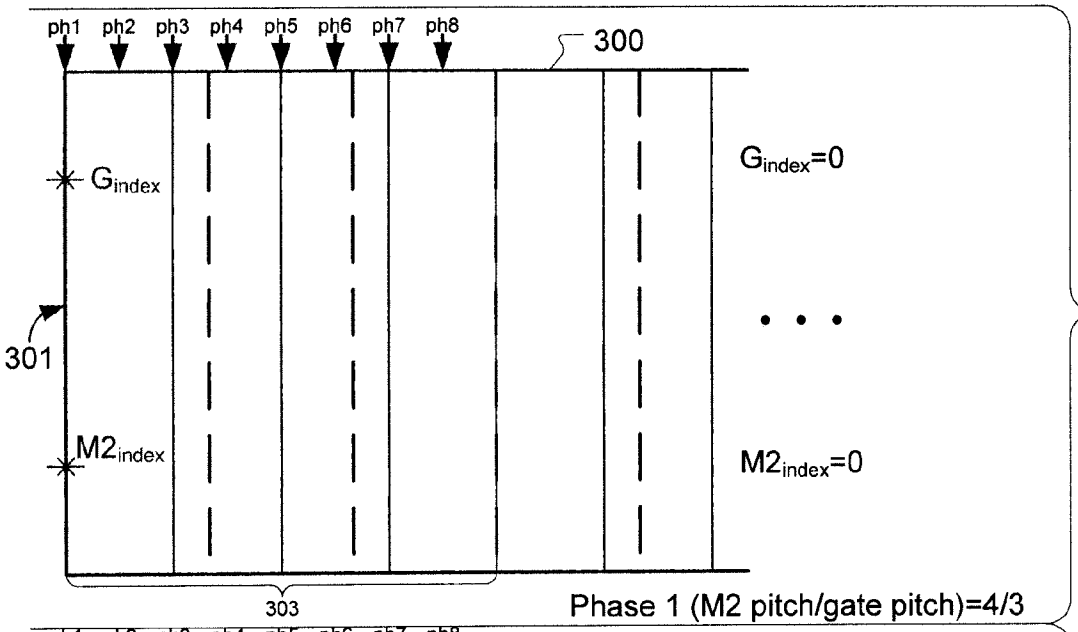


Fig. 3A

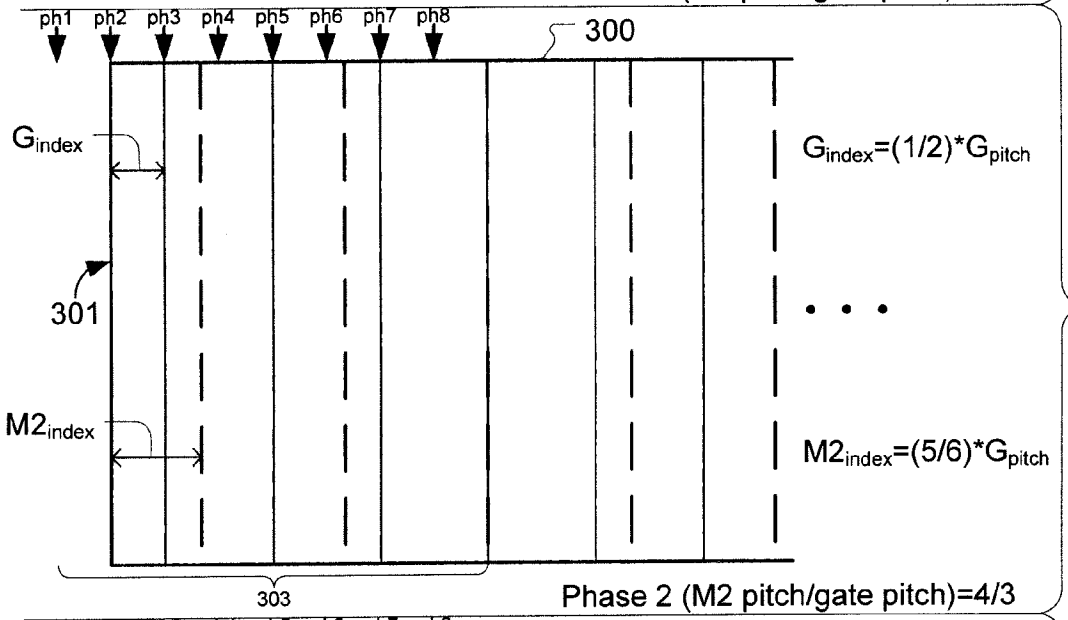


Fig. 3B

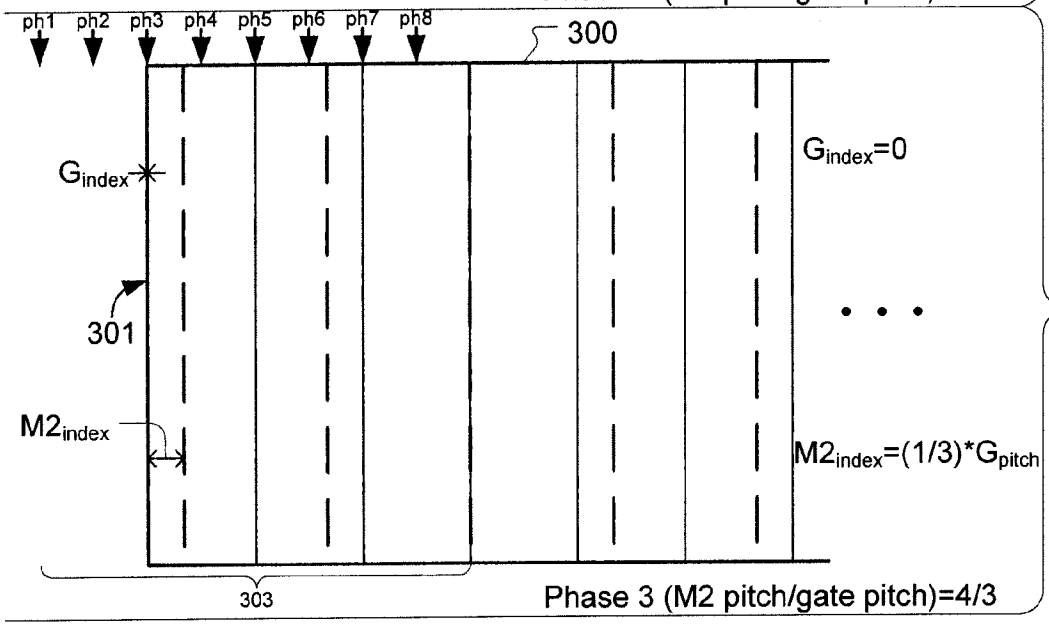


Fig. 3C

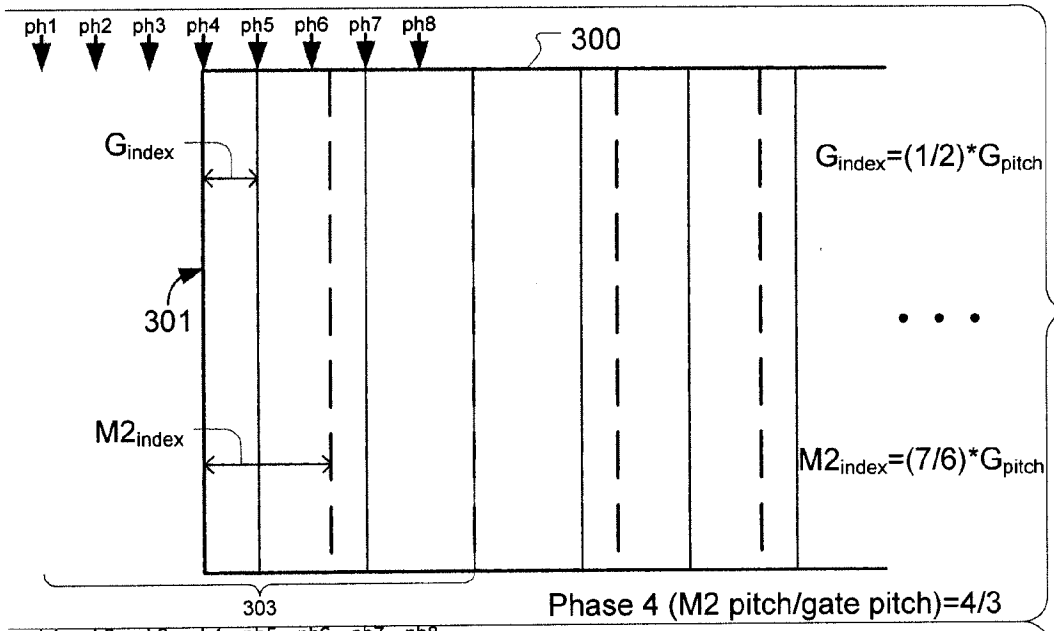


Fig. 3D

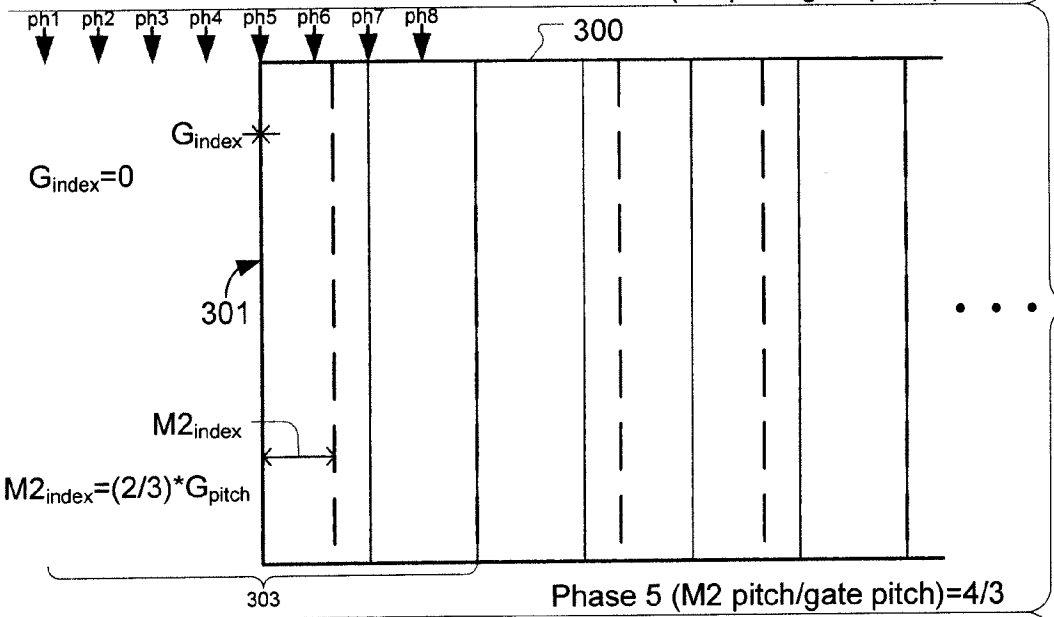


Fig. 3E

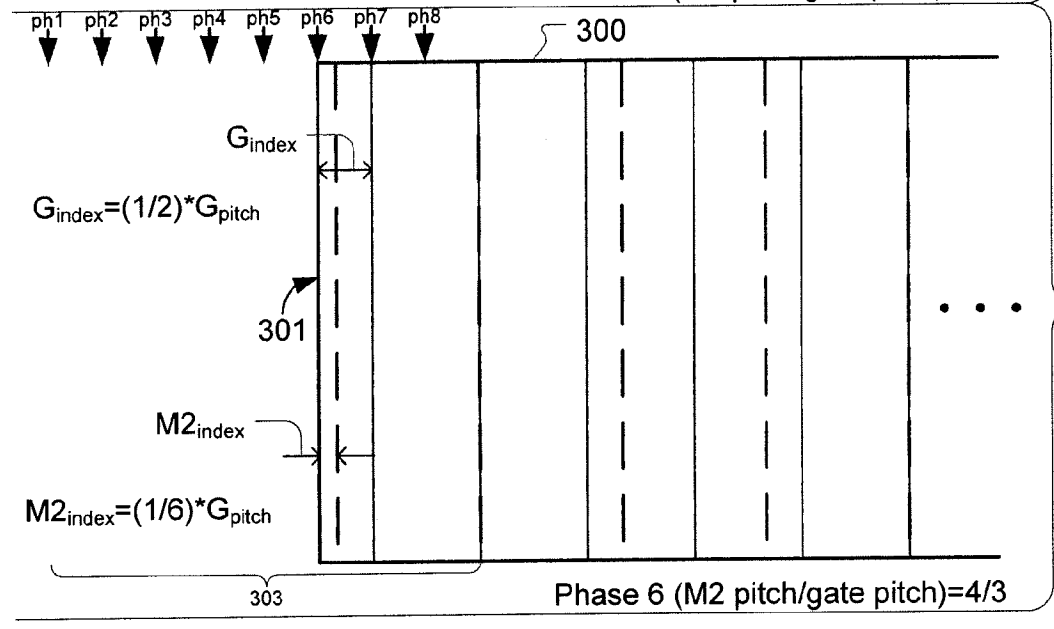


Fig. 3F

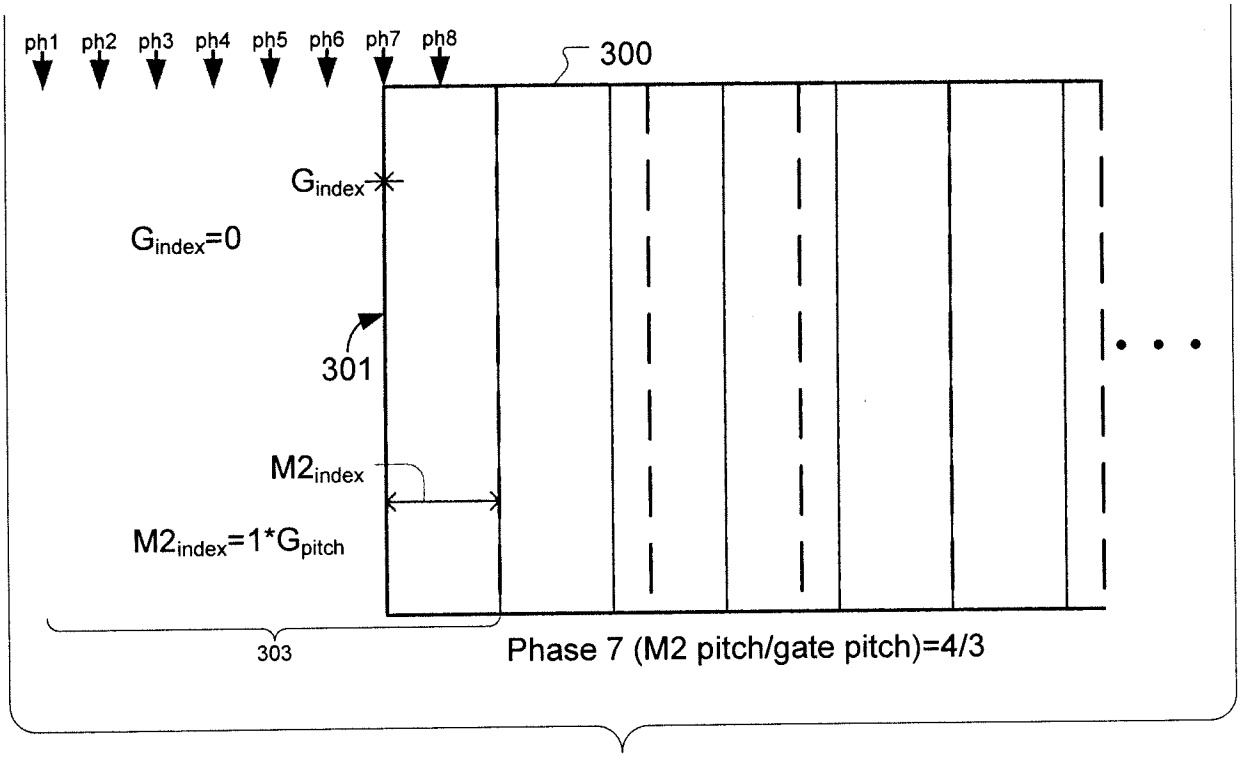

ph1
ph2
ph3
ph4
ph5
ph6
ph7
ph8
300
G_{index}
G_{index}=0
301
$M2_{index}$
$M2_{index}$=1*G_{pitch}
303
Phase 7 (M2 pitch/gate pitch)=4/3

Fig. 3G

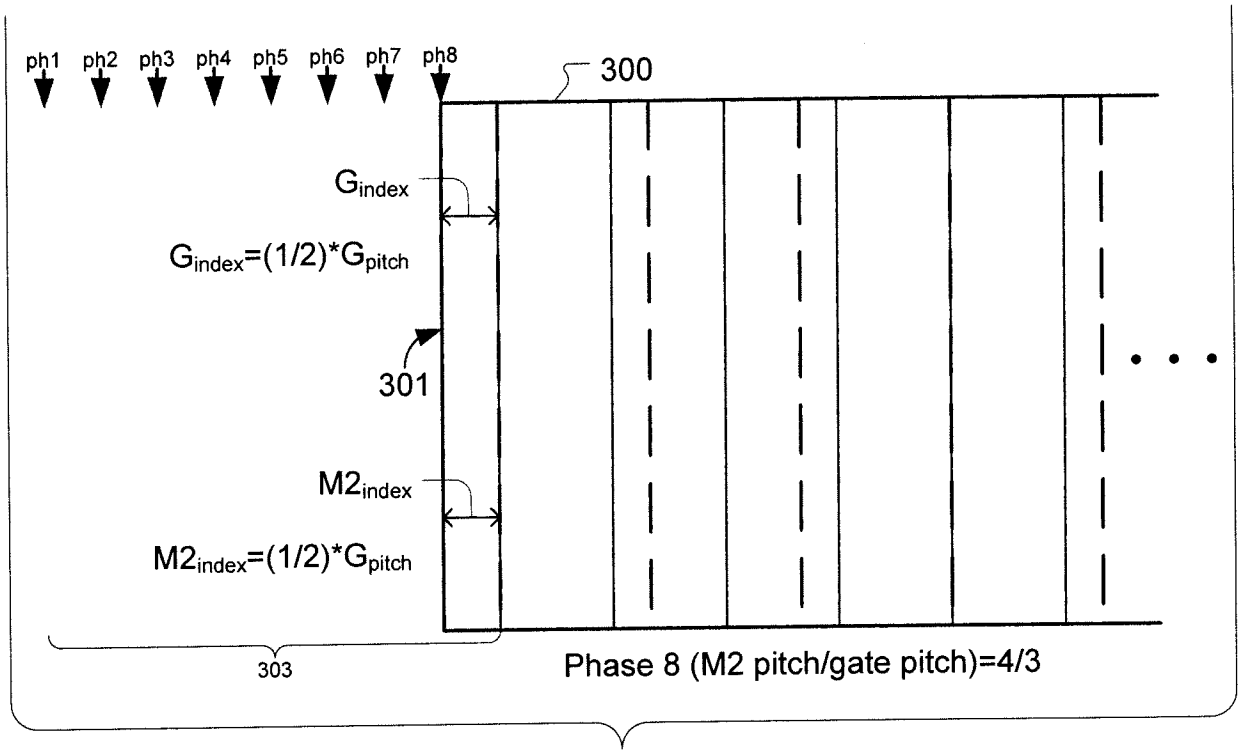

ph1
ph2
ph3
ph4
ph5
ph6
ph7
ph8
300
G_{index}
G_{index}=(1/2)*G_{pitch}
301
$M2_{index}$
$M2_{index}$=(1/2)*G_{pitch}
303
Phase 8 (M2 pitch/gate pitch)=4/3

Fig. 3H

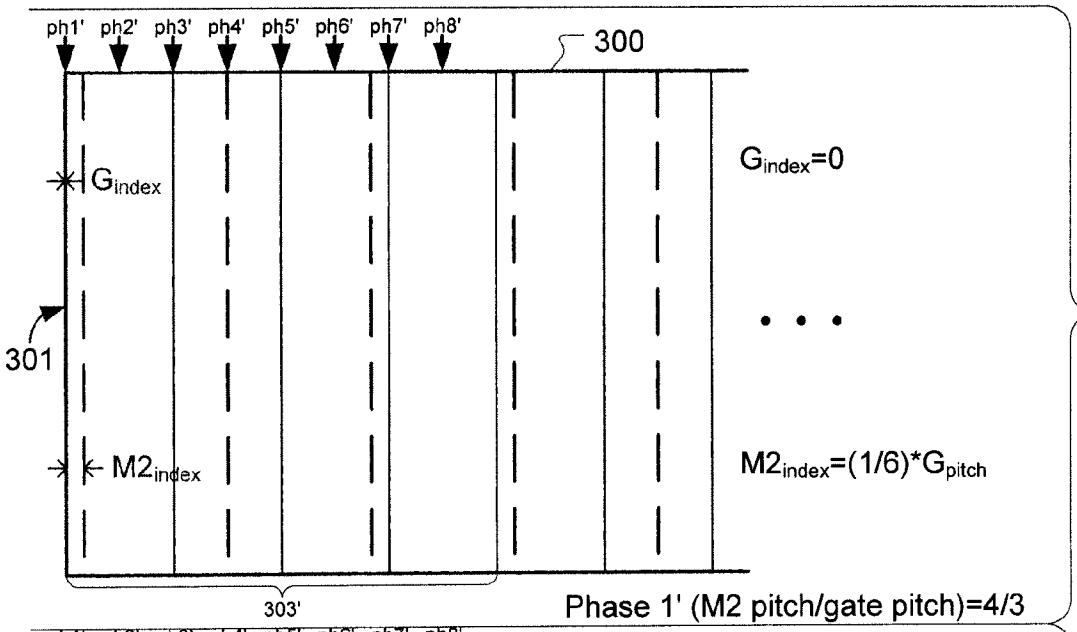


Fig. 3I

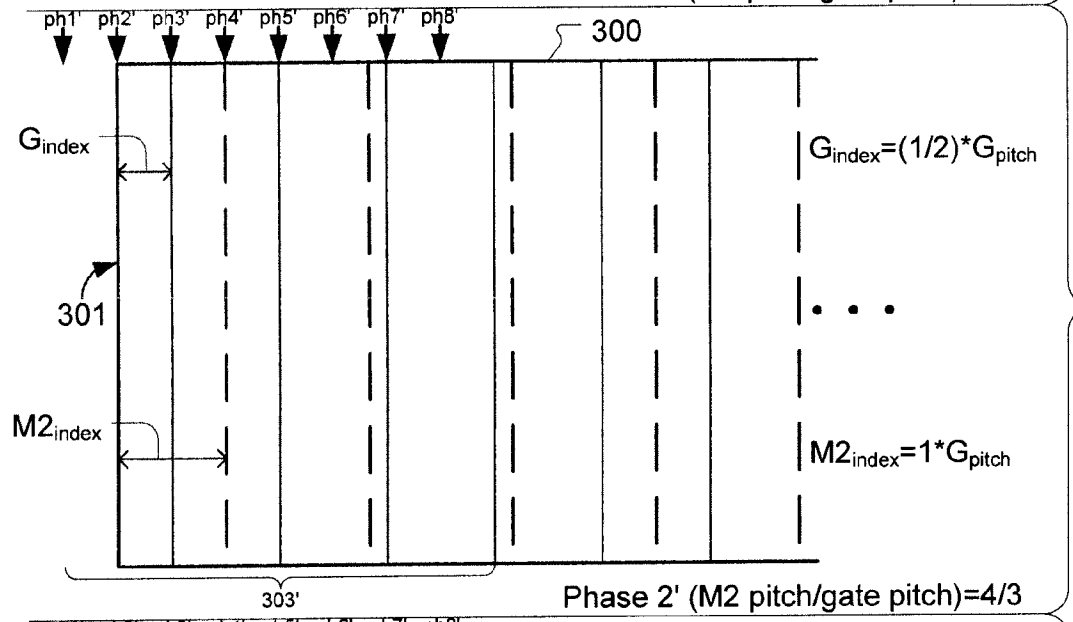


Fig. 3J

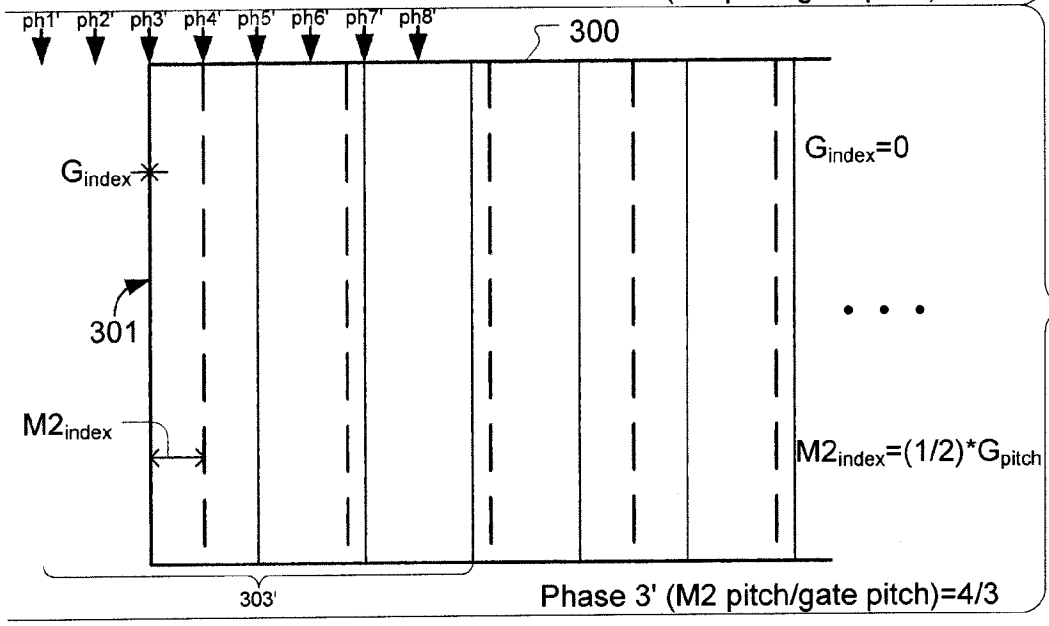


Fig. 3K

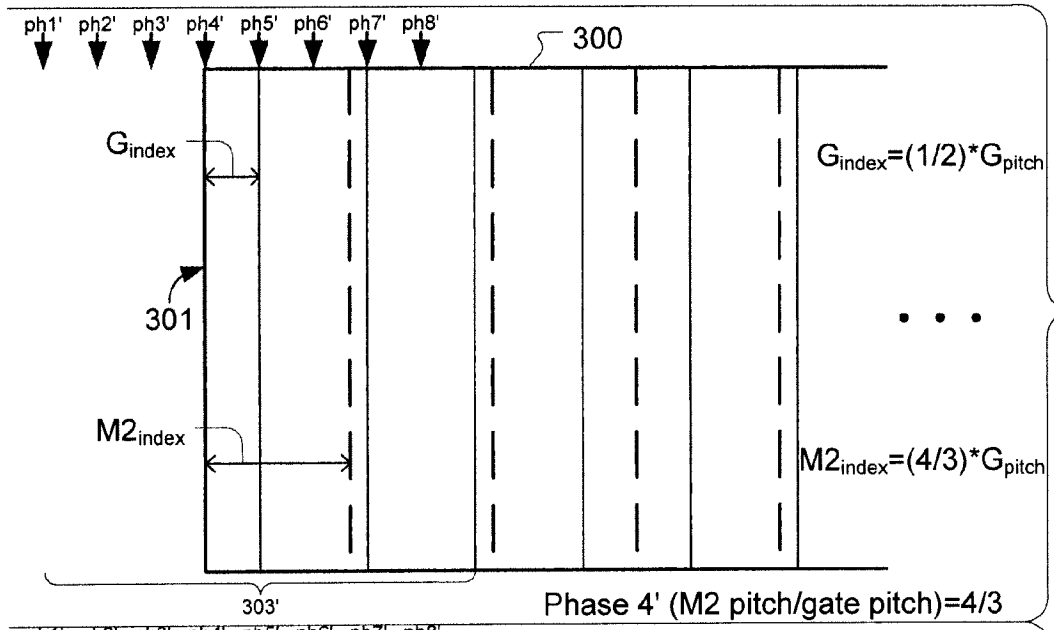


Fig. 3L

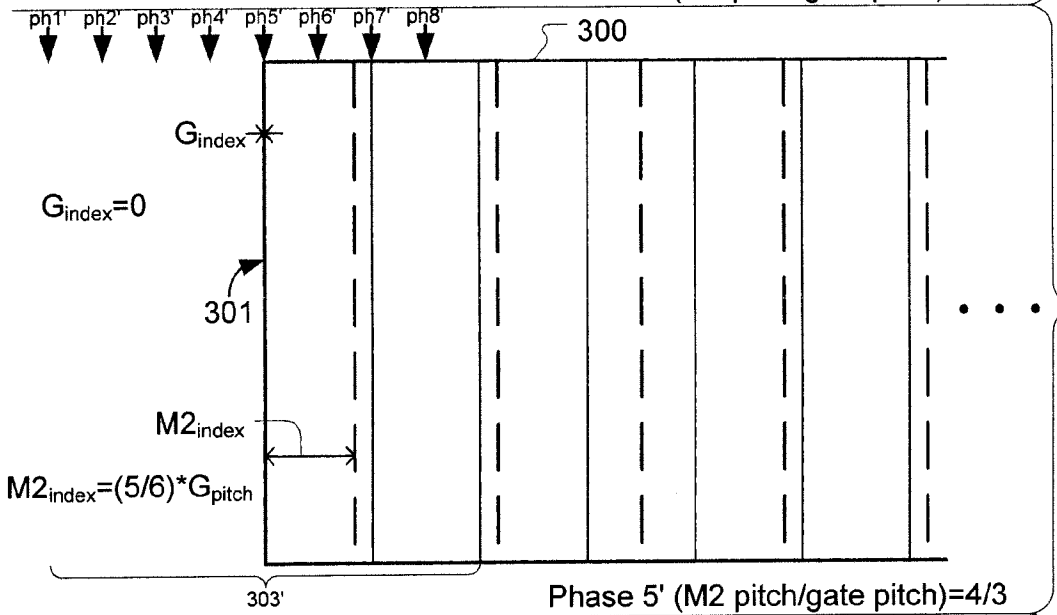


Fig. 3M

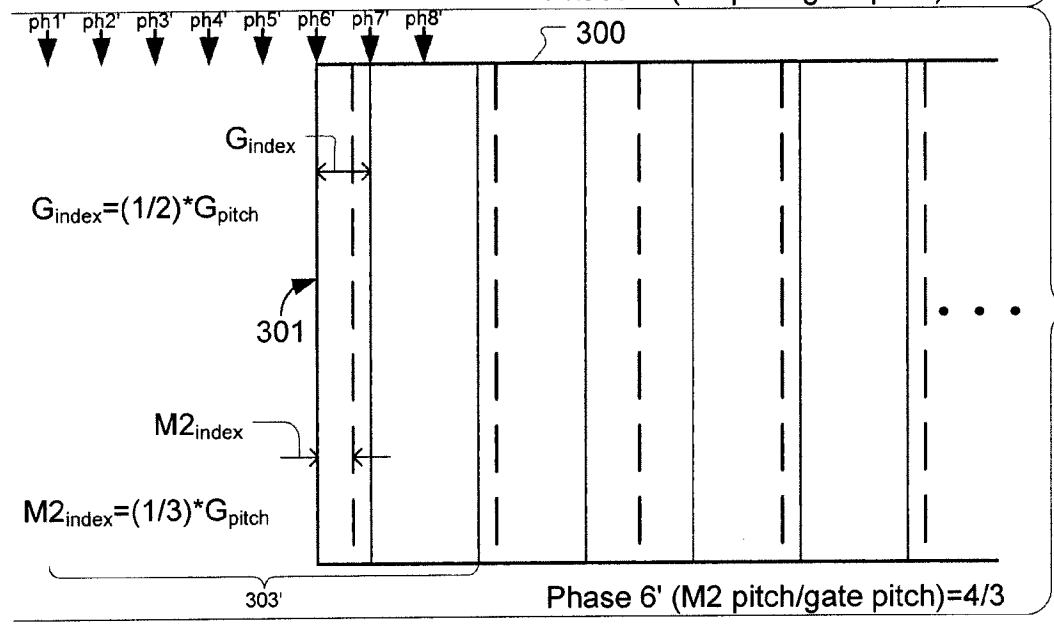


Fig. 3N

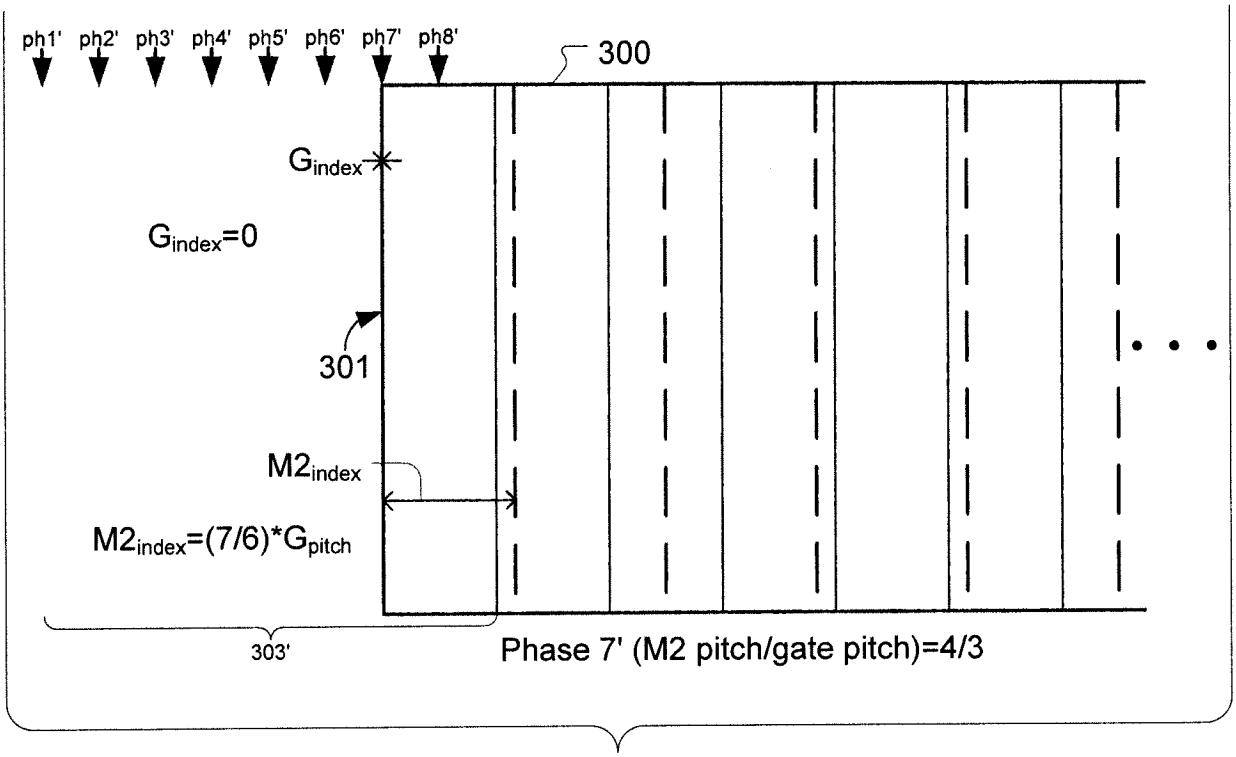

ph1' ph2' ph3' ph4' ph5' ph6' ph7' ph8'
300
G_{index}
G_{index}=0
301
$M2_{index}$
$M2_{index}$=(7/6)*G_{pitch}
303'
Phase 7' (M2 pitch/gate pitch)=4/3

Fig. 3O

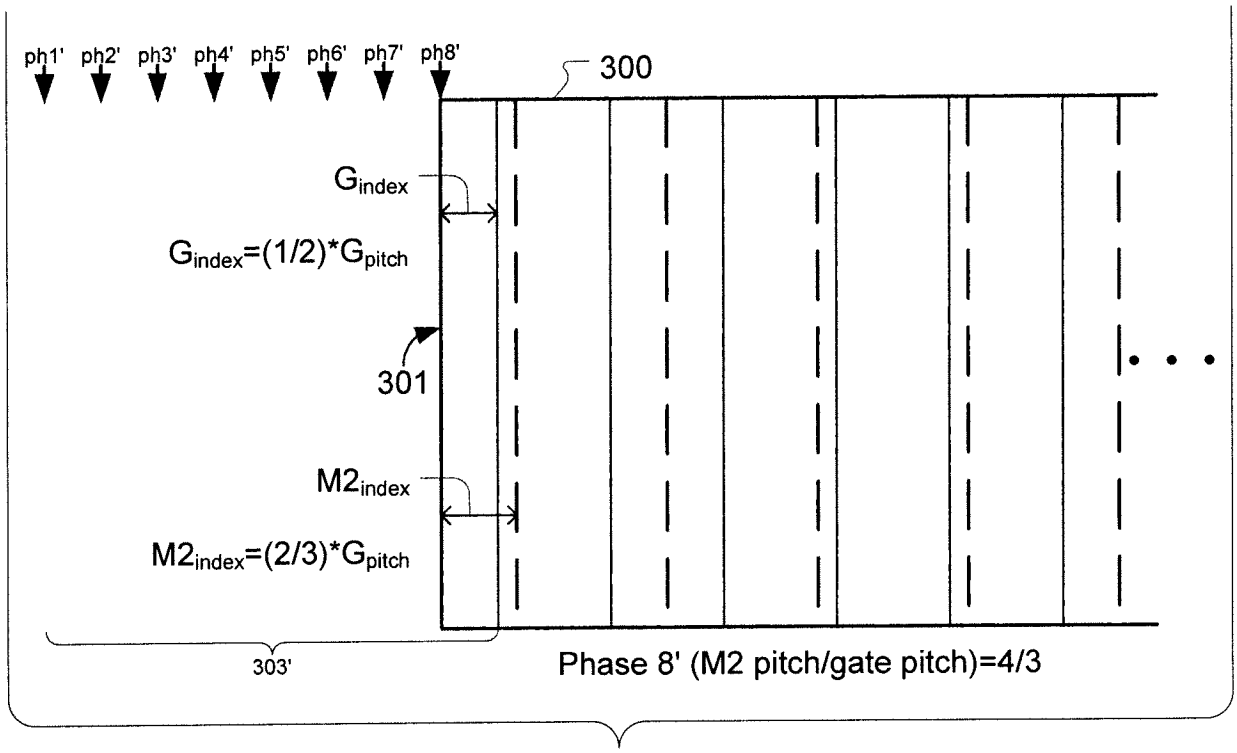

ph1' ph2' ph3' ph4' ph5' ph6' ph7' ph8'
300
G_{index}
G_{index}=(1/2)*G_{pitch}
301
$M2_{index}$
$M2_{index}$=(2/3)*G_{pitch}
303'
Phase 8' (M2 pitch/gate pitch)=4/3

Fig. 3P

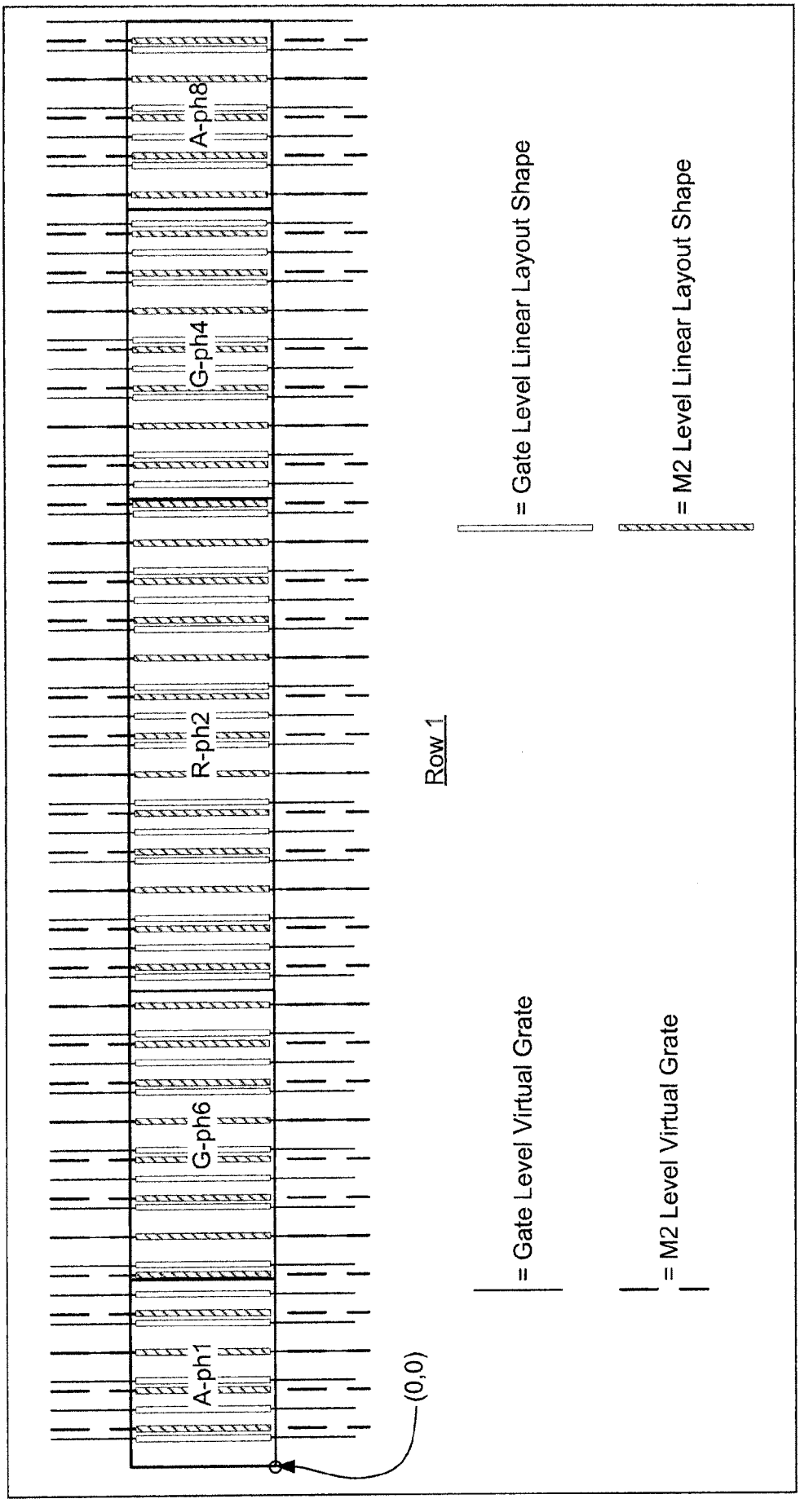

A-ph8
G-ph4
R-ph2
G-ph6
A-ph1
(0,0)
Row 1
= Gate Level Linear Layout Shape
= M2 Level Linear Layout Shape
= Gate Level Virtual Grate
= M2 Level Virtual Grate

Fig. 4

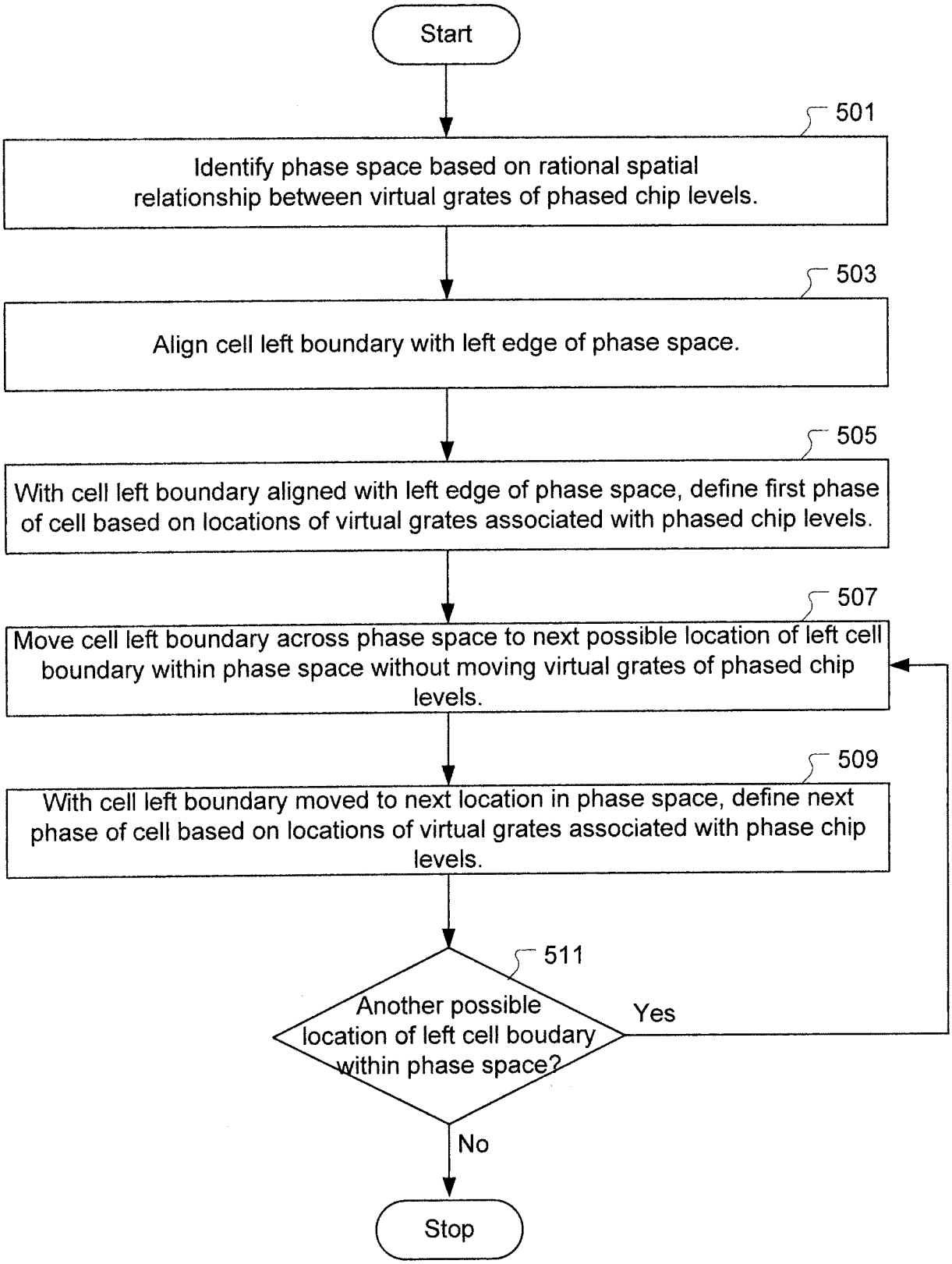

Start
501
Identify phase space based on rational spatial relationship between virtual grates of phased chip levels.
503
Align cell left boundary with left edge of phase space.
505
With cell left boundary aligned with left edge of phase space, define first phase of cell based on locations of virtual grates associated with phased chip levels.
507
Move cell left boundary across phase space to next possible location of left cell boundary within phase space without moving virtual grates of phased chip levels.
509
With cell left boundary moved to next location in phase space, define next phase of cell based on locations of virtual grates associated with phase chip levels.
511
Another possible location of left cell boudary within phase space?
Yes
No
Stop

Fig. 5

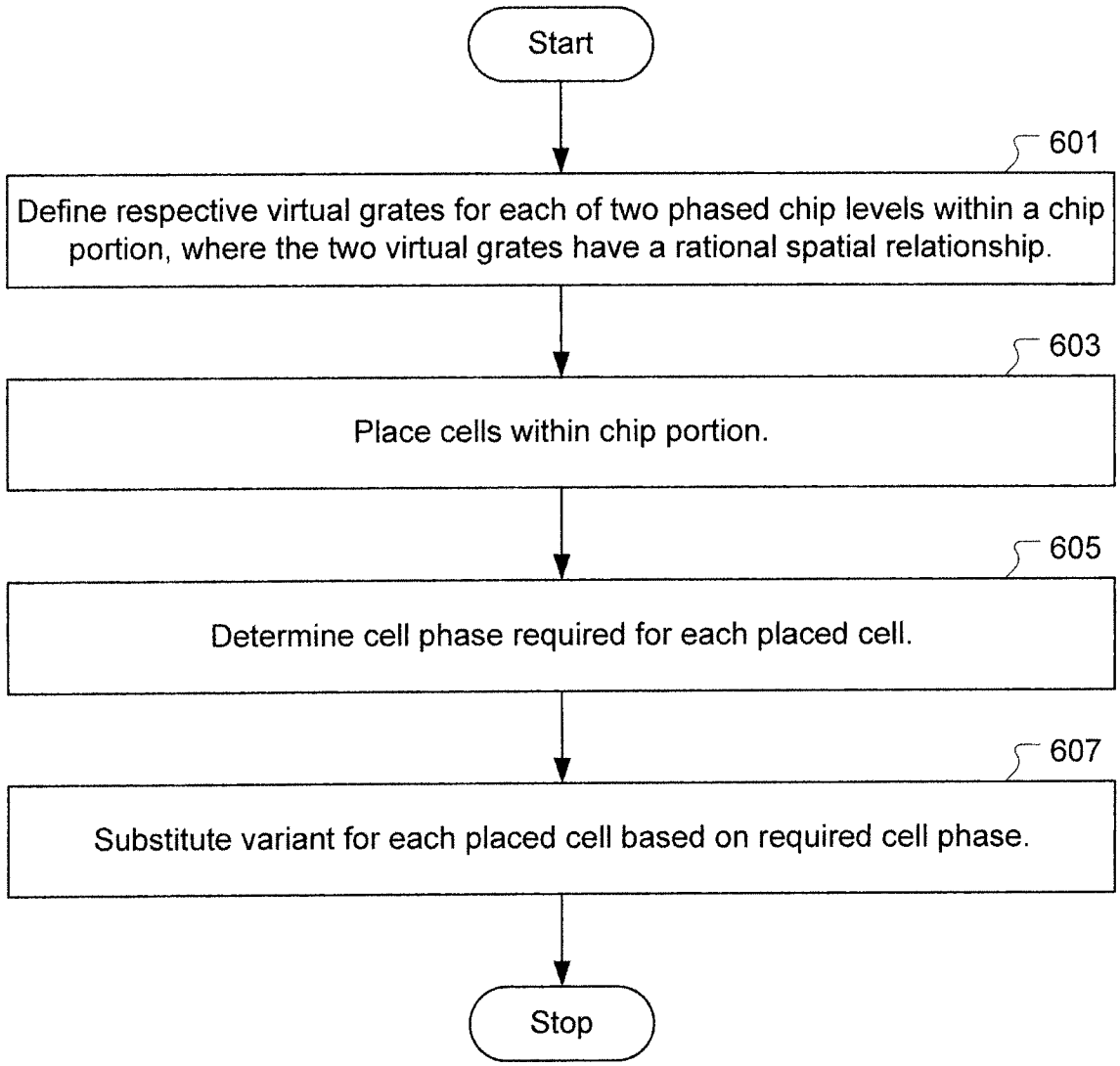

Start
601
Define respective virtual grates for each of two phased chip levels within a chip portion, where the two virtual grates have a rational spatial relationship.
603
Place cells within chip portion.
605
Determine cell phase required for each placed cell.
607
Substitute variant for each placed cell based on required cell phase.
Stop

Fig. 6

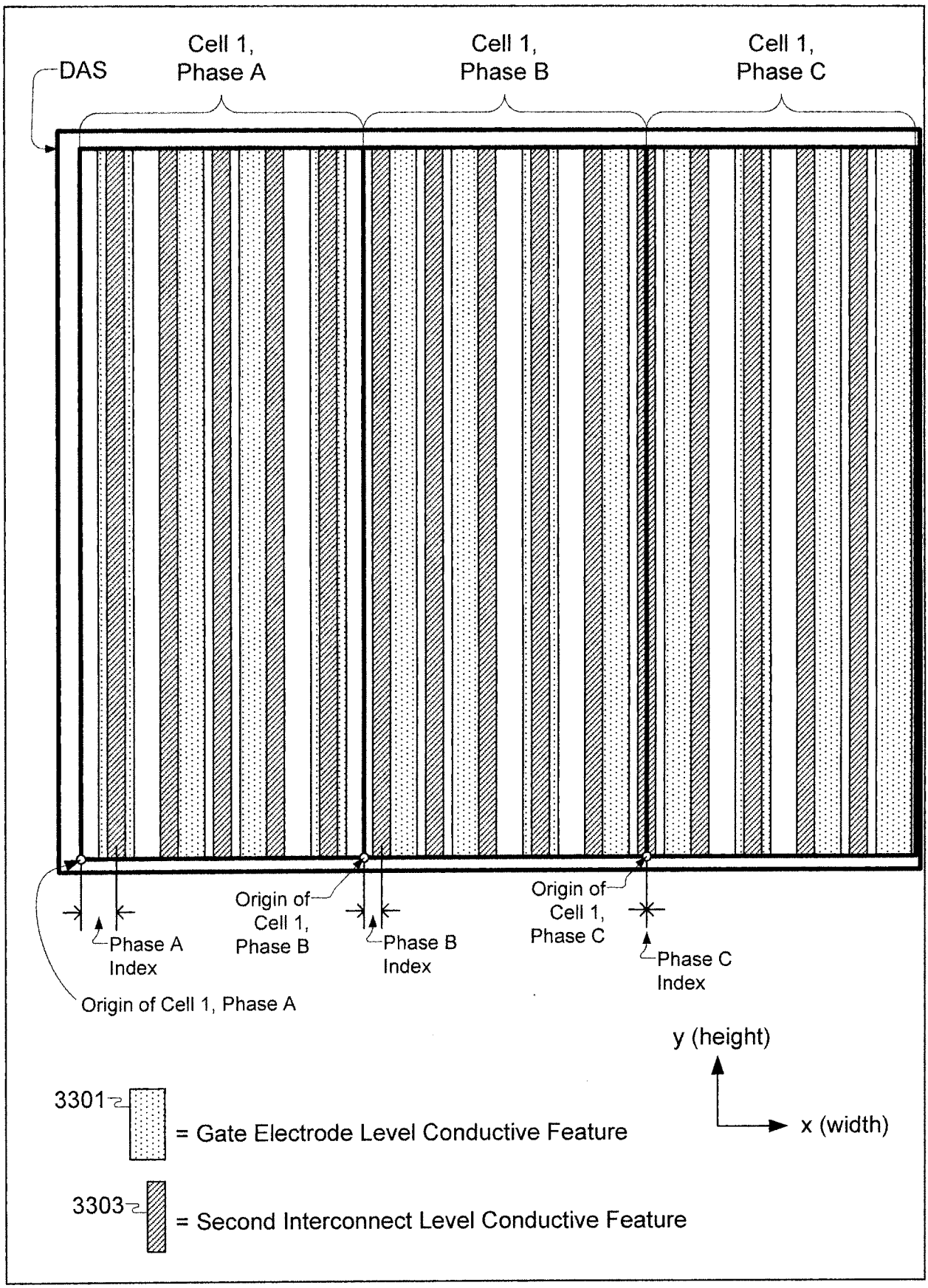

DAS
Cell 1, Phase A
Cell 1, Phase B
Cell 1, Phase C
Origin of Cell 1, Phase A
Phase A Index
Origin of Cell 1, Phase B
Phase B Index
Origin of Cell 1, Phase C
Phase C Index
y (height)
x (width)
3301
= Gate Electrode Level Conductive Feature
3303
= Second Interconnect Level Conductive Feature

Fig. 7

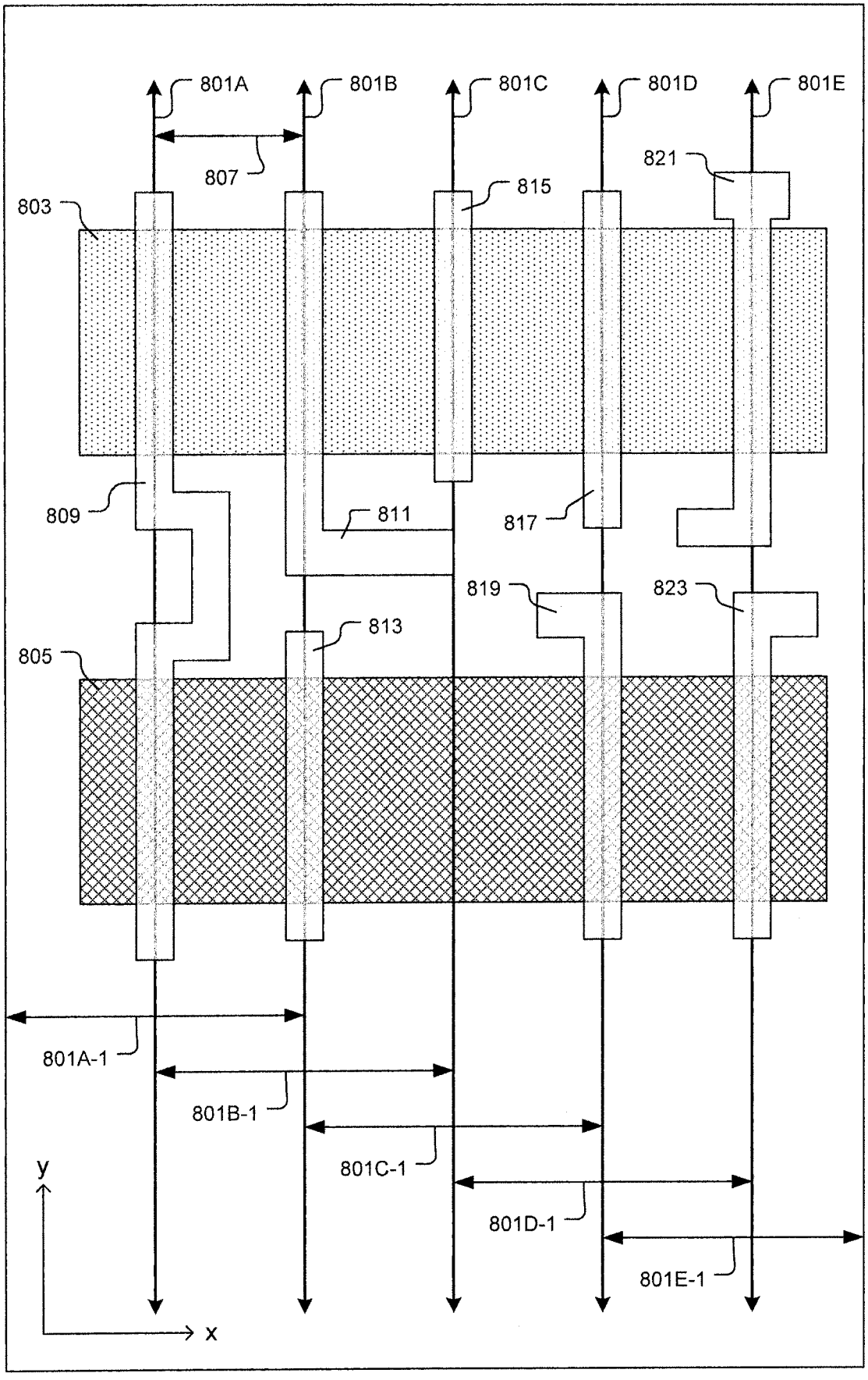

801A
801B
801C
801D
801E
807
821
815
803
809
811
817
819
823
813
805
801A-1
801B-1
801C-1
801D-1
801E-1
y
x

Fig. 8