

LZ77 DECODING CIRCUIT AND WORKING METHOD THEREOF

Abstract

Disclosed is an LZ77 decoding circuit, including, in a direction of a pair data stream, an input/output control circuit, an input buffer, an input preprocessing circuit, an address mapping circuit, a RAM input/output control circuit, a RAM, an output preprocessing circuit and an output buffer. The RAM and the output buffer jointly form a search window, and the RAM input/output control circuit searches for data required by pair from the RAM of the search window. According to a direction of a literal data stream, the LZ77 decoding circuit includes an input buffer, an input preprocessing circuit and an output buffer; and data in the output buffer update the RAM. Input data and output data are respectively reprocessed through an improved search window structure, thereby effectively enhancing a decoding speed of LZ77.

(Fig. 1)