

CLAIMS

What is claimed is:

1. A sidelink information transmission method, applied to a terminal and comprising:

5 mapping sidelink information to target notification information, wherein the sidelink information comprises sidelink hybrid automatic repeat request acknowledgement sidelink HARQ-ACK information corresponding to one or more sidelink transmissions; and

transmitting the target notification information on a target resource, wherein the
10 target resource is a PUCCH or PUSCH;

wherein a mode of mapping the sidelink information to the target notification information comprises: mapping N_3 bits to W second bits according to a preset mode, W is a positive integer, N_3 is an integer greater than 1, and N_3 is greater than W .

15 2. The method according to claim 1, wherein a mode of mapping the sidelink information to the target notification information comprises at least one of the following:

mapping each bit of N_1 first bits to one second bit;

mapping N_2 first bits to M_1 second bits; and

20 determining a first bit sequence associated with a bit sequence formed by N_4 first bits as indication information of second bits corresponding to the N_4 first bits; wherein

the first bits are bits in the sidelink information, the second bits are bits in the target notification information, N_1 , N_2 are all positive integers, N_4 is an integer
25 greater than 1, M_1 is an integer greater than N_2 .

3. The method according to claim 2, wherein the mapping N_2 first bits to M_1 second bits comprises any one of the following:

after mapping the N2 first bits to M2 second bits, inserting a second bit sequence of M3 bits in the M2 second bits to obtain the M1 second bits;

after inserting a third bit sequence of M4 bits in the N2 first bits, mapping combined bits of the N2 first bits and the third bit sequence to the M1 second bits;

5 after repeating each bit of the N2 first bits at least once, performing concatenation to obtain the M1 second bits;

after repeating each bit of the N2 first bits at least once, performing concatenation and inserting at least one fourth bit sequence to obtain the M1 second bits;

10 concatenating at least two target objects to obtain the M1 second bits; and

after concatenating at least two target objects, inserting at least one fourth bit sequence to obtain the M1 second bits; wherein

the target objects are the N2 first bits, and M2, M3, and M4 are all positive integers.

15 4. The method according to claim 3, wherein the mapping N2 first bits to M2 second bits comprises:

mapping each bit of the N2 first bits to one second bit; and

mapping N3 bits of the N2 first bits to W second bits according to a preset mode, wherein N3 and W are positive integers, and N3 is greater than W.

20 5. The method according to claim 3, wherein the mapping combined bits of the N2 first bits and the third bit sequence to the M1 second bits comprises:

mapping each bit of the combined bits to one second bit; and

mapping N3 bits of the combined bits to W second bits according to a preset mode, wherein N3 and W are positive integers, and N3 is greater than W.

25 6. The method according to claims 2, 4, or 5, wherein the preset mode comprises at least one of the following:

in a case that at least two bits comprise at least one bit for indicating a first value, one second bit corresponding to the at least two bits indicates the first value, wherein the at least two bits are bits of the N3 bits;

in a case that the at least two bits all indicate a second value, one second bit corresponding to the at least two bits indicates the second value;

in a case that the at least two bits comprise at least one bit for indicating a second value, one second bit corresponding to the at least two bits indicates the
5 second value;

in a case that the at least two bits all indicate a first value, one second bit corresponding to the at least two bits indicates the first value;

an AND operation is performed on the at least two bits to obtain indication information of the second bit corresponding to the at least two bits;

10 a modulo P operation is performed on a sum of the N3 bits to obtain indication information of the W second bits, wherein P is an integer greater than 1;

an OR operation is performed on the at least two bits to obtain indication information of one second bit corresponding to the at least two bits;

an XOR operation is performed on the at least two bits to obtain indication
15 information of one second bit corresponding to the at least two bits; and

indication information of one second bit corresponding to the at least two first bits is determined based on an interval range to which values corresponding to the at least two bits belong.

7. The method according to claim 2, wherein in a case of mapping each bit of
20 N1 first bits to one second bit, a state indicated by the first bit is the same as a state indicated by the corresponding second bit.

8. The method according to claim 1, further comprising:

receiving scheduling signaling transmitted by a control node, wherein the scheduling signaling is used to indicate a sidelink resource; and

25 performing sidelink transmission on the sidelink resource.

9. The method according to claim 8, wherein the performing sidelink transmission on the sidelink resource comprises one of the following:

performing sidelink retransmission of sidelink data corresponding to first sidelink information, wherein the first sidelink information is sidelink information
30 for which first bits indicate a negative acknowledgement character;

performing sidelink retransmission of sidelink data corresponding to second sidelink information, wherein the second sidelink information is sidelink information corresponding to a negative acknowledgement character indicated by a second bit; and

5 in a case that the control node indicates to retransmit sidelink data, performing sidelink retransmission of the sidelink data that is indicated to be retransmitted.

10. The method according to claim 1, wherein in a case the target resource is provided in plurality, the transmitting the target notification information on a target resource comprises:

10 transmitting the target notification information on the plurality of target resources.

11. A sidelink information transmission method, applied to a control node and comprising:

15 receiving, on a target resource, target notification information transmitted by a terminal, wherein the target notification information is target notification information mapped from sidelink information; and the sidelink information comprises sidelink hybrid automatic repeat request acknowledgement sidelink HARQ-ACK information corresponding to one or more sidelink transmissions, wherein the target resource is a PUCCH or PUSCH;

20 wherein a mode of mapping the sidelink information to the target notification information comprises: mapping $N3$ bits to W second bits according to a preset mode, W is a positive integer, $N3$ is an integer greater than 1, and $N3$ is greater than W .

25 12. The method according to claim 11, wherein a mode of mapping the sidelink information to the target notification information comprises at least one of the following:

mapping each bit of $N1$ first bits to one second bit;
mapping $N2$ first bits to $M1$ second bits; and

determining a first bit sequence associated with a bit sequence formed by N_4 first bits as indication information of second bits corresponding to the N_4 first bits; wherein

the first bits are bits in the sidelink information, the second bits are bits in the target notification information, N_1 , N_2 are all positive integers, N_4 is an integer greater than 1, M_1 is an integer greater than N_2 .

13. The method according to claim 12, wherein the mapping N_2 first bits to M_1 second bits comprises any one of the following:

after mapping the N_2 first bits to M_2 second bits, inserting a second bit sequence of M_3 bits in the M_2 second bits to obtain the M_1 second bits;

after inserting a third bit sequence of M_4 bits in the N_2 first bits, mapping combined bits of the N_2 first bits and the third bit sequence to the M_1 second bits;

after repeating each bit of the N_2 first bits at least once, performing concatenation to obtain the M_1 second bits;

after repeating each bit of the N_2 first bits at least once, performing concatenation and inserting at least one fourth bit sequence to obtain the M_1 second bits;

concatenating at least two target objects to obtain the M_1 second bits; and

after concatenating at least two target objects, inserting at least one fourth bit sequence to obtain the M_1 second bits; wherein

the target objects are the N_2 first bits, and M_2 , M_3 , and M_4 are all positive integers.

14. The method according to claim 13, wherein the mapping N_2 first bits to M_2 second bits comprises:

mapping each bit of the N_2 first bits to one second bit; and

mapping N_3 bits of the N_2 first bits to W second bits according to a preset mode, wherein N_3 and W are positive integers, and N_3 is greater than W .

15. The method according to claim 13, wherein the mapping combined bits of the N_2 first bits and the third bit sequence to the M_1 second bits comprises:

mapping each bit of the combined bits to one second bit; and

mapping N_3 bits of the combined bits to W second bits according to a preset mode, wherein N_3 and W are positive integers, and N_3 is greater than W .

16. The method according to claims 12, 14, or 15, wherein the preset mode comprises at least one of the following:

5 in a case that at least two bits comprise at least one bit for indicating a first value, one second bit corresponding to the at least two bits indicates the first value, wherein the at least two bits are bits of the N_3 bits;

 in a case that the at least two bits all indicate a second value, one second bit corresponding to the at least two bits indicates the second value;

10 in a case that the at least two bits comprise at least one bit for indicating a second value, one second bit corresponding to the at least two bits indicates the second value;

 in a case that the at least two bits all indicate a first value, one second bit corresponding to the at least two bits indicates the first value;

15 an AND operation is performed on the at least two bits to obtain indication information of the second bit corresponding to the at least two bits;

 a modulo P operation is performed on a sum of the N_3 bits to obtain indication information of the W second bits, wherein P is an integer greater than 1;

20 an OR operation is performed on the at least two bits to obtain indication information of one second bit corresponding to the at least two bits;

 an XOR operation is performed on the at least two bits to obtain indication information of one second bit corresponding to the at least two bits; and

25 indication information of one second bit corresponding to the at least two first bits is determined based on an interval range to which values corresponding to the at least two bits belong.

17. The method according to claim 11, further comprising:

 transmitting scheduling signaling to the terminal, wherein the scheduling signaling is used to indicate a sidelink resource.

30 18. A terminal, comprising a memory, a processor, and a program stored in the memory and capable of running on the processor, wherein when the program is

executed by the processor, the steps of the sidelink information transmission method according to any one of claims 1 to 10 are implemented.

19. A control node, comprising a memory, a processor, and a program stored in the memory and capable of running on the processor, wherein when the program is
5 executed by the processor, the steps of the sidelink information transmission method according to any one of claims 11 to 17 are implemented.

20. A computer-readable storage medium, wherein the computer-readable storage medium stores a computer program, and when the computer program is executed by a processor, the steps of the sidelink information transmission method
10 according to any one of claims 1 to 10 are implemented; or when the computer program is executed by a processor, the steps of the sidelink information transmission method according to any one of claims 11 to 17 are implemented.