CLAIMS

WHAT IS CLAIMED:

1. A method, comprising:

forming a hard mask above a semiconductor region, said hard mask having at least one mask feature that determines a lateral size of a semiconductor fin to be formed in said semiconductor region;

performing an implantation process to incorporate a dopant species at and near a surface of said semiconductor region while using said hard mask as an implantation mask;

performing an etch process to form said semiconductor fin in said semiconductor region by using said hard mask as an etch mask after performing said implantation process; and

forming a gate electrode structure above and laterally adjacent to said semiconductor fin.

2. The method of claim 1, wherein forming said hard mask comprises forming said hard mask so as to comprise at least a second mask feature covering a second semiconductor region to be used for forming therein and thereabove a planar transistor.

3. The method of claim 1, wherein forming a gate electrode structure above and laterally adjacent to said semiconductor fin comprises forming a gate mask having a gate opening and filling said gate opening with one or more materials.

4. The method of claim 3, wherein said hard mask is formed prior to forming said gate mask.

5. The method of claim 3, wherein said gate mask is formed prior to forming said hard mask.

6. The method of claim 5, wherein said implantation process is performed in the presence of said gate mask.

7. The method of claim 1, further comprising forming drain and source regions in said semiconductor region after forming said gate electrode structure.

8. The method of claim 7, wherein forming said drain and source regions comprises concurrently forming second drain and source regions in a second semiconductor region of a planar transistor.

9. The method of claim 7, wherein performing said implantation process comprises to incorporate a dopant species at and near a surface of said semiconductor region comprises incorporating said dopant species as a counter-doping species compared to a drain and source dopant species.

10. The method of claim 1, wherein forming said gate electrode structure comprises providing a placeholder structure after forming said hard mask, removing a placeholder material of said placeholder structure and providing gate materials after performing said implantation process and said etch process.

11. A method of forming a semiconductor device, the method comprising:

forming first drain and source regions of a multiple gate transistor in a first semiconductor region and second drain and source regions of a planar transistor in a second semiconductor region, said multiple gate transistor comprising a semiconductor fin connecting to said first drain and source regions; and

separately adjusting a threshold voltage of said multiple gate transistor by providing a counter-doping species in said semiconductor fin so as to have a concentration maximum at upper corners of said semiconductor fin.

12. The method of claim 11, wherein providing said counter-doping species in said semiconductor fin comprises forming a hard mask above said first semiconductor region and said second semiconductor region so as to cover at least a channel region of said planar transistor and determine the size and position of said semiconductor fin of said multiple gate transistor, and performing an implantation process by using said hard mask as an implantation mask.

13. The method of claim 12, further comprising using said hard mask as an etch mask after performing said implantation process so as to form said semiconductor fin.

14. The method of claim 11, further comprising masking a second multiple gate transistor when adjusting a threshold voltage of said multiple gate transistor.

15. The method of claim 14, further comprising adjusting a second threshold voltage of said second multiple gate transistor while masking said multiple gate transistor.

16. The method of claim 15, wherein said multiple gate transistor and said second multiple gate transistor are transistors of inverse conductivity type.

17. The method of claim 12, wherein said implantation process is performed by using an implantation energy of approximately 0.1-2 keV.

18. A semiconductor device, comprising:

a semiconductor region comprising a drain region and a source region;

a channel region formed by at least one semiconductor fin formed in said semiconductor region so as to connect with a first end portion to said drain region and to connect with a second end portion to said source region, said semiconductor fin comprising a counter-doping species having a concentration maximum locally at and along upper corners of said semiconductor fin; and

a gate electrode structure formed above and laterally adjacent to said at least one semiconductor fin.

19. The semiconductor device of claim 18, further comprising a second semiconductor region comprising second drain and source regions and a planar second channel region that extends between said second drain region and said second

source region, wherein said drain and source regions and said second drain and source regions have substantially the same dopant profile.

20. The semiconductor device of claim 18, wherein a length of said channel region and said second channel region is approximately 70 nm or less.

CLAIMS

1. A method, comprising:

forming a hard mask above a semiconductor region, said hard mask having at least one mask feature that determines a lateral size of a semiconductor fin to be formed in said semiconductor region;

performing an implantation process to incorporate a dopant species at and near an upper surface of said semiconductor region while using said hard mask as an implantation mask;

after performing said implantation process, performing an etch process to form said semiconductor fin in said semiconductor region by using said hard mask as an etch mask; and

forming a gate electrode structure above and laterally adjacent to said semiconductor fin.

2. The method of claim 1, wherein forming said hard mask comprises forming said hard mask so as to comprise at least a second mask feature covering a second semiconductor region to be used for forming therein and thereabove a planar transistor.

3. The method of claim 1, wherein forming a gate electrode structure above and laterally adjacent to said semiconductor fin comprises forming a gate mask having a gate opening and filling said gate opening with one or more materials.

4. The method of claim 3, wherein said hard mask is formed prior to forming said gate mask.

5. The method of claim 3, wherein said gate mask is formed prior to forming said hard mask.

6. The method of claim 5, wherein said implantation process is performed in the presence of said gate mask.

7. The method of claim 1, further comprising forming drain and source regions in said semiconductor region after forming said gate electrode structure.

8. The method of claim 7, wherein forming said drain and source regions comprises concurrently forming second drain and source regions in a second semiconductor region of a planar transistor.

9. The method of claim 7, wherein performing said implantation process comprises to incorporate said dopant species at and near said upper surface of said semiconductor region comprises incorporating said dopant species as a counter-doping species compared to a drain and source dopant species.

10. The method of claim 1, wherein forming said gate electrode structure comprises providing a placeholder structure after forming said hard mask, removing a placeholder material of said placeholder structure and providing gate materials after performing said implantation process and said etch process.

11. A method of forming a semiconductor device, the method comprising:

forming first drain and source regions of a multiple gate transistor in a first semiconductor region and second drain and source regions of a planar transistor in a second semiconductor region, said multiple gate transistor comprising a semiconductor fin connecting to said first drain and source regions; and

separately adjusting a threshold voltage of said multiple gate transistor by providing a counter-doping species in said semiconductor fin so as to have a concentration maximum in upper corner regions of said semiconductor fin, wherein said upper corner regions are spaced apart across a width of said semiconductor fin and a concentration of said provided counter-doping species in a region of said semiconductor fin between said upper corner regions is less than said concentration maximum.

12. The method of claim 11, wherein providing said counter-doping species in said semiconductor fin comprises forming a hard mask above said first semiconductor region and said second semiconductor region so as to cover at least a channel region of said planar transistor and determine the size and position of said semiconductor fin of said multiple gate transistor, and performing an implantation process by using said hard mask as an implantation mask.

13. The method of claim 12, further comprising using said hard mask as an etch mask after performing said implantation process so as to form said semiconductor fin.

14. The method of claim 12, wherein said implantation process is performed by using an implantation energy of approximately 0.1-2 keV.

15. The method of claim 11, further comprising masking a second multiple gate transistor when adjusting a threshold voltage of said multiple gate transistor.

16. The method of claim 15, further comprising adjusting a second threshold voltage of said second multiple gate transistor while masking said multiple gate transistor.

17. The method of claim 16, wherein said multiple gate transistor and said second multiple gate transistor are transistors of inverse conductivity type.

18. The method of claim 11, wherein said upper corner regions comprising said provided counter-doping species extend approximately 5 nm or less across an upper surface of said semiconductor fin from upper corners of said semiconductor fin.

19. The method of claim 11 wherein said upper corner regions comprising said provided counter-doping species extend approximately 5 nm or less down a sidewall surface of said semiconductor fin from upper corners of said semiconductor fin.

20. The method of claim 11, wherein said provided counter-doping species is absent from at least a portion of said region of said semiconductor fin between said upper corner regions.

21. A semiconductor device formed in accordance with the method of any one of the preceding claims.