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(71) Applicant *(for all designated States except US)*: **S.O.I. TEC SILICON ON INSULATOR TECHNOLOGIES** [FR/FR]; Chemin des Franques, Parc Technologique des Fontaines, F-38190 Bernin (FR).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **BROEKAART, Marcel** [NL/FR]; Clos des Gentons, F-38570 Theys (FR). **MIGETTE, Marion** [FR/FR]; 3, avenue Jeanne d'Arc, F-38100 Grenoble (FR). **MOLINARI, Sébastien** [FR/FR]; 2J, Chemin de Fontaine, F-38360 Sassenage (FR). **NEYRET, Eric** [FR/FR]; 7 rue F. Gerin, F-38360 Sassenage (FR).

(74) Agents: **DESORMIERE, Pierre-Louis** et al.; Cabinet Beau De Lomenie, 158 Rue de l'Université, F-75340 Paris Cedex 07 (FR).

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(54) **Title**: A MIXED TRIMMING METHOD

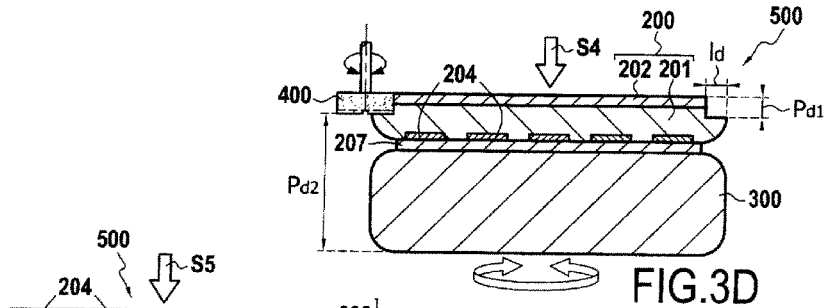


FIG.3D

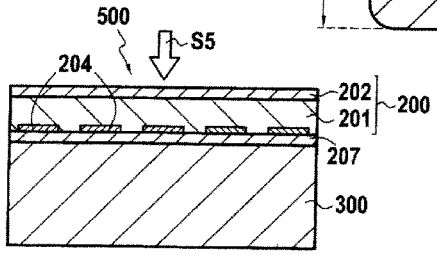


FIG.3E

(57) **Abstract**: The invention relates to a method of trimming a structure (500) comprising a first wafer (200) bonded to a second wafer (300), the first wafer (200) having a chamfered edge. The method comprises a first step (S4) for trimming the edge of the first wafer (200) carried out by mechanical machining over a predetermined depth (Pd_1) in the first wafer. This first trimming step is followed by a second step (S5) for non-mechanical trimming over at least the remaining thickness of the first wafer.

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