

CIRCUIT OF UNIFORM TRANSISTORS ON SeOI WITH BURIED BACK
CONTROL GATE BENEATH THE INSULATING FILM

FIELD OF THE INVENTION

The field of the invention is that of microelectronics.

The invention relates more precisely to a semiconductor device made
5 on an SeOI (Semiconductor On Insulator) substrate based on components
with uniformized patterns.

BACKGROUND OF THE INVENTION

10 A general tendency in the field of application of the invention is to seek
to simplify the lithography in order to solve the distortion and deformation
problems in lithographic structures that have to be transferred onto a wafer.

The prior art thus recommends avoiding as far as possible corners in
the same lithographic plane. However, the use of different widths of
15 transistors for constructing circuits is a common practice.

The channel length of an MOSFET transistor is at the present time
typically around 30 nm, whereas its width W is typically much greater. Now,
the width determines the current intensity in the transistor for given source,
drain and gate voltages.

20 It is usually possible to design an electronic circuit in which the various
transistors have different widths. However, in practice it is difficult to obtain
different widths with any precision because of the resolution limit of the
lithography. In fact, although it is relatively easy to produce long stripstrips by
lithography, short strips of very controlled dimensions are particularly difficult
25 to obtain.

Document US 2008/0251848 teaches a fabrication process aimed at
obviating inhomogeneities in performance between the various transistors of
a circuit. To do so, this document proposes to make the influence of the
environment on the various transistors uniform. More precisely, the above
30 document provides for an array of FET transistors to be arranged in the form
of long strips. The drain and source regions of any one strip then have the

same dimensions, being spaced apart by gate regions of fixed dimensions.

It will therefore be understood that the resolution limit of the lithography tends to dictate the use of such long strips of transistors having identical dimensions.

5 However, the flexibility in designing electronic circuits is then lost since it is no longer possible to vary the geometric width of the various transistors so as to modulate their performance.

BRIEF DESCRIPTION OF THE INVENTION

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In this context, objectives of the invention are: to solve the problem posed by the variability inherent in lithographic pattern transfer (random variability due to the structuring of the lines and line/space/line variability); to save space, by avoiding the need for shallow trench isolation (STI) and by
15 tightening up the structures (active zones, gate lines, interconnect lines, etc.); and to simplify the lithography by proposing structures to be transferred that are more regular and denser.

For this purpose, the invention provides, according to a first aspect, a semiconductor device formed on a semiconductor-on-insulator substrate
20 comprising a thin film of semiconductor material separated from a base substrate by an insulating film, the device comprising an array of patterns each formed from at least one field-effect transistor, each transistor having, in the thin film, a source region, a drain region and a channel region which is delimited by the source and drain regions, and furthermore comprising a front
25 control gate region formed above the channel region, the patterns being arranged in the form of rows, the source and drain regions of any one row having the same dimensions and being spaced apart by front control gate regions of fixed dimensions, characterized in that at least one transistor of a pattern has a back control gate region formed in the base substrate beneath
30 the channel region, the back gate region being capable of being biased in order to shift the threshold voltage of the transistor to simulate a modification

in the channel width of the transistor or to force the transistor to remain off or on whatever the voltage applied on its front control gate.

Certain preferred, but non-limiting, aspects of this device are the following:

- 5 – some of the patterns in a row are formed on one and the same active zone of the thin film of the semiconductor substrate and in which an isolation region delimits the adjacent patterns, the isolation region comprising a front isolation gate formed above the active zone and a back isolation gate formed in the base substrate beneath the active zone;
- 10 – a back isolation line connects the back isolation gates of each of the isolation regions of any one row;
 - the back isolation line is common to several rows;
 - the back isolation gate has a conductivity of opposite type to that of the active zone;
- 15 – a back gate line connects the back gate region(s) of one or a plurality of transistors;
 - a back gate line connects the back gate region(s) to ground or to a nominal supply voltage;
 - a back gate line connects the back gate region(s) to a an analogue and
 - 20 adjustable potential;
 - the back gate region is isolated from the base substrate by a well of opposite conductivity;
 - the back gate region has a conductivity of the same type as that of the transistor channel; and
- 25 – the back gate region has a conductivity of opposite type to that of the transistor channel.

According to another aspect, the invention relates to a method of driving a device according to the first aspect of the invention, in which the back control gate region is biased positively or negatively in order to shift the

30 threshold voltage of the transistor, and especially a driving method in which a the back control gate region is biased by an analogue and adjustable

potential.

According to another aspect, the invention relates to a method of driving a device according to the first aspect of the invention, in which the shift of the threshold voltage is controlled to cause the transistor to remain off or on whatever the voltage applied to its front control gate. The shift of the threshold voltage can in particular be programmed by means of memory cells that store and deliver predetermined voltages to the back control gates.

According to another aspect, the invention relates to a re-programmable circuit comprising a device according to the first aspect of the invention interleaved with rows of memory cells that store and deliver predetermined voltages to the back control gate regions.

BRIEF DESCRIPTION OF THE DRAWINGS

Other aspects, objects and advantages of the present invention will become more apparent on reading the following detailed description of preferred embodiments thereof, given by way of non-limiting example and with reference to the appended drawings in which:

- Figure 1 shows a circuit according to prior art;
- Figure 2 illustrates the way the threshold voltage of a transistor is controlled by biasing a back control gate;
- Figures 3 to 7 show the active zone beneath the insulating film of a circuit identical to that of Figure 1 according to various embodiments of the invention;
- Figure 8 is a sectional view of a portion of a row of transistors of the circuit shown in Figure 7;
- Figure 9 is an example of logic circuit that is reconfigurable to cover all 2-input Boolean functions by means of appropriate voltages applied of the back gates of the various transistors;
- Figure 10 is the truth table of the reconfigurable logic circuit of figure 9;

- Figure 11 shows a possible arrangement of logic cells and of memory cells used to store the programming of the logic cells and to deliver the appropriate voltages to the back gates of the transistors of the logic cells.

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DETAILED DESCRIPTION OF THE INVENTION

Figure 1 shows a CMOS electronic circuit according to the prior art, as taught by document US 2008/0251848.

10 This circuit comprises an array of patterns each formed from at least one field-effect transistor, the patterns being arranged in the form of rows, the source and drain regions of each transistor of any one row having the same dimensions and being spaced apart by front control gate regions WL1-WL7 of fixed dimensions.

15 Thus, during the lithography steps only wide strips (horizontal rows and vertical front control gate regions) are formed. The channel width of the various transistors is then uniform, defined by the section between two perpendicular strips.

It should be noted that there are no STI-type isolation trenches between adjacent transistors of any one strip. However, such isolation trenches are
20 indeed present along the strips so as to isolate them from one another.

The circuit comprises, from left to right in Figure 1, the following patterns: a logic gate NOR2, three inverters INV₁, INV₂ and INV₃ and a logic gate NAND2.

25 More precisely, the circuit comprises, in this example, nine metal₂ busses, the p-FET transistors being arranged along busses 2 and 3 whereas the n-FET transistors are arranged along busses 7 and 8. Busses 4 to 6 are used to make the input/output connection to these patterns and to connect these various patterns together. It is clear that other combinations are possible, with reasonably 8 to 12 metal₂ busses.

30 Metal₁ supply lines BL_{P1}, BL_{P2}, BL_{N1}, BL_{N2} serve to fix the potential of some of the drain regions of the transistors.

Thus, the drain of the first p-FET transistor of the logic gate NOR2 and the drain of the p-FET transistors of the inverters INV_1 and INV_2 are connected to the line BL_{P1} , whereas the drain of the p-FET transistor of the inverter INV_3 and the drain of the p-FET transistors of the logic gate NAND2
 5 are connected to the line BL_{P2} .

The drain of the n-FET transistors of the logic gate NOR2 and the drain of the n-FET transistors of the inverters INV_1 and INV_2 are connected to the line BL_{N1} , whereas the drain of the n-FET transistor of the inverter INV_3 and the drain of the first n-FET transistor of the logic gate NAND2 are connected
 10 to the line BL_{N2} .

The lines BL_{P1} and BL_{P2} are used typically to deliver a nominal supply voltage V_{DD} , whereas the lines BL_{N1} and BL_{N2} are typically connected to ground GND.

The patterns along a row are formed on one and the same active zone
 15 of the substrate, and therefore isolation regions are provided between adjacent patterns. These isolation regions, each having a front isolation gate formed above the active zone, bear, in what follows, the references IP_1 - IP_6 for the isolation regions linked to the p-FET transistors and the references IN_1 - IN_6 for the isolation regions linked to the n-FET transistors

20 The front isolation gates of the isolation regions are biased by means of isolation gate supply lines Bl_P and Bl_N for the isolation regions between p-FET patterns and between n-FET patterns respectively. These lines Bl_P and Bl_N are typically formed from a polycrystalline semiconductor material (typically polycrystalline silicon).

25 In general, the invention proposes to transfer circuits with a uniformized environment of the type shown in Figure 1 onto an SeOI substrate (comprising a thin film of semiconductor material separated from a base substrate by an insulating film). In this context, the invention proposes to place a back control gate in the base substrate facing the channel of at least
 30 one transistor. By biasing the back control gate of the transistor positively or negatively (typically by $+v_{dd}$ or $-v_{dd}$), the properties of the transistor may be

individually modified. In particular, the threshold voltage of the transistor may be shifted. Then, modifying the threshold voltage is equivalent to modifying the physical width of the channel.

Thus, in the context of the invention, the physical width of the channel is defined once and for all and for all the transistors. However, it proves possible to modify, individually for each transistor, the apparent (effective) width of its channel by choosing the way in which the back control gate is driven. Since the voltage applied to the back control gate may be modified, the invention thus offers the advantage of modifying the effective channel width dynamically.

A transistor in which the channel is of n-type conductivity and a back control gate is of p-type conductivity (in the context of the present description, the back control gate is then said to have a work function) has a very high threshold voltage. This threshold voltage may then be reduced by applying a positive voltage to the back control gate.

A transistor in which the channel is of n-type conductivity and a back control gate is of n-type conductivity (in the context of the present description, the back control gate is then said to have no work function) has a nominal threshold voltage that can be reduced by applying a positive voltage to the back control gate.

This variation in the threshold voltage of the transistor via the back control gate may be formulated as $V_{th} = V_{t0} - \alpha V_{BG}$, where V_{th} represents the threshold voltage of the transistor, V_{BG} represents the voltage applied to the back control gate, V_{t0} represents the nominal threshold voltage (which may be shifted by the work function depending on whether a back control gate of n-type or p-type is used) and α represents a factor associated with the geometry of the transistor.

As presented in the thesis "Architectures innovantes de mémoire non-volatile embarquée sur film mince de silicium [*Innovative non-volatile memory architectures on thin silicon films*]" defended by Germain Bossu in June 2009 at the Provence, Aix-Marseille University I, the factor α may in

particular be approximated as $\alpha = 3t_{ox1}/(t_{Si}+3t_{ox2})$, where t_{ox1} denotes the thickness of the dielectric gate film separating the front control gate from the channel (typically 1-2nm), t_{ox2} denotes the thickness of the insulating film separating the back control gate from the channel (typically 5-20nm for SeOI substrates) and t_{Si} denotes the thickness of the thin film.

It will therefore be understood that the doping type of the back control gate associated with a transistor may or may not shift the nominal threshold voltage and that by biasing the back control gate it is possible to adjust the threshold voltage.

It is thus possible to benefit from an increase in the conduction current I_{ON} in the on-state of the transistor (by reducing the threshold voltage) and from a reduction in the small leakage current I_{OFF} in the off-state of the transistor (by increasing the threshold voltage).

A contribution may also be made to the isolating function of an isolation region separating the adjacent patterns along a row by reducing the leakage current therein.

The purpose of Figure 2 is to illustrate the way in which the threshold voltage of a transistor produced on an SeOI substrate is controlled by biasing a back control gate made in the base substrate, beneath the insulating film, facing the channel of the transistor.

In this Figure 2, the central curve C_N represents the nominal characteristic $\log(I_D(V_G))$ (for a transistor with no back control gate).

The upper curve C_{VT-} represents the nominal characteristic $\log(I_D(V_G))$ under the effect of a back control gate driven with a voltage below the nominal supply voltage V_{DD} of the circuit. This upper curve illustrates the increase in the threshold voltage and the reduction in the currents I_{ON} and I_{OFF} .

The lower curve C_{VT+} represents the nominal characteristic $\log(I_D(V_G))$ under the effect of a back control gate driven with a nominal supply voltage V_{DD} . This lower curve illustrates the reduction in the threshold voltage and the increase in the currents I_{ON} and I_{OFF} .

It will thus be understood that, by varying the back control gate bias, it is possible to cover the entire area between the lower curve C_{VT-} and the upper curve C_{VT+} , thus modulating the threshold voltage of the transistor and its characteristic currents I_{ON} and I_{OFF} .

- 5 The following equation links in particular the current I_D in the channel to the channel width W and to the threshold voltage V_{th} :

$$I_D = \frac{\mu_n C_{ox} W}{2L} (V_{GS} - V_{th})^2 (1 + \lambda V_{DS}).$$

Firstly consider gate and drain voltages of 0.9 V ($V_{GS} = V_{DS} = 0.9$ V), with $\lambda = 0.05$ and a threshold voltage $V_{th} = 0.3$ V.

- 10 By modifying the threshold voltage of the transistor so that it takes a value between 0.05 V and 0.6 V, it is then possible to simulate a modification in the physical width of the channel. Theoretically, the effective width of the transistor channel is actually between 0.25 and 2.01 times the physical width W_0 of the channel.

- 15 Consider, in another example, lower gate and drain voltages, namely 0.7 V, and again modifying the threshold voltage of the transistor so that it takes a value between 0.05 V and 0.6 V, the effective width of the channel then being theoretically between 0.06 and 2.64 times the physical width of the channel

- 20 The invention thus allows a reduction/increase of the effective channel width which is even more important that the supply voltages are low.

- It should be noted in this regard that the tendency in the technical field of the invention is for future generations of electronic components to use ever lower supply voltages. The invention thus proves itself to be a priori even
25 more interesting for the future generations.

Figures 3 to 7 show the active zone beneath the insulating film of a circuit identical to that in Figure 1 according to various embodiments of the invention.

In Figure 3:

- 30 - p-doped back control gate regions are associated with the isolation

regions I_{P1} - I_{P6} , with the two, p-FET and n-FET, transistors of the inverter INV_2 and with the two n-FET transistors of the logic gate NAND2; and

- n-doped back control gate regions are associated with the isolation regions I_{N1} - I_{N6} and with the two, p-FET and n-FET, transistors of the inverter INV_3 .

A back gate line BG_P and a back gate line BG_N serve for collectively connecting the p-doped back gate regions and the n-doped back gate regions, respectively, to the same potential.

The line BG_P associated with the p-doped back gates may thus be in a high state (being typically connected to the potential V_{DD}), whereas the line BG_N associated with the n-doped back gates may be in a low state (being typically connected to ground GND).

In such a manner, the isolation regions experience higher threshold voltages and consequently lower leakage currents I_{OFF} , thus helping to maintain better isolation between adjacent patterns along any one row.

As regards the inverter INV_2 , the back control gate of the p-FET transistor and that of the n-FET transistor are in the high state V_{DD} . The conduction current I_{ON} of the n-FET transistor is increased, while the conduction current of the p-FET transistor is reduced. The inverter INV_2 thus has a low p-FET and a high n-FET.

As regards the inverter INV_3 , this has a high p-FET and a low n-FET (the back control gate of the p-FET transistor and that of the n-FET transistor are in the low state GND).

As regards the logic gate NAND2, the p-FET transistors do not have a back control gate. These p-FET transistors therefore operate in the nominal manner. n-FET transistors do have back control gates in the high state. These n-FET transistors have a higher conduction current.

Figure 4 shows another embodiment in which four different voltage levels are used to offer more flexibility. In Figure 4:

- p-doped back control gate regions collectively connected to a back gate line BG_{PH} in the high state are associated with the isolation regions I_{P1} - I_{P6}

and with the p-FET transistor of the inverter INV_2 ;

- a p-doped back control gate region connected to a back gate line BG_{PL} in a low state is associated with the p-FET transistor of the inverter INV_3 ;
- n-doped back control gate regions collectively connected to a back gate line BG_{NL} in a low state are associated with the isolation regions $I_{N1}-I_{N6}$ and with the n-FET transistor of the inverter INV_3 ; and
- an n-doped back control gate region connected to a back gate line BG_{NH} in a high state is associated with the n-FET transistor of the inverter INV_2 .

Just like the example in Figure 3, the leakage current of the isolation regions is thus reduced.

The inverter INV_2 has a low p-FET transistor (p-doped back control gate in a high state) and a high n-FET transistor (n-doped back control gate in a high state).

The inverter INV_3 has a high p-FET transistor (p-doped back control gate in a low state) and a low n-FET transistor (n-doped back control gate in a low state).

Figure 5 shows another embodiment in which a back control gate associated with a transistor is connected to a back gate line which is specific thereto. It will be understood that such an embodiment enables the potential applied to the back gate line dedicated to a single transistor to be modulated. In this Figure 5:

- p-doped back control gate regions collectively connected to a back gate line BG_{PH} in a high state are associated with the isolation regions $I_{P1}-I_{P6}$ and with the p-FET transistor of the inverter INV_2 ;
- a p-doped back control gate region connected to an individual back gate line BG_{PA} , the voltage of which can be adjusted, is associated with the p-FET transistor of the inverter INV_3 ;
- n-doped back control gate regions collectively connected to a back gate line BG_{NL} in a low state are associated with the isolation regions $I_{N1}-I_{N6}$ and with the n-FET transistor; and

- an n-doped back control gate region connected to an individual back gate line BG_{NA} , the voltage of which can be adjusted, is associated with the n-FET transistor of the inverter INV_2 .

Thus, the inverter INV_2 has a low p-FET transistor (p-doped back control gate in a high state) and an adjustable n-FET transistor (individual n-doped back control gate addressed via the line BG_{NA} , the potential of which can be adjusted).

As for the inverter INV_3 , this has a low n-FET transistor (n-doped back control gate in a low state) and an adjustable p-FET transistor (individual p-doped back control gate addressed via the line BG_{PA} , the potential of which can be adjusted).

Figure 6 shows an alternative embodiment of the example of Figure 4. In this Figure 6:

- p-doped back control gate regions collectively connected to a back gate line BG_{PH} in a high state are associated with the isolation regions I_{P1} - I_{P6} ;
- p-doped back control gate regions collectively connected to a back gate line BG_{PL} in a low state are associated with the p-FET transistor of the inverter INV_2 and with the p-FET transistor of the inverter INV_3 ;
- n-doped back control gate regions collectively connected to a back gate line BG_{NH} in a high state are associated with the isolation regions I_{N1} - I_{N6} and with the n-FET transistor of the inverter INV_3 ; and
- an n-doped back control gate region connected to a back gate line BG_{NL} in a low state is associated with the n-FET transistor of the inverter INV_2 .

Thus, the inverter INV_2 has a high p-FET transistor (p-doped back control gate in a low state) and a low n-FET transistor (n-doped back control gate in a low state).

The inverter INV_3 has a high p-FET transistor (p-doped back control gate in a low state) and a high n-FET transistor (n-doped back control gate in a high state).

Figure 7 shows a preferred embodiment in which the isolation regions are associated with back control gate regions having a conductivity of

opposite type. The leakage currents in these isolation regions are thus further reduced.

More precisely, in this Figure 7:

- n-doped back control gate regions collectively connected to a back gate line BG_{NH} in a high state are associated with the isolation regions I_{P1} - I_{P6} , with one of the n-FET transistors of the logic gate NOR_2 and with the p-FET transistor of the inverter INV_2 ;
- a p-doped back control gate region connected to an individual back gate line BG_{PA1} , the voltage of which can be adjusted (to any intermediate value chosen by the skilled person), is associated with the p-FET transistor of the inverter INV_3 ;
- p-doped back control gate regions collectively connected to a back gate line BG_{PL} in a low state are associated with the isolation regions I_{N1} - I_{N6} , with one of the p-FET transistors of the logic gate $NAND2$ and with the n-FET transistor of the inverter INV_3 ;
- a p-doped back control gate region connected to an individual back gate line BG_{PA2} , the voltage of which can be adjusted (to any intermediate value chosen by the skilled person), is associated with the n-FET transistor of the inverter INV_1 ;
- an n-doped back control gate region connected to an individual back gate line BG_{NA1} , the voltage of which can be adjusted (to any intermediate value chosen by the skilled person), is associated with the n-FET transistor of the inverter INV_2 ; and
- an n-doped back control gate region connected to an individual back gate line BG_{NA2} , the voltage of which can be adjusted (to any intermediate value chosen by the skilled person), is associated with the p-FET transistor of the logic gate $NAND2$ which is not connected to BG_{PL} .

Thus, the isolation regions I_{P1} - I_{P6} have a p-channel with a p-type back control gate in the high state (typically at V_{DD}). These regions have a maximum threshold voltage and consequently a minimum leakage current.

The isolation regions I_{N1} - I_{N6} themselves have an n-channel with an

n-type back control gate in the low state (typically at GND). These regions have a maximum threshold voltage and consequently a minimum leakage current.

One of the n-FET transistors of the logic gate NOR_2 also has an n-channel, but with an n-type back control gate in the high state. It has a minimum threshold voltage and consequently maximum performance characteristics (in terms of conduction current I_{ON}).

The n-FET transistor of the inverter INV_1 has an n-channel with a p-type back control gate, the voltage of which can be adjusted. Thus, this transistor has performance characteristics lying between the minimum performance characteristics and the mean performance characteristics depending on the voltage applied to the individual line BGP_{A2} .

The p-FET transistor of the inverter INV_1 does not have a back control gate, and therefore it operates in a nominal manner.

The n-FET transistor of the inverter INV_2 has an n-channel with an n-type back control gate, the voltage of which can be adjusted. Thus, this transistor has performance characteristics lying between the mean performance characteristics and the maximum performance characteristics depending on the voltage applied to the individual line BGP_{NA1} .

The p-FET transistor of the inverter INV_3 has a p-channel with a p-type back control gate, the voltage of which can be adjusted. Thus, this transistor has performance characteristics lying between the minimum performance characteristics and the mean performance characteristics depending on the voltage applied to the individual line BGP_{PA1} .

The p-FET transistor of the logic gate $NAND2$, which does have an n-type back control gate, the voltage of which can be adjusted via the individual line BG_{NA2} , has performance characteristics lying between the mean performance characteristics and the maximum performance characteristics.

The p-FET transistor of the logic gate $NAND2$, which has a p-type back control gate, the voltage of which is in the low state via the line BG_{PL} , has itself a minimum threshold voltage and maximum performance

characteristics.

The upper part of Figure 8 shows two metal2 lines, 7 and 8, along which the FET transistors of the circuit shown in Figure 7 are placed. The lower part of Figure 8 shows a sectional view of a portion of metal2 line 8 comprising the isolation regions I_{N1} - I_{N3} and the n-FET transistors T_1 - T_4 of the NOR2 (T_1 and T_2), INV₁ (T_3) and INV₂ (T_4) patterns. In this sectional view, the insulating film bears the reference BOX.

In Figure 8, the transistor channels are fully depleted, the source and drain regions being in contact with the insulating film.

However, the invention also applies to the partially depleted technology in which the source and drain regions do not extend into the entire thin film. It should be noted in this case that the back control gate is overall less effective as it is further away from the channel region between the source and drain regions.

As discussed above, the isolation regions I_{N1} - I_{N3} have an n-channel and each region has a p⁺-type back control gate G_{P1} - G_{P3} (in the low state via the line BG_{PL}).

One of the nFET transistors, T_1 , of the logic gate NOR2 has an n⁺-type back control gate G_{N1} (in the high state via the line BG_{NH}), whereas the other nFET transistor, T_2 , of the logic gate NOR2 does not have a back control gate.

The nFET transistor T_3 of the inverter INV₁ has a p⁺-type back control gate G_{P4} (which can be adjusted via the individual line BG_{PA2}).

The nFET transistor T_4 of the inverter INV₂ has an n⁺-type back control gate G_{N2} (which can be adjusted via the individual line BG_{NA1}).

As shown in Figure 8, the associated back control gate is localized so as to extend only opposite the transistor channel. For example, the back control gate is formed by implanting dopants beneath the insulating film BOX.

The back control gate is isolated from the base substrate by a well C_{N1} , C_{P1} , C_{N2} , C_{P2} of opposite conductivity to that of the control gate (n⁻-type well C_{N1} , C_{N2} for a p⁺-type back control gate G_{P1} , G_{P2} , G_{P3} , G_{P4} ; p⁻-type well C_{P1} ,

C_{P2} for an n^+ -type back control gate G_{N1} , G_{N2}).

The well voltage is chosen so that the diode created by the electrical node between the back control gate and the well is always reverse-biased, the diode isolating the back control gate from the well and from anything that it may contain (especially other back control gates). In fact, it is of course possible to provide a well common to several back control gates of the same type, as is the case for the well C_{N2} which collectively isolates the back control gates G_{P2} , G_{P3} and G_{P4} .

Returning to Figure 7, the references C_P and C_N represent the wells that isolate the n-type and p-type back control gates respectively. The wells C_P are typically in the low state GND, whereas the wells C_N are typically in the high state V_{DD} .

According to an alternative embodiment (not shown), a second insulating film, placed in the base substrate beneath the insulating film BOX, may contribute, fully or partly, to isolating a back control gate from the base substrate.

A device according to the invention has the following advantages.

A wide performance range may be obtained for the p-FET and n-FET transistors while using only a single physical channel width. Typically, three types of performance are the following:

- regular performance, in the absence of a back control gate:
 - the transistor is then an ordinary SeOI transistor, and it is unnecessary to modify the existing circuit designs;
- boosted performance, with an "ON" back control gate, increasing the conduction of the transistor:
 - the transistor then operates as if it were wider than it actually is, or it has a smaller footprint per performance unit (speed, I_{ON}); and
- reduced performance, with an "OFF" back control gate, reducing the conduction of the transistor:
 - the transistor then operates as if it were narrower than it

actually is. This may prove to be advantageous when performance ratios are desired (in the case of latches, for example of the flip-flop type) since it is therefore unnecessary to widen another device. The leakage currents are also significantly reduced. This type of performance may thus be used in the off-states in so far as no transistor switches (no ratio to be respected), the leakage current I_{OFF} then being reduced.

However, the invention is in no way limited to these three types of performance. Indeed, the performance characteristics can be dynamically modulated by applying an analogue and adjustable bias to the back control gate of a transistor. Any kind of performance in between the above mentioned "reduced performance" and the "boosted performance" can therefore be achieved.

In a particular variant, the back control gate may be biased by any one of multiple predefined voltages. These multiple voltages are typically voltages that are available in the environment of the device, such as V_{dd} , various fractions of V_{dd} (such as $V_{dd}/2$, $V_{dd}/4$) and various combinations of available voltages (such as $V_{dd}-V_{tp}$, $V_{dd}-V_{tn}$, etc.).

Thus, the ratios between the pFET and nFET transistors may be adjusted without having to modify the channel width.

Thus, it will be understood that a device according to the invention obviates the needs encountered in the conventional designs for transistors having different dimensions. Effectively only a single physical width and simplified transistor models and parameters are used. It should be pointed out that the transistor models are actually complex equations with many secondary (parasitic) or tertiary edge effects. Most of these effects depend on the dimensions of the transistor and, for recent technologies, the environment (proximity stress). In the context of the invention, the topology is unique and the models can then be greatly simplified (this results in more rapid availability, shorter development times, etc.).

It should also be noted that there is very low variability owing to the high

level of regularity and because only the polysilicon roughness remains, whereas any fluctuation in the level of dopants disappears when fully depleted structures are produced.

5 A device according to the invention is also insensitive to edge rounding effects of patterns because all the channels have the same physical width. The active zone strip is effectively a long polygon, having no rounding near a polysilicon connection line. The 90° corner of such a line is also far from the active strip (both at the top and the bottom of the structure) and does not interact with the active strip.

10 Moreover, a device according to the invention is insensitive to cross-coupling effects.

This is because, in conventional designs it often happens that a polysilicon connection is adjacent to a drain of another logic gate. The two nodes are then capacitively coupled and mutually disturbed, generally
15 resulting in communication delays. Since the neighbouring of cells is unpredictable, this coupling cannot be taken into account in the model of each cell and is therefore discovered relatively late in the design of the application. In the context of the invention, the interaction between active strip and polysilicon connection is the same for all situations, thereby
20 resolving the drawback encountered in conventional designs. In particular, the modelling of the coupling remains valid after circuit production.

Furthermore, a device according to the invention has a reduced consumption via the association of back control gates with the isolation regions, in order to reduce the leakage currents therein, and the possibility of
25 dynamically acting on the back control gates associated with the transistors in their off-state, in order to further reduce the leakage currents.

To illustrate the effectiveness of the invention, it will be recalled that a standard CMOS cell library may comprise twelve inverters having different performance characteristics.

30 The invention makes it possible, when applied in fully-depleted technology, to use only three inverters (INV₁, INV₄ and INV₈) because the

effective channel width may be modulated by $\pm 50\%$ of the physical width.

In partially-depleted technology, four inverters are necessary (INV_1 , INV_4 , INV_6 and INV_9) because the effective channel width may be modulated by $\pm 30\%$ of the physical width.

5 It follows that the standard cell library is considerably simplified - in fact it can be generally reduced by a factor of 2.

Thus, although around a hundred design rules are used today, the invention makes it possible for only around fifty of them to have to be used.

10 It should be noted in this regard that, in the past, the design rule manual contained approximately 100-200 rules. Since technologies are now generally below 100 nm, many physical effects are appearing that are resulting in new rules that prevent the simple and easy application of the initial set of 100-200 rules. At the 32 nm technology node, the design rule manual comprises about 800 to 1000 rules, in which most of the new rules
15 are complex descriptions of difficult combinations of topologies. This entails a loss of efficiency in terms of footprint. In contrast, the efficiency of the invention remains generally constant. Thus, if the invention and a conventional approach are generally equivalent in terms of footprint used at the 45 nm node, the invention will become increasingly more efficient at
20 subsequent technology nodes.

Moreover, in so far as the set of design rules is an extremely reduced subset of the usual set of rules, and because these rules are applied in a unique context for each of them, it proves possible to design transistors below what the lithography initially permits. In particular, it is possible to
25 optimize the width of contacts (for example by replacing two nominal square contacts by a single rectangular, and somewhat narrower, contact) and the poly-contact distance.

Moreover, it should be noted that the back control gates have the advantage of being buried beneath the insulating film and consequently have
30 no impact on the footprint.

It should also be pointed out that the footprint may be reduced by about

10 to 15% since it is possible to generate strong conduction with the aid of cells "boosted" in accordance with the invention.

Finally, it should be noted that the extreme regularity of what is called the "front-end" structure of the transistors is particularly suitable for the normal use of what are called "back-end" metallizations for what are called "standard" cells (i.e. cells predesigned for general usage).

This is because standard cells are interconnected (routed) together via metallization levels that are alternately horizontal and vertical with a constant pitch. The reduction in number of design rules enormously facilitates the closing-off of the front-end and back-end constraints (the transistor repeat pitch and the routing pitch are made identical). The usage of standard cells then becomes easier since - by construction - the inputs/outputs are placed on the metal routing grid. In the conventional case, this is not always very easy and it is necessary in particular to take into account the possibility of reflecting the cells along the vertical and/or horizontal axes. However, keeping the inputs/outputs of the routing grid often means increasing the footprint of the standard cell. In the case of the invention, all these considerations are eliminated through the general simplification and preplacement of the strips of transistors.

Moreover, the invention is not limited to the device according to its first aspect, rather it extends to a method of driving such a device in which the back control gate region is biased positively or negatively in order to shift the threshold voltage of the transistor. Advantageously, a p-type back isolation gate is connected to ground and an n-type back isolation gate is connected to a nominal supply voltage.

As mentioned above, the application of a back gate voltage on a FDSOI transistor modifies the electrical characteristic of the device. Simply described, a higher voltage on the back gate reduces the threshold voltage of a N-channel device and vice-versa. The same applies on P channel devices in absolute values.

It is possible to saturate this effect by applying very high voltages on the

back gates. For instance a very high voltage applied on a N-channel transistor reduces its threshold down to a negative value, making the transistor always ON, despite the voltage level applied on its front gate. On the contrary, a (very) negative voltage on the back gate increases the threshold above the power supply V_{dd} , at a level such that the transistor remains OFF for all voltages applied on its front gate (0- V_{dd}). By symmetry the same applies on the complementary P channel device.

In other words, transistors can be transformed into “open” and “shorts” through an appropriate back gate control. This feature proves to be particularly efficient to create a reconfigurable logic. Figure 9 represents an example of a reconfigurable logic circuit that can be converted in all 2-input Boolean functions, depending on the voltage applied on the back gate BG1-BG4 of the various transistors T1-T4, as indicated on the truth table of figure 10.

On figure 9, A and B represent the two inputs of the reconfigurable logic circuit, while OUT represents the output of the reconfigurable logic circuit. On figure 10, V_{pp} represents a voltage that is sufficiently high to force the threshold voltage either to a negative value (the transistor is always ON) or a value higher than the supply voltage V_{dd} (the transistor is always OFF) for a N-channel transistor, and respectively to a value either positive or greater than V_{dd} in absolute value for a P-channel transistor. It will be noted that this principle of reconfigurable logic can easily be extended to 3 or more inputs.

Transforming transistors into “opens” and “shorts” through an appropriate back gate control proves interesting for re-programmable circuits such as FPGA for instance. In this case, the back gate is not used to modulate the strength of the transistor but to establish or cut electrical links between a group of transistors. Of interest is that the layout of a re-programmable cell is unique for all functions.

The voltage applied to the different back gates advantageously comes from external, and if possible adjacent, circuits such as SRAM cells or Flash cells. The programming of the various functions that can be implemented by

the re-programmable circuits is stored in these circuits. As all Boolean functions can be programmed from this type of cells, then a unique and predefined back-end interconnection can be defined as well. As a result the predefined chip can be fully processed and then programmed by the end user. For instance, figure 11 shows a re-reprogrammable logic circuit according to the invention and indicates a possible arrangement of the logic cells LC (each logic cell corresponding for instance to the circuit of figure 9) and of the memory cells MC (SRAM or Flash) used to store the programming of the logic cells and to deliver the appropriate voltages to the back gates. In figure 11, strips of logical cells LC are interleaved with rows of memory cells MC. For clarity purpose, the logic cells LC have been schematically represented by a box on figure 11, while the arrows originating from the memory cells MC represent the control of the back gate voltages of the logic cells LC by the memory cells MC.

The memory cells MC use only the metal1 and metal2 layers at relatively relaxed pitches as the dimensions are induced by the transistor pitches in the logic area LC. On figure 11, M1-MC represents the metal1 layer used for selecting rows of the memory cells MC, while M2-MC represents the metal2 layer used for selecting columns of the memory cells. In particular there is still enough resources at the metal2 level to connect different inputs and outputs of the logic cells LC to a predefined network composed by the upper metal layers. On figure 12, M2-LC represents the metal2 layer used for interconnecting tracks of logic cells LC, while M3-LC represents the metal3 layer used for interconnecting tracks of logic cells LC.

CLAIMS

1. Semiconductor device formed on a semiconductor-on-insulator substrate comprising a thin film of semiconductor material separated from a
5 base substrate by an insulating film, the device comprising an array of patterns each formed from at least one field-effect transistor, each transistor having, in the thin film, a source region, a drain region and a channel region which is delimited by the source and drain regions, and furthermore comprising a front control gate region formed above the channel region, the
10 patterns being arranged in the form of rows, the source and drain regions of any one row having the same dimensions and being spaced apart by front control gate regions of fixed dimensions, characterized in that at least one transistor of a pattern has a back control gate region formed in the base substrate beneath the channel region, the back gate region being capable of
15 being biased in order to shift the threshold voltage of the transistor to simulate a modification in the channel width of the transistor or to force the transistor to remain off or on whatever the voltage applied on its front control gate.
- 20 2. Device according to Claim 1, in which some of the patterns in a row are formed on one and the same active zone of the thin film of the semiconductor substrate and in which an isolation region delimits the adjacent patterns, the isolation region comprising a front isolation gate formed above the active zone and a back isolation gate formed in the base substrate beneath the
25 active zone.
3. Device according to Claim 2, in which a back isolation line connects the back isolation gates of each of the isolation regions of any one row.
- 30 4. Device according to Claim 3, in which the back isolation line is common to several rows.

5. Device according to one of Claims 2 to 4, in which the back isolation gate has a conductivity of opposite type to that of the active zone.
- 5 6. Device according to Claim 1, in which a back gate line connects the back gate region(s) of one or a plurality of transistors.
7. Device according to Claim 6, in which a back gate line connects the back gate region(s) to ground or to a nominal supply voltage.
- 10 8. Device according to Claim 6, in which a back gate line connects the back gate region(s) to an analogue and adjustable potential.
9. Device according to Claim 1, in which the back gate region is isolated
15 from the base substrate by a well of opposite conductivity.
10. Device according to Claim 1, in which the back gate region has a conductivity of the same type as that of the transistor channel.
- 20 11. Device according to Claim 1, in which the back gate region has a conductivity of opposite type to that of the transistor channel.
12. Method of driving a device according to Claim 1, in which the back control gate region is biased positively or negatively in order to shift the
25 threshold voltage of the transistor.
13. Method according to claim 12, in which the back control gate region is biased by an analogue and adjustable potential.
- 30 14. Method of driving a device according to claim 1, in which the shift of the threshold voltage is controlled to cause the transistor to remain off or on whatever the voltage applied to its front control gate.

15. Method according to claim 14, wherein the shift of the threshold voltage is programmed by means of memory cells that store and deliver predetermined voltages to the back control gates.

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16. Re-programmable circuit comprising a device according to claim 1 interleaved with rows of memory cells that store and deliver predetermined voltages to the back control gate regions.