

DESCRIPTION

INTEGRATED CIRCUIT INTERNAL SIGNAL MONITORING APPARATUS

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TECHNICAL FIELD

The present invention relates to an integrated circuit internal signal monitoring apparatus, in particular, an apparatus characterized by a read operation of a plurality of internal states without increasing the number of input/output pins provided in a large scale integrated circuit (hereinafter, referred to as an LSI) system.

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BACKGROUND ART

Conventionally, an integrated circuit internal signal monitoring apparatus as described in Japanese Patent No. 2580558 is known.

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A conventional integrated circuit internal signal monitoring apparatus will be described with reference to Figure 3. In order to monitor from outside an internal operation of a circuit block 12 provided in an LSI 11, a selector 19 is provided. The circuit block 12 has its original function. The selector 19 receives signals 21 to be monitored among signals inside the circuit block 12 as inputs, and also receives a selection signal 31 from outside the LSI 11 through an input pin, thus to designate the specific signal to be monitored. Based on the value of the selection signal 31, the selector 19 selects a plurality of signals 32 from the input signals 21 and outputs the signals 32 to outside the LSI 11 through an output pin, so that the signals can be monitored.

However, the conventional structure described above has the following problem. When signals driven inside the LSI 11 are monitored outside through the LSI output pins, a large number of output pins for monitoring and the selection signal input pins are required, as the number of the signals to be simultaneously monitored increases. Therefore, the number of pins in the entire LSI 11 increases.

Furthermore, when monitoring the LSI internal signals from outside the LSI 11 with a logic analyzer or the like, a signal analysis performed with the internal states of the LSI as event conditions requires even the internal signals relating to the event conditions to be output externally. This causes a problem of a further increase in the number of the input/output pins.

DISCLOSURE OF THE INVENTION

An integrated circuit internal signal monitoring apparatus according to the present invention includes: an integrated circuit, including: signal change information generating means for detecting changes in a plurality of internal signals to be monitored in a circuit block, and for, when a level of at least one of the plurality of internal signals is changed, sequentially generating flags indicating the internal signal whose level has been changed, the post-change level, and that the levels of other internal signals have not been changed, storage means for sequentially storing the flags generated by the signal change information generating means, and trigger generating means for generating a write stop trigger signal for stopping a write operation of the flags to the storage means; and

internal signal waveform reproduction means for reading the flags from the storage means after the generation of the write stop trigger signal, and reproducing waveforms of the plurality of internal signals. Thus, the above-described problems are solved.

The storage means includes a ring buffer, and the flags may be sequentially stored in the ring buffer in a time series.

The trigger generating means may generate the write stop trigger signal when a value of one of the plurality of internal signals and an expected value of a signal input from outside the integrated circuit match each other.

According to one aspect of the present invention, LSI internal signals around a required point can be monitored with a significantly smaller number of input/output pins compared to the prior art, and debug can easily be performed based on a signal state around a generation time of external events and internal events.

According to another aspect of the present invention, only a signal change point value is stored to a storage device, and information of the storage device is read from outside to form waveforms as necessary. Thus, the number of LSI input/output pins can be reduced, and, in a system incorporating an LSI, the system can easily be debugged by monitoring an internal signal state with the time to monitor being specified.

According to still another aspect of the present invention, the capacity of storage means can be reduced,

and an internal signal state of an LSI system can be monitored without increasing the number of LSI input/output pins, and thus system debug is easily performed.

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BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram of an integrated circuit internal signal monitoring apparatus according to an embodiment of the present invention.

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Figure 2 shows a waveform diagram of signals to be monitored by the integrated circuit internal signal monitoring apparatus according to the embodiment of the present invention and a diagram for schematically illustrating a recording state of a ring buffer.

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Figure 3 is a block diagram of a conventional integrated circuit internal signal monitoring apparatus.

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BEST MODE FOR CARRYING OUT THE INVENTION

Hereinafter, an embodiment according to the present invention will be described with reference to Figs 1 and 2.

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Figure 1 illustrates a block structure of an LSI internal signal monitoring apparatus 100 according to the present invention. Figure 2 illustrates a waveform diagram and storage contents for illustrating an operation of recording signal change information of internal signals to be monitored of an LSI 11 to a storage device.

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In order to monitor from outside an internal

operation of a circuit block 12 provided in the LSI 11, signals 21 as monitoring targets inside the circuit block 12 are processed with a structure described below. The circuit block 12 has its original function. The
5 signals 21 as monitoring targets are input to a signal change information generating section 13. When an arbitrary signal, among all the signals 21 as monitoring targets, changes, flags 28 indicating the signal level immediately after the change, and that the other signals have not been
10 changed, are generated, and are sequentially stored in a ring buffer 14. The timing to stop a write operation to the ring buffer 14 depends on a write stop trigger signal 27, which is output from an event trigger generating section 15.

15 Next, a process of an event trigger generation will be described. There are two types of trigger events; one is based on a change in a signal 24 from outside the LSI 11, and the other is based on a change in an internal signal 22 of the circuit block 12. In the former case, the write stop
20 trigger signal 27 is generated based on the change in the signal 24 from outside. In the latter case, the write stop trigger signal 27 is generated based on the change in the internal signal 22. In more detail, a signal used for a trigger event is selected from the internal signals 22 by
25 using a selector 18 based on an event designation signal 23 set from outside the LSI 11 and stored in an internal state latching section 16. An expected value of the signal selected by the event designation signal 23 is written to an event designation section 17. A signal value 25 which
30 is to be a trigger factor and an expected signal value 26 written to the event designation section are continuously compared by the event trigger generating section 15, and when the signal values 25 and 26 match, the trigger signal 27

is output.

The write stop trigger signal 27 output by the event trigger generating section 15 stops the write operation of the flag information 28 to the ring buffer 14. The write stop trigger signal 27 is output to an internal signal waveform reproduction section 30, and thus, the information that the write operation to the ring buffer 14 has been stopped is sent to the internal signal waveform reproduction section 30. The internal signal waveform reproduction section 30 provided outside the LSI 11 reads out read information 29 from the ring buffer 14. The read operation can also be performed by using a single serial pin. The internal signal waveform reproduction section 30 reproduces an internal signal waveform based on the read information 29.

Next, a write operation of the flag 28 will be described with reference to Figure 2. The flag 28 is write information to be written to the ring buffer 14 (having 8 locations) for storing the signal change information of the internal signals of the LSI 11 to be monitored. It is assumed that 4 types of signals are input to the signal change information generating section 13. First, at point [1] where signal A changes from "L" to "H", other signals B, C, and D do not change. Therefore, the flag 28, which is the write information to be written to the ring buffer 14, is "1" for signal A immediately after a rise, indicating "H", and "2" for the other signals, indicating that the level has not been changed. Next, at point [2] where signal B changes from "H" to "L", the flag 28 as the write information to be written to the ring buffer 14 is "0" for signal B immediately after a fall, indicating "L", and "2" for the

other signals, indicating that the level has not been changed. Thereafter, flag information at the signal change points are sequentially written to the ring buffer 14 in a similar manner.

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After the flag is written for the final point [8] of the ring buffer 14, at the next change point [9], the flag information at point [9] ("1" for signal B, and "2" for the other signals) is written over the leading information of the ring buffer 14. In this example, an address pointer of the ring buffer 14 points to the pointer position in the figure in the state where the flag information up to the state at change point [10] has been written to the ring buffer 14. In the case where the event trigger generating section 15 outputs the write stop trigger signal 27 at this point, the write operation of the flag information 28 to the ring buffer 14 stops. Then, for reading the information of the ring buffer 14 from outside, the output flag information 29 is read in the order of [3], [4], [5], [6], [7], [8], [9], and [10], starting from the pointer. Thus, waveforms of signals A, B, C, and D can be reproduced.

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INDUSTRIAL APPLICABILITY

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As described above, according to the present invention, it is possible to reduce the number of input/output pins used, regardless of the number of internal control signals to be monitored, and thus to provide an integrated circuit internal signal monitoring apparatus which is capable of simultaneously monitoring a large number of signals. Compared to the prior art, a chip size of the LSI can be smaller. When a system including the LSI is

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debugged, trigger generation and signal analysis using an external logic analyzer are not required. Therefore, a phase relation of the inner control signals around the event trigger generation time can easily be analyzed.

AMENDED CLAIMS

1. An integrated circuit internal signal monitoring apparatus, comprising:
 - an integrated circuit, comprising:
 - signal change information generating means for determining whether a level of at least one of the plurality of internal signals to be monitored in a circuit block has changed, and when it is determined that the level of at least one of the plurality of internal signals has changed, sequentially generating flags indicating a direction along which the level of at least one of the plurality of internal signals has changed and indicating that the levels of other internal signals have not been changed,
 - storage means for sequentially storing the flags generated by the signal change information generating means, and
 - trigger generating means for generating a write stop trigger signal for stopping a write operation of the flags to the storage means; and
 - internal signal waveform reproduction means for reading the flags from the storage means after the generation of the write stop trigger signal, and reproducing waveforms of the plurality of internal signals.
2. An integrated circuit internal signal monitoring apparatus according to claim 1, wherein the storage means includes a ring buffer, and the flags are sequentially stored in the ring buffer in a time series.
3. An integrated circuit internal signal monitoring apparatus according to claim 1, wherein the trigger generating means generates the write stop trigger signal

when a value of one of the plurality of internal signals and an expected value of a signal input from outside the integrated circuit match each other.