

SEAM HEALING USING HIGH PRESSURE ANNEAL

BACKGROUND

Field

[0001] Embodiments of the present disclosure generally relate to integrated circuit fabrication methods, and in particular, to correcting seam defects in semiconductor devices.

Description of the Related Art

[0002] The miniaturization of semiconductor devices continues to require increasing complexity of geometry and arrangement of material layers which form the device. Among these, properly filling features formed on the semiconductor device, such as trenches and vias, with a material is increasingly difficult due to the shrinking size of the features.

[0003] Features are typically filled by a deposition process, such chemical vapor deposition (CVD), physical vapor deposition (PVD), or plating processes, which can result in less than optimal filling of the features. Problems arise from the accumulation of material at the upper surface of the feature. The accumulation of such material at the edges of the feature can block or otherwise obstruct the feature prior to completely and evenly filling the feature, resulting in the formation of voids, seams, and uneven structures within the feature. The smaller features that are used in smaller geometry devices, such as trenches in the tens-of-nanometer range, necessarily have a larger aspect ratio (i.e., relationship of feature height to width) than do larger geometry devices, thereby exacerbating the trench and via filling difficulties described above.

[0004] Conventional approaches utilize multiple cycles of deposition and anneal in attempt to repair seams and cavities in the features. However, these conventional approaches result in extremely slow process time. Further, these approaches can damage the material of the semiconductor device and cause reliability issues in the operation of the semiconductor device.

[0005] Therefore, there is a need for an improved method of correcting seam defects.

SUMMARY

[0006] In one embodiment, a method of processing a substrate is provided, including positioning a substrate with a plurality of substrate features in a process chamber, depositing a conformal layer on the substrate features, and treating the substrate with a high pressure anneal. A seam is formed between neighboring substrate features when the conformal layer is deposited. The high pressure anneal is performed in the presence of an oxidizer. The volume of the seams within the conformal layer are reduced by the high pressure anneal.

[0007] In another embodiment, a method of processing a substrate is provided, including positioning a substrate with a plurality of substrate features in a process chamber, depositing a conformal layer on the substrate features, and treating the substrate with a high pressure anneal. The conformal layer is crystalline in structure. A seam is formed between neighboring substrate features when the conformal layer is deposited. The high pressure anneal is performed in the presence of an oxidizer. The volume of the seams within the conformal layer are reduced by the high pressure anneal.

[0008] In another embodiment, a method of processing a substrate is provided, including positioning a substrate with a plurality of substrate features in a process chamber, depositing a conformal layer on the substrate features, and treating the substrate with a high pressure anneal. The conformal layer is crystalline in structure. A seam is formed between neighboring substrate features when the conformal layer is deposited. The high pressure anneal is performed in the presence of an oxidizer. The volume of the seams within the conformal layer are reduced by the high pressure anneal. The volume of the conformal layer expands during the high pressure anneal.

[0009] The high pressure anneal helps reduce the size of the seams located between conformal films, where the conformal films are disposed on adjacent features of the semiconductor. The reduction in seam size increases the electrical insulating properties of the conformal film.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] So that the manner in which the above recited features of the present disclosure can be understood in detail, a more particular description of the disclosure, briefly summarized above, may be had by reference to embodiments, some of which are illustrated in the appended drawings. It is to be noted, however, that the appended drawings illustrate only exemplary embodiments and are therefore not to be considered limiting of scope, as the disclosure may admit to other equally effective embodiments.

[0011] Figure 1 is a flowchart of a method of processing a substrate according to one embodiment of the disclosure.

[0012] Figure 2A is a sectional view of a substrate at one operation of the method of Figure 1.

[0013] Figure 2B is a sectional view of a substrate at one operation of the method of Figure 1.

[0014] Figure 2C is a sectional view of a substrate at one operation of the method of Figure 1.

[0015] Figure 2D is a sectional view of a substrate at one operation of the method of Figure 1.

[0016] Figure 3 is a sectional view of an exemplary annealing chamber.

[0017] To facilitate understanding, identical reference numerals have been used, where possible, to designate identical elements that are common to the figures. It is contemplated that elements and features of one embodiment may be beneficially incorporated in other embodiments without further recitation.

DETAILED DESCRIPTION

[0018] Embodiments of the disclosure provided herein include methods of treating a substrate to remove defects, such as seams, in interconnects formed on the substrate. In some embodiments, the method includes heating the substrate in a pressurized environment in the presence of an oxidizer. The conformal layers

deposited on the substrate expand in volume, such that the conformal layers on opposing sides of a seam chemically cross-link with one another, reducing or eliminating the seams. Embodiments of the disclosure may prove useful for, but are not limited to, decreasing the size of seams on substrate features.

[0019] Figure 1 is a flow diagram of a method 100 for processing a substrate 210, according to one embodiment of the disclosure. Figures 2A-2D are schematic sectional views a substrate at stages of the method 100. To facilitate explanation of aspects of the disclosure, Figures 2A-2D will be explained in conjunction with Figure 1.

[0020] Method 100 begins at operation 102. In operation 102, a substrate 210 is positioned in a process chamber. The process chamber is, for example, a deposition chamber. The substrate 210 includes one or more substrate features 212 formed thereon. Here, the substrate features 212 are four trenches. The substrate 210 can be a photomask, a semiconductor wafer, or other workpiece. The substrate 210 comprises any material to make any of integrated circuits, passive (e.g., capacitors, inductors) and active (e.g., transistors, photo detectors, lasers, diodes) microelectronic devices, according to some embodiments. The substrate 210 comprises insulating or dielectric materials that separate such active and passive microelectronic devices (or features thereof) from a conducting layer or layers that are formed on the substrate. In one embodiment, the substrate 210 is a semiconductor substrate that includes one or more dielectric layers e.g., silicon dioxide, silicon nitride, aluminum oxide, and other dielectric materials. In one embodiment, the substrate 210 includes a one or more layers of films. The one or more layers of the substrate 210 can include conducting layers, semiconducting layers, insulating layers, or any combination thereof.

[0021] At operation 104, a conformal layer 214 is deposited in the substrate features 212. The conformal layer 214 is a silicon-containing layer, such as a silicon dioxide layer, according to one embodiment. The conformal layer 214 is a metal oxide layer, such as aluminum oxide or vanadium oxide, according to one embodiment. The conformal layer 214 is formed by a deposition process. The deposition process is chemical vapor deposition (CVD) or atomic layer deposition

(ALD), according to some embodiments. To deposit the conformal layer 214, a first precursor is flowed into the processing chamber. The precursor may comprise silicon (Si) and hydrogen (H). According to some embodiments, the precursor comprises a silane precursor, a disilane precursor, a trisilane precursor, or a tetrasilane precursor. The first precursor is reacted with a second precursor gas, such as an oxidizing agent, for example ozone or oxygen radicals, to form silicon dioxide within the substrate features 212. The deposition process occurs at a processing temperature in a range, for example, between about 150 degrees Celsius and about 700 degrees Celsius, between about 250 degrees Celsius and about 600 degrees Celsius, between about 300 degrees Celsius and about 550 degrees Celsius, such as between about 350 degrees Celsius and about 500 degrees Celsius. Additionally, during deposition, the chamber is maintained at a reduced pressure. For example, the pressure in the chamber may be between about 5 Torr and about 700 Torr, between about 10 Torr and about 600 Torr, such as between about 15 Torr and about 500 Torr.

[0022] As shown in Figure 2B, the deposited conformal layer 214 is deposited on the substrate 210 in the substrate features 212. The conformal layer 214 conforms to the shape of the substrate features 212, thereby forming a seam 216 within the substrate features 212. It is to be noted that the seam 216 is exaggerated in size for clarity. In some aspects, the conformal layer 214 formed on adjacent structures defining the substrate features 212 may be deposited to a thickness sufficient to contact the conformal layer 214 on an opposite surface of a respective substrate feature 212. Stated otherwise, the seam 216 need not necessarily include a physical void, but rather, the seam 216 may form as a result of portions 240, 250 of the conformal layer 214 contacting one another, for example, within the substrate feature 212. The presence of the seam 216 negatively affects performance of the gapfill within substrate feature 212 by decreasing the electrical insulating properties thereof.

[0023] The substrate 210, having the conformal layer 214 thereon, is transferred to an anneal chamber at operation 106. At operation 108, the substrate 210 is treated with a high pressure anneal. The high pressure anneal is performed with the substrate 210 in the presence of an oxidizer 220 such as steam or a steam/oxygen

mixture. The substrate 210 is annealed at an annealing temperature. The annealing temperature is about 100 degrees Celsius to about 600 degrees Celsius, such as about 150 degrees Celsius to about 550 degrees Celsius, or about 200 degrees Celsius to about 500 degrees Celsius.

[0024] The pressure within the anneal chamber is raised to a predetermined pressure in order to perform the high pressure anneal. The predetermined pressure is between about 1 bar and about 90 bar, such as about 1 bar to about 80 bar, or about 1 bar to about 70 bar. The increased pressure forces the oxidizer 220 within the environment of the anneal chamber down into the seams of the conformal layer 214. The substrate 210 is treated with the high pressure anneal for a desired soak time. The soak time is generally about 3 minutes to about 150 minutes, such as about 5 minutes to about 120 minutes.

[0025] During the high pressure anneal, the oxidizer 220 is carried into the seams 216 by the high pressure. The conformal layer 214 deposited within the substrate features 212 is exposed to the oxidizer 220 in Figure 2C. The arrows illustrate the flow of the oxidizer 220 into the seams 216. During the anneal process, the conformal layer 214 oxidizes as a result to exposure of the oxidizer 220. As a result of the oxidation, the conformal layer 214 undergoes a volume expansion. That is, the volume of the conformal layer 214 increases, such as to an expanded volume 218, shown in phantom. The expanded volume 218 shown in Figure 2C represents conformal layer 214 undergoing volume expansion during the high pressure anneal.

[0026] As a result of the oxidation process of the high-pressure anneal of the high pressure anneal, the conformal layer 214 is converted to a densified oxide substantially free of the seams 216 as shown in Figure 2D. As the conformal layer 214 expands during the high pressure anneal, portions of the conformal layer 214 that do not contact, such as portions 240, 250 of the conformal layer 214 opposed across the seam 216, expand until the portions interact with one another. Oxidation at the seam boundary facilitates reaction between portions 240, 250, such that the atoms of the oxidizer 220 react and/or cross-link with each portion 240, 250. The reaction and/or cross-linking of portions 240, 250 across the seam 216 results in formation of a unified structure and removal of the seam. In examples wherein the

conformal layer 214 is crystalline in structure, the oxidizer 220 results in joining of the crystal structures of portions 240, 250, thereby eliminating the seam 216.

[0027] In addition to healing seams in the conformal layer 214, the high pressure anneal of operation 208 densifies the conformal layer 214 via the inclusion of additional oxide, further improving the electrical insulating properties of the conformal layer 214.

[0028] Figure 1 illustrates one embodiment of treating a substrate 210. However, additional embodiments are also contemplated. In another aspect, operations 104 and 108 may occur in the same chamber without operation 106. In another aspect, operation 104 may include multiple deposition steps or cycles to form the conformal layer 214.

[0029] Additionally, it is contemplated the conformal layer 214 may be a layer other than silicon dioxide, such as silicon, germanium, a metal layer, a metal oxide layer, or combinations thereof. In such an embodiment, the metals used to form the conformal layer 214 include aluminum, titanium, vanadium, chromium, manganese, iron, cobalt, nickel, copper, yttrium, zirconium, hafnium, molybdenum, and alloys thereof, among others. The metals may also be used in combination with one another.

[0030] In other embodiments, it is contemplated that deposition processes other than CVD may be used to deposit material in the substrate features 212. For example, atomic layer deposition (ALD), plasma-enhanced, ALD, plasma-enhanced CVD, physical vapor deposition (PVD), plating, or other deposition methods may be utilized, according to various materials to be deposited in the substrate features 212.

[0031] Moreover, while Figures 2A-2D illustrate a substrate 210 having trenches thereon, it is contemplated that the substrate features 212 other than trenches may benefit from aspects of the disclosure.

[0032] Figure 3 is a schematic sectional view of an exemplary processing chamber which may be practiced with the methods described herein. The batch processing chamber 300 has a cassette 330 disposed in an internal volume 350 for processing a plurality of substrates 335. The batch processing chamber 300 has a

chamber body 310 enclosing the internal volume 350, and a lid 311 disposed on the chamber body 310. One or more cartridge heaters 312 are disposed within the chamber body 310. The heaters 312, such as resistive heaters, are configured to heat the chamber body 310. Power to the heaters 312 is controlled by the controller 380. A shell 320 is disposed within the internal volume 350. An insulating liner 316 is disposed in the internal volume 150 surrounding the shell 320. The insulating liner 316 prevents heat transfer between chamber body 310 and the shell 320.

[0033] The cassette 330 couples to a shaft 374 which extends through an opening 354 in the chamber body 110. The cassette 330 is moveably disposed within the internal volume 350 by an actuator 370 coupled to the shaft 374. The cassette 130 facilitates transfer of substrates 335 between a loading position and a processing position. Substrates 335 are transferred into and out of the internal volume 350 through a loading port 395 formed in the chamber body 310. The shell 320 couples to the lid 340 of the cassette 330 when the cassette 330 is in the processing position and defines a processing region wherein the substrates 335 are annealed at an elevated pressure and an elevated temperature.

[0034] During processing, a processing fluid, such as an oxidizer 220, is flowed into the processing region through an inlet port 352. The inlet port 352 is in fluid communication with the substrates 335 through a plurality of apertures 333 in the cassette 330. Auxiliary heaters 327, disposed within the processing region, are configured heat the processing volume and the substrates 335 therein. The pressure and temperature within the processing region are raised in order to anneal the substrates 335 therein. The processing fluid is evacuated from the processing region through an outlet port 356.

[0035] The controller 380 is coupled to a plurality of sensors 314, such as temperature sensors or pressure sensors. The sensors 314 provide signals to the controller 380 to indicate the conditions within the internal volume 350. The controller 380 controls the flow of the processing fluid as well as the power supplied to the heaters 312 and auxiliary heaters 327 to process the substrates 335 in a desired manner. In such a manner, the controller 380 is configured to control aspects of the processing chamber 300 to perform operations as disclosed herein.

[0036] In one example of operations disclosed herein, a substrate 210 containing one or more substrate features 212 is positioned in a process chamber. A conformal layer 214 is deposited on the substrate features 212 of the substrate 210. The substrate 210 is transferred to an anneal chamber. A high pressure anneal is performed on the substrate 210, and the conformal layers 214 expand in volume such that adjacent conformal layers contact and/or chemically react with one another.

[0037] The method described herein results in a high quality oxide layer that is substantially free of seams or voids. The layer is oxidized in a substantially uniform manner across the entirety of the layer, thereby increasing uniformity of the distribution of oxygen throughout the layer. Further, the uniformity of the densification of the oxide layer is increased by the methods described herein. The uniform densification also results in improved etch selectivity.

[0038] While the foregoing is directed to embodiments of the present disclosure, other and further embodiments of the disclosure may be devised without departing from the basic scope thereof, and the scope thereof is determined by the claims that follow.