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METHOD FOR ENHANCING SURFACE CONDITION

The present invention generally concerns the surface treatment of materials, and particularly the treatment of substrates intended for the fabrication of components in microelectronics and/or optoelectronics applications.

More precisely, the invention concerns a method for enhancing the condition of the free surface of a wafer in semiconductor material, said method comprising a rapid thermal annealing step to smooth said free surface.

By "free surface" is meant the surface of a wafer which is exposed to the outside environment (as compared with an interface surface which is in contact which the surface of another wafer or another element).

By "rapid thermal annealing" is meant rapid annealing in a controlled atmosphere, following a method that is usually known as the RTA method, the abbreviation for Rapid Thermal Annealing.

In the remainder of this description, this method shall indifferently be called rapid thermal annealing or RTA.

To achieve RTA annealing of a wafer of material, the wafer is annealed at a high temperature, possibly in the region of 1100°C to 1300°C for 1 to 60 seconds.

RTA annealing is conducted in a controlled atmosphere. In the preferred application of the invention, this atmosphere may for example be an atmosphere containing a mixture of hydrogen and argon, or an atmosphere of pure argon.

In this preferred application of the invention, said invention is implemented in particularly advantageous manner in combination with a method for fabricating thin films or layers of semiconductor material of the type described in patent FR 2 881 472.

One method reproducing the teaching of the above-cited document is known as the SMARTCUT® method. Its main steps are schematically as follows:

- an atom implanting step to implant atoms under a surface of a substrate in semiconductor material (silicon in particular) in an implantation zone of the substrate,
- a contacting step for close contacting of the implanted substrate with a stiffener, and
- a splitting step of the implanted substrate at the implantation zone, to transfer that part of the substrate located between the surface submitted to implantation and the implantation zone onto the stiffener thereby forming a thin film, or a layer, of semiconductor upon the latter.

By atom implantation is particularly meant any bombarding of atom or ion species able to insert these species in the wafer material with a maximum concentration of implanted species located at a determined depth of the wafer relative to the bombarded surface, so as to define a weakening zone.

The depth of the weakening zone is dependent upon the type of species implanted, and on their implanting energy.

It is specified that in this description by the general term "wafer" is meant the film or layer transferred by said method of SMARTCUT® type.

The wafer (which is in semiconductor material) may therefore be associated with a stiffener and optionally with other intermediate layers.

In this description, the term "wafer" also covers any wafer, layer or film of semiconductor material such as silicon, whether or not the wafer has been produced by a method of SMARTCUT® type, the objective in all cases being to enhance the condition of the free surface of the wafer.

For the applications mentioned at the start of this description, the roughness specifications associated with the free surface of wafers are very stringent, and the roughness of the free surface of wafers is a parameter which, to a certain extent, determines the quality of the components which are to be made on this wafer.

It is therefore frequent to find roughness specifications which do not exceed 5 Angstroms in rms value (rms standing for root mean square).

It is specified that roughness measurements are generally made using an Atomic Force Microscope - AFM).

With this type of apparatus, roughness is measured on surfaces scanned by the tip of a AFM microscope, and ranges from 1x1 μm^2 to 10x10 μm^2, and more unusually 50x50 $\square m^2$, and even sometimes 100x100 μm^2.

Roughness can be characterized according to two modalities in particular.

According to the first, roughness is said to be high frequency and relates to scanned surfaces in the order of 1x1 μm^2.

According to the second modality, roughness is said to be low frequency and relates to scanned surfaces in the order of $10x10\mu m^2$ or greater. The 5-Angstrom specification given above by way of indication is therefore a roughness corresponding to a scanned surface of $10x10\mu m^2$.

And wafers which are produced using known methods (SMARTCUT® or other methods) have surface roughness values which are greater than those mentioned above, in the absence of any specific treatment to the wafer surface such as polishing.

One first type of known method to reduce the roughness of wafer surfaces consists of submitting the wafer to "conventional" heat treatment (sacrificial oxidation for example).

But treatment of this type does not make it possible to bring wafer roughness down to the level of the above-mentioned specifications.

And while it is indeed possible to consider multiplying the steps of said conventional heat treatment and/or combining them with other types of known methods, to further reduce surface roughness, this would require a long, complex process.

A second type of known method for reducing surface roughness consists of conducting chemical-mechanical polishing of the free surface of the wafer.

With this type of method it is effectively possible to reduce the roughness of the free surface of the wafer.

If the defect concentration has an increasing gradient in the direction of the free surface of the wafer, with this second type of known method it is also possible to abrade said wafer down to a zone having an acceptable defect concentration.

However, this second type of known method has the disadvantage of compromising the uniformity of the thickness of the effective layer of the wafer, that is to say the layer which will effectively be used to create components.

And this disadvantage is heightened if major polishing of the wafer surface is performed, which would be the case in order to achieve roughness values such as those mentioned above.

According to a third type of method, the wafer is subjected to RTA annealing in a controlled atmosphere.

With this third type of method it is possible, in generally satisfactory manner, to reduce the surface roughness of wafers (in particular without deteriorating the thickness uniformity of the effective layer) and this therefore offers a solution of interest.

However, while it is indeed possible with this third type of method to achieve globally satisfactory high frequency and low frequency roughness values, the Applicant has observed that submitting the wafer to RTA annealing can lead to a disadvantage.

On fine analysis of the surface condition of wafers (silicon wafers in particular) which have undergone such treatment, the Applicant found that holes of very small size were superimposed on a surface whose general roughness was otherwise satisfactory.

Such analysis can be made by observation through an atomic force microscope.

These small holes typically have a size in the order of a few nm in depth and a few dozen nm in diameter.

These holes have similarities with the holes that can sometimes be observed on the surface of materials such as silicon and which are attributed to a so-called 'pitting' phenomenon.

It is specified that while the term "pitting" will be used in this description for reasons of practicality, the depth/diameter ratio of these holes is less than the ratios usually encountered in conventional cases of pitting.

More precisely, the "pitting" with which we are concerned here does not have the same cause as the "pitting" phenomenon which is generally described in the state of the art.

Pitting in the state of the art is generally due to defects embedded in the thickness of the wafer material.

These defects may be attacked by heat treatment (for example heat treatment to improve the surface condition of the wafer).

Therefore, in the state of the art, the phenomenon of pitting relates to holes generated by the attack of embedded defects.

In this respect, reference may be made to patent application EP 1 158 581 which specifies the characteristics of these embedded defects - in particular defects of "COP" type, COP standing for Crystal Originated Particle. Reference may be made for example to the passage on page 1 lines 48 to 54 of this patent application.

It will also be noted that this application only sets out to improve the "long period" components of roughness, which relate to low frequency roughness (scanned surfaces in the order of 10x10 μm^2) whereas high frequency components of roughness are not treated (see in particular page 10 lines 54-55 of this application). Yet the phenomenon designated as "pitting" in this description also relates to high frequency roughness.

In other documents, example EP 1 045 448 or FR 2 797 713, this same treatment objective for "pitting" as defined by the state of the art is also found.

And in these documents, the "pitting" to which reference is made is not the "pitting" concerned by the present invention.

For example EP 1 045 448 specifies that the targeted defects are of "COP" type, these defects being, as we have seen, embedded defects whose attack is likely to generate fairly deep holes.

EP 1 045 448 therefore specifies (column 2 lines 55 *et al*) that COPS may extend down to the embedded oxide layer of a structure of SOI type (that is to say that these defects may extend into the thickness of the material as far as this embedded oxide layer which is located underneath an effective layer of silicon whose thickness may typically reach a few thousand angstroms).

The corresponding "pitting" holes, in the case of EP 1 045 488 therefore have a depth possibly reaching these values of a few thousand angstroms.

Therefore "pitting" as understood in the state of the art designates holes that are:

- generated by the attack of defects embedded in the thickness of the wafer layer

- these holes possibly having a depth in the order of a few thousand angstroms.

The "pitting" concerned by the present invention, on the other hand, does not result from the attack of pre-existing defects.

This pitting only relates to places on the wafer surface on which reconstruction smoothing by RTA annealing is not fully achieved, causing the onset of the small holes mentioned above.

The "pitting" concerned by the invention is therefore a purely superficial phenomenon.

In this respect, reference may be made to the single figure which shows a section view of a silicon wafer 10 whose surface 100, initially determined by a transfer process with detachment, was then submitted to RTA annealing.

The figure shows a superficial zone 101 having a thickness of less than 100 nm, in which the silicon structure is no longer crystalline.

It is this zone 101 of very narrow thickness which generates the pitting under consideration in this description.

This figure illustrates the different nature of the respective "pitting" of the state of the art and the "pitting" of the invention.

And in the remainder of this description, the term "pitting" is to be understood as specifically defined above and not as understood in the prior art (unless otherwise indicated).

The Applicant has therefore found that the application of RTA annealing to a wafer (in particular a

silicon wafer) promotes the onset of this pitting phenomenon.

This observation was particularly made with SOI wafers (Silicon-On-Insulator wafers) or SOA wafers (Silicon-On-Anything) derived from a method of SMARTCUT□ type.

And insofar as RTA annealing forms the ultimate step in wafer treatment to improve its surface condition, the pitting of a wafer surface after RTA annealing raises a problem since the "pitted" surface generated by RTA annealing will exist in the end product.

It is of course possible to contemplate re-treating the wafers derived from RTA annealing to correct this phenomenon and to endeavour to remove the pitting by polishing a sufficient thickness of pitted wafer.

But this would again give rise to the polishing disadvantages mentioned above (as with the teaching of document FR 2 797 713) and in this case the benefits connected with RTA annealing would be lost.

One purpose of the invention is to improve the methods for enhancing the condition of the free surface of a wafer in semiconductor material by RTA annealing.

More precisely, one purpose of the invention is to free such methods from the disadvantage related to the above-mentioned pitting.

And as already said, the invention applies more particularly to surfaces of wafers of SOI (or SOA) type derived from a transfer method with detachment (for example a method of SMARTCUT® type).

A further purpose of the invention is to put forward an alternative to methods comprising a polishing step.

To attain the objectives set forth above, the invention proposes a method for enhancing the condition of the free surface of a wafer in semiconductor material, said method comprising a rapid thermal annealing step to smooth said free surface, characterized in that before rapid thermal annealing the method comprises prior treatment of a superficial zone of the wafer to prevent the onset of pitting during rapid thermal annealing, and rapid thermal annealing can be conducted in a non-reducing atmosphere.

Some preferred, but not limitative, aspects of the method of the invention are the following:

- said prior treatment is high temperature annealing intended to reconstruct the superficial zone,
- said high temperature annealing is conducted in a neutral atmosphere,
- the temperature of said high temperature annealing lies between 600°C and 1300°C,
- the temperature of said high temperature annealing lies between 800°C and 1100°C,
- with said prior treatment it is possible to remove the disturbed part of the superficial zone,
- said prior treatment is chemical attack,
- said prior treatment is of wet etching or dry etching type,
- said prior treatment is sacrificial oxidation,
- the rapid thermal annealing step is followed by sacrificial oxidation.

And the invention also proposes a SOI or SOA structure obtained using a method according to one of the preceding claims.

Others aspects, purposes and advantages of the invention will be more clearly understood on reading the following description of preferred embodiments of the invention.

This description is made with reference to the preferred application of the invention, which concerns enhancement of the surface condition of a SOI or SOA wafer derived from a SMARTCUT® method. However, the wafer may be of different type.

One common characteristic of the different embodiments of the invention is that the surface of the wafer is prepared prior to a RTA annealing step which is intended to reduce the surface roughness of the wafer.

RTA annealing may in particular be conducted in an atmosphere of a hydrogen/argon mixture, or pure argon.

This RTA annealing may therefore be conducted in a non-reducing atmosphere.

It will be noted that this forms an additional difference compared with the teaching of documents EP 1 045 448 and EP 954 014 (cited for the record only as these documents are concerned by "pitting" such as defined in the state of the art and not by the "pitting" such as defined in this description).

It is also specified that EP 1 045 488 at all events does not teach treatment intended to prevent the onset of pitting, but rather curative treatment intended to cure existing defects.

It is also specified that EP 954 014 does not teach the application to a wafer of a treatment specifically intended to prevent the onset of any pitting before RTA annealing. The above document limits its teaching to the

application of RTA annealing. This also applies to the teaching of document FR 2 761 526.

If a wafer has been produced by splitting using the SMARTCUT® method, the surface of the wafer is the surface "as splitted"; this surface has irregularities which it is sought to reduce through RTA annealing.

According to one first embodiment of the invention, this preparation of the surface of the wafer is made by high temperature annealing in a neutral atmosphere, before RTA annealing.

The atmosphere of this prior annealing may be an argon or nitrogen atmosphere.

This prior annealing is applied to the wafer, whose surface to be treated is arranged such that it is exposed to annealing.

During this prior annealing, the temperature may lie between 600°C and 1300°C.

Preferably, this temperature lies between 800°C and 1100°C.

This prior annealing may also be conducted in a vacuum, the pressure possibly having any value of up to 1 atmosphere.

With said prior annealing it is possible to reconstruct the disturbed zone of the wafer surface and to remove the defects which would lead to pitting during RTA annealing.

These defects, particularly generated during splitting, were observed by the Applicant using an electron transmission microscope with which it is possible to visualize details in the order of magnitude of one atom, in the form of cavities in the superficial

zone of the wafer, on surfaces of wafers derived from a SMARTCUT□ method.

These cavities are grouped together in a superficial zone of the wafer having a thickness in the order of several dozen nm.

Owing to the presence of these cavities, the zone under consideration is a disturbed zone relative to the lower regions of the wafer whose crystalline structure is not disturbed.

These cavities may have a diameter in the order of 10 to 20 nm.

The prior annealing may be conducted in a conventional furnace (RTA annealing for surface smoothing being subsequently conducted in a specific furnace) or in the same furnace as RTA annealing.

According to a second embodiment of the invention, the prior treatment of the wafer consists of conducting chemical attack of the wafer surface.

This chemical attack may be of wet or dry etching type. In this case, the effect of the prior treatment is to remove the superficial zone of the wafer which contains the cavities mentioned above and which are the cause of the pitting phenomenon under RTA annealing.

In all the embodiments of the invention, the purpose of the treatment prior to RTA annealing is to treat the superficial zone whose structure is disturbed by the presence of cavities.

This treatment of the zone may consist of reducing or removing the zone cavities (this is the case in the first embodiment) or of directly attacking this zone to reduce/remove this zone itself (second embodiment and as will be seen later, the third embodiment also).

According to a third embodiment of the invention, the wafer is submitted to sacrificial oxidation prior to RTA annealing.

In this third embodiment, the effect of the prior treatment is again to reduce or to remove not only the cavities of the disturbed superficial zone containing the cavities, but to reduce or remove this disturbed superficial zone itself.

Therefore, by submitting the wafer to sacrificial oxidation before RTA annealing, this contributes towards reduction/removal of the disturbed zone (it is specified that it is also possible for this sacrificial oxidation to contribute towards reducing or removing the cavities of this zone).

In one preferred variant of this third embodiment, the sacrificial oxidation step is divided into an oxidation step and a deoxidation step, heat treatment being inserted between the oxidation step and the deoxidation step.

The oxidation step is preferably conducted at a temperature of between 700°C and 1100°C.

The oxidation step may be performed by dry route or by wet route.

By dry route, the oxidation step is performed for example by heating the wafer under gaseous oxygen.

By wet route, the oxidation step may be conducted for example by heating the wafer in an atmosphere containing water vapour.

Whether by dry route or wet route, according to conventional methods known to persons skilled in the art, the oxidation atmosphere may also contain hydrochloric acid.

The oxidation step leads to the formation of an oxide on the surface of the wafer.

The heat treatment step is conducted using any heat operation intended to improve the qualities of the material forming the superficial zone of the wafer.

This heat treatment may be conducted under constant or variable temperature.

In the latter case, heat treatment is performed for example with a gradual rise in temperature between two values or with cyclic oscillation between two values, etc..

Preferably, the heat treatment step is conducted at least in part at a temperature greater than 1000°C, and more particularly at around 1100-1200°C.

Preferably, the heat treatment step is conducted in a non-oxidizing atmosphere.

The atmosphere of the heat treatment may contain argon, nitrogen, hydrogen, etc.. or it may also contain a mixture of these gases. Heat treatment may also be conducted in a vacuum.

In this preferred variant of the third embodiment of the invention, the oxidation step is conducted before the heat treatment step.

It is to be noted that while consideration may already have been given to reducing pitting that is specifically due to the heat treatment step of such sacrificial oxidation, the problem which this invention sets out to solve which is to prevent pitting due to a subsequent RTA annealing step, has not been approached.

Moreover, it is recalled in this respect that the "pitting" which may be caused by sacrificial oxidation is "true" pitting (in which the holes are deeper than they

are wide) whereas the holes under consideration, whose onset it is sought to prevent subsequent to RTA annealing, are generally wider than they are deep.

According to one advantageous variant, the oxidation step starts with the start in temperature rise for heat treatment and ends before the latter ends.

With heat treatment it is possible to cure, at least in part, the defects that are generated during the preceding steps of the fabrication process and wafer treatment.

More particularly, heat treatment can be conducted for a time and at a temperature such that it can cure crystalline defects such as stacking faults, "HF" faults etc., generated in the superficial layer of the wafer during the oxidation step.

By "HF" defect is meant a defect whose presence is revealed by a decorative halo in a layer such as an oxide layer embedded in the thickness of the wafer, after treatment of the wafer in a hydrofluoric acid bath.

The deoxidation step is preferentially conducted in a solution.

This solution is for example a 10 % or 20 % hydrofluoric acid solution. A few minutes are sufficient to remove one thousand to a few thousand angstroms of oxide by immersing the wafer in this solution.

It is specified that in the different embodiments of the invention, the RTA annealing step may be followed by sacrificial oxidation such as described above (in this case, if the third embodiment of the invention is used, a two sacrificial oxidation operations will be conducted).

The addition of this sacrificial oxidation after RTA annealing makes it possible to thin the effective layer of the wafer to reduce it to a desired thickness.

And it is chiefly by acting on oxidation time that it is possible to determine the thickness to be removed from the effective layer of the wafer.

It will therefore be understood that with the invention, in each of its different embodiments, it is possible to treat the superficial zone highlighted by the Applicant (particularly in the case of SOI or SOA structures derived from SMARTCUT® methods) so as to prevent the subsequent onset of pitting during RTA annealing.

And in each of these embodiments, the invention brings major improvement in the surface morphology of wafers which have undergone RTA annealing; this annealing enhances the roughness of wafers and, on a finer scale, the invention brings the added advantage of preventing the onset of pitting.

CLAIMS

1. Method for enhancing the surface condition of wafers in semiconductor material, said method comprising a rapid thermal annealing step to smooth said free surface, characterized in that before rapid thermal annealing the method comprises prior treatment of a superficial zone of the wafer to prevent the onset of pitting during rapid thermal annealing, and the rapid thermal annealing can be conducted in a non-reducing atmosphere.

2. Method according to the preceding claim, characterized in that said prior treatment is high temperature annealing intended to reconstruct the superficial zone.

3. Method according to the preceding claim, characterized in that said high temperature annealing is conducted in a neutral atmosphere.

4. Method according to either of the two preceding claims, characterized in that the temperature of said high temperature annealing lies between 600°C and 1300°C.

5. Method according to the preceding claim, characterized in that the temperature of said high temperature annealing lies between 800°C and 1100°C.

6. Method according to claim 1, characterized in that with said prior treatment it is possible to remove the disturbed part of the superficial zone.

7. Method according to the preceding claim, characterized in that said prior treatment is chemical attack.

8. Method according to the preceding claim, characterized in that said prior treatment is of wet etching or dry etching type.

9. Method according to claim 6, characterized in that said prior treatment is sacrificial oxidation.

10. Method according to any of the preceding claims, characterized in that the rapid thermal annealing step is followed by sacrificial oxidation.

11. SOI or SOA structure obtained using a method according to any of the preceding claims.