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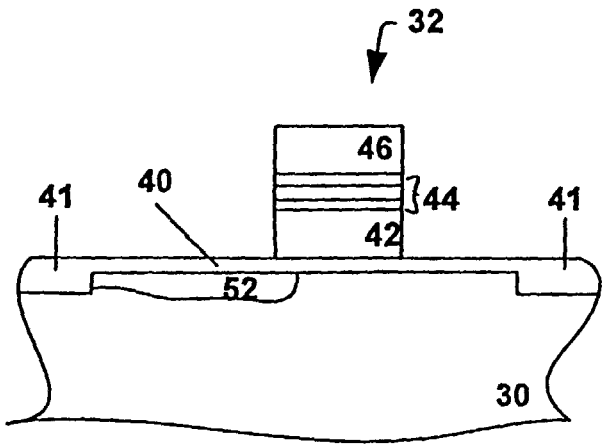
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(54) Title: LOWERED CHANNEL DOPING WITH SOURCE SIDE BORON IMPLANT FOR DEEP SUB 0.18 MICRON FLASH MEMORY CELL



(57) Abstract: For fabricating a flash memory cell on a semiconductor substrate, a channel dopant is implanted into the semiconductor substrate. The concentration of the channel dopang in the semiconductor substrate from the implantation process is less than about $4X10^{13}/Cm^2$. A source line mask is formed over the substrate, and the source link mask has an opening to expose a source line of the semiconductor substrate. A source line dopant of a first conductivity type is implanted into the exposed source line of the semiconductor substrate. The source line mask is then removed from the semiconductor substrate. A drain mask is formed over the semiconductor substrate, and the drain mask has an opening to expose a drain region of the semiconductor substrate. A drain dopant of a second conductivity type is implanted into the exposed drain region of the semiconductor substrate. A channel region of the semiconductor substrate is disposed between the source line and the drain region. The first conductivity type of the source line dopant is opposite to the second conductivity type of the drain dopang. In addition, a conductivity type of the channel dopant is same as the first conductivity type of the source line dopant. The source line dopant that diffuses from the source line into the channel region is used to alter a threshold voltage of the flash memory cell and/or to reduce short channel effects of the flash memory cell such that a lower concentration of the channel dopant is implanted or such that the implantation of the channel dopant is even eliminated, for improved reliability and performance of the flash memory cell.

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