LOW STRESS SIDEWALL SPACER IN INTEGRATED CIRCUIT TECHNOLOGY

BACKGROUND

TECHNICAL FIELD

The present invention relates generally to semiconductor technology, and more specifically to siliciding in semiconductor devices.

BACKGROUND ART

Electronic products are used in almost every aspect of life, and the heart of these electronic products is the integrated circuit. Integrated circuits are used in everything from airplanes and televisions to wristwatches.

Integrated circuits are made in and on silicon wafers by extremely complex systems that require the coordination of hundreds or even thousands of precisely controlled processes to produce a finished semiconductor wafer. Each finished semiconductor wafer has hundreds to tens of thousands of integrated circuits, each worth hundreds or thousands of dollars.

Integrated circuits are made up of hundreds to millions of individual components. One common component is the semiconductor transistor. The most common and important semiconductor technology presently used is silicon-based, and the most preferred silicon-based semiconductor device is a Complementary Metal Oxide Semiconductor (CMOS) transistor.

The principal elements of a CMOS transistor generally consist of a silicon substrate having shallow trench oxide isolation regions cordoning off transistor areas. The transistor areas contain polysilicon gates on silicon oxide gates, or gate oxides, over the silicon substrate. The silicon substrate on both sides of the polysilicon gate is slightly doped to become conductive. The lightly doped regions of the silicon substrate are referred to as "shallow source/drain junctions," which are separated by a channel region beneath the polysilicon gate. A curved silicon oxide or silicon nitride spacer, referred to as a "sidewall spacer", on the sides of the polysilicon gate allows deposition of additional doping to form more heavily doped regions of the shallow source/drain junctions, which are called "deep source/drain junctions". The shallow and deep source/drain junctions are collectively referred to as "S/D junctions."

The sidewall spacer also may be formed as a two-layer spacer comprising a first insulating layer, such as an oxide layer covered by a second insulating layer, such as a nitride layer. The two insulating layers then are processed to form a two-layer spacer.

To complete the transistor, a silicon oxide dielectric layer is deposited to cover the polysilicon gate, the curved spacer, and the silicon substrate. To provide electrical connections for the transistor, openings are etched in the silicon oxide dielectric layer to the polysilicon gate and the source/drain junctions. The openings are filled with metal to form electrical contacts. To complete the integrated circuits, the contacts are connected to additional levels of wiring in additional levels of dielectric material to the outside of the dielectric material.

In operation, an input signal to the gate contact to the polysilicon gate controls the flow of electric current from one source/drain contact through one source/drain junction through the channel to the other source/drain junction and to the other source/drain contact.

Transistors are fabricated by thermally growing a gate oxide layer on the silicon substrate of a semiconductor wafer and forming a polysilicon layer over the gate oxide layer. The oxide layer and polysilicon layer are patterned and etched to form the gate oxides and polysilicon gates, respectively. The gate oxides and polysilicon gates in turn are used as masks to form the shallow source/drain regions by ion implantation of boron or phosphorus impurity atoms into the surface of the silicon substrate. The ion implantation is followed by a high-temperature anneal above 700°C to activate the implanted impurity atoms to form the shallow source/drain junctions.

A silicon nitride layer is deposited and etched to form sidewall spacers around the side surfaces of the gate oxides and polysilicon gates. The sidewall spacers, the gate oxides, and the polysilicon gates are used as masks for the conventional source/drain regions by ion implantation of boron or phosphorus impurity atoms into the surface of the silicon substrate into and through the shallow source/drain junctions. The ion implantation is again followed by a high-temperature anneal above 700°C to activate the implanted impurity atoms to form the S/D junctions.

After formation of the transistors, a silicon oxide dielectric layer is deposited over the transistors and contact openings are etched down to the source/drain junctions and to the polysilicon gates. The contact openings are then filled with a conductive metal and interconnected by formation of conductive wires in other interlayer dielectric (ILD) layers.

As transistors have decreased in size, it has been found that the electrical resistance between the metal contacts and the silicon substrate or the polysilicon has increased to the level where it negatively impacts the performance of the transistors. To lower the electrical resistance, a transition material is formed between the metal contacts and the silicon substrate or the polysilicon. The best transition materials have been found to be cobalt silicide ($CoSi_2$) and titanium silicide ($TiSi_2$) although other materials also can be used.

The silicides are formed by first applying a thin layer of the cobalt or titanium on the silicon substrate above the source/drain junctions and the polysilicon gates. The semiconductor wafer is subjected to one or more annealing steps at temperatures above 800°C and this causes the cobalt or titanium to selectively react with the silicon and the polysilicon to form the metal silicide. The process is generally referred to as "siliciding." Since the shallow trench oxide and the sidewall spacers will not react to form a silicide, the silicides are aligned over the source/drain junctions and the polysilicon gates so the process is also referred to as "self-aligned siliciding," or "saliciding."

However, existing siliciding and saliciding have not succeeded in solving all the problems related to connecting metal contacts to silicon.

Solutions to these problems have been long sought but prior developments have not taught or suggested any solutions and, thus, solutions to these problems have long eluded those skilled in the art.

DISCLOSURE OF THE INVENTION

The present invention provides a method of forming an integrated circuit. A gate dielectric is formed on a semiconductor substrate, and a gate is formed on the gate dielectric. Source/drain junctions are formed in the semiconductor substrate. A sidewall spacer is formed around the gate using a low power plasma enhanced chemical vapor deposition (PECVD) process. A silicide is formed on the source/drain junctions and on the gate, and an interlayer dielectric is deposited above the semiconductor substrate. Contacts then are formed in the interlayer dielectric to the silicide. This method significantly lowers the electrical resistance between the contacts and the silicon or polysilicon greatly improving performance of the integrated circuit. The PECVD process preferably is performed within a low bias power range of about 100 watts to about 200 watts.

Certain embodiments of the invention have other advantages in addition to or in place of those mentioned above. The advantages will become apparent to those skilled in the art from a reading of the following detailed description when taken with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a view of a transistor in an intermediate stage of fabrication in accordance with the present invention;

FIG. 2 is the structure of FIG. 1 with a liner layer deposited thereon;

FIG. 3 is the structure of FIG. 2 during ion implantation to form shallow source/drain junctions;

FIG. 4 is the structure of FIG. 3 after formation of a sidewall spacer;

FIG. 5 is the structure of FIG. 4 during ion implantation to form deep source/drain junctions;

FIG. 6 is the structure of FIG.5 during the formation of silicide;

FIG. 7 is the structure of FIG. 6 after deposition of a dielectric layer over the silicide, the sidewall spacer, and shallow trench isolation;

FIG. 8 is the structure of FIG. 7 after formation of metal contacts; and

FIG. 9 is a simplified flow chart of the method of manufacturing the silicide in accordance with the present invention.

DETAILED DESCRIPTION OF THE INVENTION

In the following description, numerous specific details are given to provide a thorough understanding of the invention. However, it will be apparent to one skilled in the art that the invention may be practiced without these specific details. In order to avoid obscuring the present invention, some well-known configurations and process steps are not disclosed in detail. In addition, the drawings showing embodiments of the apparatus are semi-diagrammatic and not to scale and, particularly, some of the dimensions are for the clarity of presentation and may be exaggerated in the drawing FIGs. The same numbers will be used in all the drawing FIGs. to relate to the same elements.

The term "horizontal" as used herein is defined as a plane parallel to a substrate or wafer. The term "vertical" refers to a direction perpendicular to the horizontal as just defined. Terms, such as "on", "above", "below", "bottom", "top", "side" (as in "sidewall"), "higher", "lower", "over", and "under", are defined with respect to the horizontal plane.

Referring now to FIG. 1, therein is shown a transistor 100 in an intermediate stage of fabrication in accordance with the present invention.

To form the intermediate stage, a gate dielectric layer, such as silicon oxide, and a conductive gate layer, such as polysilicon, have been deposited on a semiconductor substrate 102 of a material such as silicon. The layers are patterned and etched to form a gate dielectric 104 and a gate 106. The semiconductor substrate 102 has been further patterned, etched, and filled with a silicon oxide material to form a shallow trench isolation (STI) 108.

Referring now to FIG. 2, therein is shown the structure of FIG. 1 having a liner layer 202 deposited thereon. The liner layer 202, generally of silicon oxide, covers the semiconductor substrate 102, the gate dielectric 104, the gate 106, and the STI 108. The liner layer 202 can be of an etch stop material or an implant-protection material.

Referring now to FIG. 3, therein is shown the structure of FIG. 2 during an ion implantation 302 to form shallow source/drain junctions 304 and 306.

The gate 106 and the gate dielectric 104 act as masks for the formation of shallow source/drain junctions 304 and 306 by the ion implantation 302 of boron (B) or phosphorus (P) impurity atoms into the surface of the semiconductor substrate 102. The ion implantation 302 is followed by a high-temperature anneal above 700°C to activate the implanted impurity atoms to form the shallow source/drain junctions 304 and 306.

Referring now to FIG. 4, therein is shown the structure of FIG. 3 after formation of a curved sidewall spacer 402. The sidewall spacer can be an insulating material selected from the group of an oxide, a nitride, and combinations thereof.

The liner layer 202, which protects from implant damage, has been removed and a sidewall spacer layer of an insulating material, such as a nitride or an oxide, has been deposited and etched to form the curved shape of the sidewall spacer 402. The sidewall spacer layer used to form the sidewall spacer 402 typically is deposited using a plasma enhanced chemical vapor deposition (PECVD) process.

PECVD processes use a number of radio frequency powers to direct ions of the material being deposited at the target surface, such as the semiconductor substrate102. It has been discovered that operating PECVD processes at low bias power reduces, or eliminates, the stress between the material used to form the sidewall spacer 402 and the semiconductor substrate 102. In accordance with the present invention, the PECVD process is performed at low bias power. It has been discovered that a PECVD process preferably within a low bias power range of about 100 watts to about 200 watts reduces the stress between the sidewall spacer 402 and the semiconductor substrate 102. Thus, performance of the transistor 100 is improved.

Referring now to FIG. 5, therein is shown the structure of FIG. 4 during an ion implantation 502 to form deep source/drain junctions 504 and 506.

The sidewall spacer 402, the gate 106, and the STI 108, act as masks for the formation of the deep source/drain junctions 504 and 506 by the ion implantation 502 of boron or phosphorus impurity atoms into the surface of the semiconductor substrate 102 and into and through the shallow source/drain junctions 304 and 306, respectively. The ion implantation 502 is again followed by a high-temperature anneal above 700°C to activate the implanted impurity atoms to form the source/drain junctions 504 and 506.

Referring now to FIG. 6, therein is shown a deposition process 602 used in the formation of silicide layers 604, 606, and 608 in accordance with the present invention. The silicide layers 604 and 608 are formed with the surface of the semiconductor substrate 102 over the deep source/drain junctions 504 and 506, respectively, and the silicide 606 is formed on the gate 106.

Generally, there are three ways in which to form a silicide. In one technique, the deposition process 602 deposits a pure metal on exposed silicon areas (both single crystalline and polycrystalline silicon). Thereafter, the metal is reacted with the silicon to form what is known as a first phase, metal-rich silicide. The non-reacted metal is then removed, and the pre-existing first phase product is then reacted again with the underlying silicon to form a second phase, silicon-rich silicide. In a second technique, the deposition process 602 involves co-evaporation of both metal and silicon onto the exposed silicon. Both metal and silicon are vaporized by, for example, an electron beam. The vapor is then drawn onto the wafer and across the silicon. In a third technique, the deposition process 602 involves co-sputtering both metal and silicon onto the silicon surface. Co-sputtering entails physically dislodging metal and silicon materials from a composite target or separate targets, and then directing the composite material onto the wafer.

Conventional salicidation processes have become problematic with modern semiconductor devices that have shallow source/drain junctions, e.g., junction depths on the order of 1000 Angstroms (Å). In particular, during such salicidation processes, some of the existing source/drain regions are consumed.

When cobalt is used as the refractory metal, it consumes about twice its thickness of silicon in the process of being converted to a metal silicide, e.g., a 100 Å layer of cobalt consumes about 103 Å of silicon. Such consumption acts to reduce the dopant present in the source/drain junctions and may adversely impact the electrical performance characteristics of the source/drain junctions, and ultimately, degrades the performance of the integrated circuit.

When the refractory metal is titanium, titanium silicide forms between metal contacts because the sidewall spacer becomes smaller with smaller integrated circuits thereby allowing a capacitive-coupled or fully conductive path between the polysilicon gate and the source/drain junctions, and similarly, degrades the performance of the integrated circuit.

While the present invention may be used with various refractory metal silicides, it has been found that nickel silicide has many desirable characteristics. However, in working with nickel silicide, it has been found to be difficult to form robust nickel silicide. It has been thought that thick silicides around 100 Å thick with rough surfaces would best protect the silicon substrate and provide good adhesion.

However, an ultra-uniform nickel can form extremely robust nickel silicide. By definition, an ultra-uniform silicide means a layer of silicide where there are no variations in thickness greater than about 3% of the overall thickness.

One example of forming ultra-uniform nickel ultra-uniform silicides 604, 606, and 608, is by depositing the nickel on the exposed silicon areas by a very low power vapor deposition process, where the very low power means a power level below 500 watts direct current and preferably between about 400 and 300 watts direct current.

In addition, an extra slow rate of metal deposition is preferred, which is defined to be below 7.0 Å per second and preferably between about 6.8 and 6.0 Å per second.

Still further, it is preferable that the silicide be deposited under these power levels and deposition rates to an ultra-thin thickness of not more than 50 Å thickness in order to provide an ultra-uniform, ultra-thin silicide. The deposited silicide metal is then converted to a silicide by an annealing process, such as a high-temperature anneal around 700°C.

The silicide 604, 606, 608 preferably is formed of a metal selected from the group consisting of cobalt, titanium, nickel, arsenic doped nickel, an alloy thereof, a compound thereof, and a combination thereof.

Referring now to FIG. 7, therein is shown the structure of FIG. 6 after deposition of a dielectric layer 702 over the silicide layers 604, 606, and 608, the sidewall spacer 402, and the STI 108.

In various embodiments, the dielectric layer 107 are of dielectric materials such as silicon oxide (SiO_x), tetraethylorthosilicate (TEOS), borophosphosilicate (BPSG) glass, etc. with medium dielectric constants from 4.2 to 3.9 or low dielectric constant dielectric materials such as fluorinated tetraethylorthosilicate (FTEOS), hydrogen silsesquioxane (HSQ), bis-benzocyclobutene (BCB), tetramethylorthosilicate (TMOS), octamethyleyclotetrasiloxane (OMCTS), hexamethyldisiloxane (HMDS), trimethylsilil borxle (SOB), diaceloxyditerliarybutosiloxane (DADBS), trimethylsilil phosphate (SOP), etc. with dielectric constants below 3.9 to 2.5. Ultra-low dielectric constant dielectric materials, having dielectric constants below 2.5 and which are available, include commercially available Teflon-AF, Teflon microemulsion, polimide nanofoams, silica aerogels, silica xerogels, and mesoporous silica. Stop layers and capping layers (where used) are of materials such as silicon nitride (Si_xN_x) or silicon oxynitride (SiON).

Referring now to FIG. 8, therein is shown the structure of FIG. 7 after formation of metal contacts 802, 804, and 806.

The metal contacts 802, 804, and 806 are respectively electrically connected to the silicide layers 604, 606, and 608, and respectively to the deep source/drain junction 504, the gate 106, and the deep source/drain junction 506.

In various embodiments, the metal contacts 802, 804, and 806 are of metals such as tantalum (Ta), titanium (Ti), tungsten (W), alloys thereof, and compounds thereof. In other embodiments, the metal contacts 802, 804, and 806 are of metals such as copper (Cu), gold (Au), silver (Ag), alloys thereof, and compounds thereof with one or more of the above elements with diffusion barriers around them.

Referring now to FIG. 9, therein is shown a simplified flow chart of a method 900 in accordance with the present invention. The method 900 includes: providing a semiconductor substrate in a step 902; forming a gate dielectric on the semiconductor substrate in a step 904; forming a gate on the gate dielectric in a step 906; forming source/drain junctions in the semiconductor substrate in a step 908; forming a sidewall spacer around the gate using a low power plasma enhanced chemical vapor deposition process in a step

910; forming a silicide on the source/drain junctions and on the gate in a step 912; depositing an interlayer dielectric above the semiconductor substrate in a step 912; and forming contacts in the interlayer dielectric to the silicide in a step 914.

While the invention has been described in conjunction with a specific best mode, it is to be understood that many alternatives, modifications, and variations will be apparent to those skilled in the art in light of the foregoing description. Accordingly, it is intended to embrace all such alternatives, modifications, and variations that fall within the spirit and scope of the included claims. All matters hither-to-fore set forth or shown in the accompanying drawings are to be interpreted in an illustrative and non-limiting sense.

CLAIMS:

1. A method (900) of forming an integrated circuit comprising:

providing a semiconductor substrate (102);

forming a gate dielectric (104) on the semiconductor substrate (102);

forming a gate (106) on the gate dielectric (104);

forming source/drain junctions (304) (306) in the semiconductor substrate (102);

forming a sidewall spacer (402) around the gate (106) using a low power plasma enhanced chemical vapor deposition process;

forming a silicide (604) (606) (608) on the source/drain junctions (304) (306) and on the gate (106) at a rate of deposition of a silicide metal of less than 7.0 Angstroms per second;

depositing an interlayer dielectric (702) above the semiconductor substrate (102); and

forming contacts (802) (804) (806) in the interlayer dielectric to the silicide (604) (606) (608).

2. The method as claimed in claim 1 wherein the rate of deposit is between 6 and 6.8 angstroms per second.

3. The method (900) as claimed in claim 1 wherein: forming the sidewall spacer (402) uses a low bias power plasma enhanced chemical vapor deposition process in the range of about 100 watts to about 200 watts.

4. The method (900) as claimed in claim 1 wherein: forming the silicide (604) (606)(608) uses an ultra-thin thickness of a silicide metal.

5. The method (900) as claimed in claim 1 wherein: depositing the interlayer dielectric (702) deposits a dielectric material having a dielectric constant of at least one of medium, low, or ultra-low dielectric constants.

6. The method (900) as claimed in claim 1 wherein: forming the contacts (802) (804)(806) to the silicide (604) (606) (608) uses at least one of tantalum, titanium, tungsten, copper, gold, silver, an alloy thereof, a compound thereof, or a combination thereof.

7. The method (900) as claimed in claim 1 wherein: forming the silicide (604) (606) (608) forms a nickel silicide.

8. The method (900) as claimed in claim 1 wherein: forming the silicide (604) (606)(608) forms a nickel silicide doped with arsenic.

9. The method (900) as claimed in claim 1 wherein: forming the silicide (604) (606) (608) uses a low bias power deposition technique.

10. The method (900) as claimed in claim 1 wherein: forming the silicide (604) (606)(608) forms a silicide of at least one of cobalt, titanium, nickel, an alloy thereof, a compound thereof, or a combination thereof.