Claims

1. In a phase locked loop (PLL) that generates an output frequency signal responsive to a reference frequency signal, the output frequency signal and the reference frequency signal each being characterized by phase and frequency, the PLL having a loop bandwidth, the PLL being susceptible to generating a phase or a frequency error in the output frequency signal responsive to a change in the loop bandwidth of the PLL, a method for suppressing the phase or the frequency error generated in the output frequency signal responsive to the change in the loop bandwidth of the PLL, the method comprising the steps of:

receiving a request to lock the frequency of the output frequency signal to a predetermined frequency;

adjusting the loop bandwidth of the PLL to a first loop bandwidth responsive to the step of receiving;

locking the frequency of the output frequency signal to substantially the predetermined frequency responsive to the step of adjusting the loop bandwidth of the PLL to the first bandwidth;

adjusting the loop bandwidth of the PLL to a second loop bandwidth, narrower than the first loop bandwidth, responsive to the step of locking;

opening the PLL for a period of time responsive to one of the step of locking and the step of adjusting the loop bandwidth of the PLL to the second loop bandwidth to permit the frequency error in the output frequency signal to reach a favorable level;

synchronizing the phase of the reference frequency signal and the phase of the output frequency signal after a lapse of the period of time to substantially eliminate the phase error in the output frequency signal; and

closing the PLL responsive to the phase of the reference frequency signal and the phase of the output frequency signal being synchronized;

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wherein the predetermined frequency of the output frequency signal before the PLL is opened is substantially the same frequency as the predetermined frequency of the output frequency signal after the PLL is closed.

2. A method according to claim 1 wherein the step of receiving comprises the step of:

receiving a request to change the frequency of the output frequency signal between a first frequency channel and a second frequency channel.

3. A method according to claim 1 wherein the steps of opening and closing further comprises disabling and enabling, respectively, a phase detector of the PLL.

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4. A method according to claim 1 wherein the period of time is predetermined.

5. A method according to claim 1 wherein the period of time is responsive to a duration of time during which the phase or the frequency error is generated in the output frequency signal.

6. In a phase locked loop (PLL) that generates an output frequency signal responsive to a reference frequency signal, the output frequency signal and the reference frequency signal each being characterized by phase and frequency, the output frequency signal being divided to produce a feedback signal, the PLL being susceptible to generating a phase or a frequency error in the output frequency signal responsive to a transient condition, an apparatus for suppressing the phase or the frequency error generated in the output frequency signal responsive to the transient condition, the apparatus comprising:

a signal detector coupled to receive an indication of the transient condition, an indication of the reference frequency signal, the feedback signal, and a reset signal, and operative to produce a control signal;

a time delay circuit coupled to receive the indication of the transient condition, the indication of the reference frequency signal, and the control signal, and operative to produce a timing signal;

a synchronization circuit coupled to receive the indication of the transient condition, the output frequency signal, the control signal, and the timing signal, and operative to produce the reset signal and a synchronization signal;

a logic circuit coupled to receive the synchronization signal and the feedback signal, and operative to produce a synchronized feedback signal;

a first gate circuit operative to transmit the indication of the reference frequency signal responsive to the control signal; and

a second gate circuit operative to transmit the synchronized feedback signal responsive to the control signal.

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7. An apparatus according to claim 6 wherein the transient condition is an indication to change a loop bandwidth of the PLL.

AN ERROR SUPPRESSING CIRCUIT AND METHOD THEREFOR FOR A PHASE LOCKED LOOP

Abstract of the Disclosure

An error suppressing circuit (301) and method therefor for a phase locked loop (PLL) (300). According to one embodiment of the present invention, a transient condition, for example, a bandwidth switch, in the PLL (300) is detected. The PLL (300) is opened for a period of time (509) responsive to detecting the transient condition. The phase of a reference frequency signal (115) and the phase of a output frequency signal (116 or 117) are synchronized after a lapse of the period of time (509). The PLL (300) is closed responsive to the phase of the reference frequency signal (115) and the phase of the output frequency signal (116 or 117) being synchronized. The present invention advantageously reduces the length of time it takes for the PLL (300) to correct for the phase and frequency error generated by the transient condition, and is capable of operating with various types of PLLs.

Fig. 3 accompanies this abstract.