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(54) **Title**: METHODS FOR CELL PHASING AND PLACEMENT IN DYNAMIC ARRAY ARCHITECTURE AND IMPLEMENTATION OF THE SAME

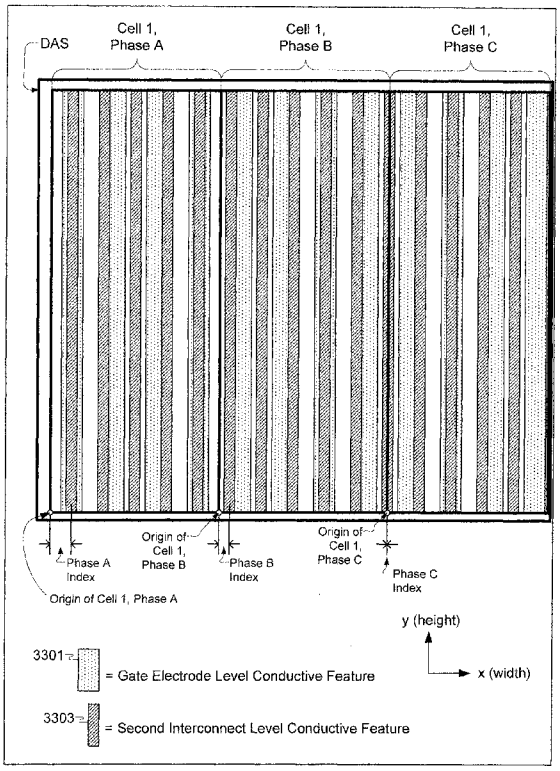

Fig. 7

(57) **Abstract**: A semiconductor chip is defined to include a logic block area having a first chip level in which layout features are placed according to a first virtual grate, and a second chip level in which layout features are placed according to a second virtual grate. A rational spatial relationship exists between the first and second virtual grates. A number of cells are placed within the logic block area. Each of the number of cells is defined according to an appropriate one of a number of cell phases. The appropriate one of the number of cell phases causes layout features in the first and second chip levels of a given placed cell to be aligned with the first and second virtual grates as positioned within the given placed cell.

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