



APPARATUS FOR REGION-BASED DETECTION OF INTERFERENCE AMONG
REORDERED MEMORY OPERATIONS IN A PROCESSOR

ABSTRACT

A computer processing system stores sequences of instructions in memory for execution by a processor unit (100). An out-of-order load instruction may be created, either statically or dynamically, by moving a load instruction from its original position to an earlier position in said sequence. Such an out-of-order load instruction identifies a location in memory from which to read a datum.

The present invention is an apparatus that maps the memory address space into regions, and detects the incorrect execution of a load operation performed earlier than a sequentially preceding store operation. The apparatus detects out-of-order load operations, uses a region-based mapping table (105) to track memory regions accessed, detects execution of store operations into regions accessed, and directs the processor (100) to execute a recovery sequence when interference among reordered operations is detected. The invention is applicable to static and dynamic reordering of memory operations.

Fig. 1