

## ABSTRACT OF THE DISCLOSURE

A semiconductor package may include a first semiconductor chip on and electrically connected to a wiring substrate, an intermediate layer on the first semiconductor chip and covering an entire surface of the first semiconductor chip, a second semiconductor chip on the intermediate layer and electrically connected to the wiring substrate, a mold layer on the wiring substrate and covering the first semiconductor chip and the second semiconductor chip, the mold layer including one or more inner surfaces defining a mold via hole that exposes a portion of a surface of the intermediate layer, an electromagnetic shielding layer on the one or more inner surfaces of the mold layer and further on one or more outer surfaces of the mold layer, and a thermal discharge layer on the electromagnetic shielding layer in the mold via hole, such that the thermal discharge layer fills the mold via hole.

FIG. 2