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THIN FILM TRANSISTOR

This application is divided from Application No. 8039608 (publication No. 2067353) which discloses and claims a thin film field effect transistor.

The present invention relates to a thin film, field effect transistor.

In this respect, reference is made to U.S. Patent No. 4,217,374 Stanford R. Ovshinsky and Masatsugu Izu entitled: AMORPHOUS SEMICONDUCTORS EQUIVALENT TO CRYSTALLINE SEMICONDUCTORS and U.S. Patent No. 4,226,898 Stanford R Ovshinsky and Arun Madan, of the same title.

Silicon is the basis of the huge crystalline semiconductor industry and is the material which is utilized in substantially all the commercial integrated circuits now produced. When crystalline semiconductor technology reached a commercial state, it became the foundation of the present huge semiconductor device manufacturing industry. This was due to the ability of the scientist to grow substantially defect-free germanium and particularly silicon crystals, and then turn then into extrinsic materials with p-type and n-type conductivity regions therein. This was accomplished by diffusing into such crystalline material parts per million of

donor (n) or acceptor (p) dopant materials introduced as substitutional impurities into the substantially pure crystalline materials, to increase their electrical conductivity and to control their being either of a p or n conduction type.

The semiconductor fabrication processes for making p-n junction cyrstals involve extremely complex, time consuming and expensive procedures as well as high processing temperatures. Thus, these crystalline materials used in transistors and other current control devices are produced under very carefully controlled conditions by growing individual single silicon or germanium crystals, where p-n junctions are required by doping such single crystals with extremely small and critical amounts of dopants. These crystal growing processes produce relatively small crystal wafers upon which the integrated circuits are formed.

In wafer scale integration technology the small area crystal wafer limits the overall size of the integrated circuit which can be formed thereon. In applications requiring large scale areas, such as in the display technology, the crystal wafers cannot be manufactured with as large areas as re-

quired or desired. The devices are formed, at least in part, by diffusing p or n-type dopants into the substrate. Further, each device is formed between isolation channels which are diffused into the substrate. Packing density (the number of devices per unit area of wafer surface) is also limited on the silicon wafers, because of the leakage current in each device and the power necessary to operate the devices, each of which generate heat which is undesirable. The silicon wafers do not readily dissipate heat. Also, the leakage current adversely affects the battery or power cell lifetime in portable applications.

In MOS type circuitry the switching speed is related directly to the gate length with the smallest length having the highest speed. The diffusion processes, photolithogrophy and other crystalline manufacturing processes limit how short the gate length can be made.

Further, the packing density is extremely important because the cell size is exponentially related to the cost of each device. For instance, a decrease in die size by a factor of two results in a decrease in cost on the order of a factor of six.

In summary, crystal silicon transistor and integrated circuit parameters which are not variable as desired, require large amounts of material, high processing temperatures, are only producible only on relatively small area wafers and are expensive and time consuming to produce. Devices based upon amorphous silicon can eliminate these crystal silicon disadvantages. Amorphous silicon can be made faster, easier, at lower temperatures and in larger areas than can crystal silicon.

Accordingly, a considerable effort has been made to develop processes for readily depositing amorphous semiconductor alloys or films each of which can encompass relatively large areas, if desired, limited only by the size of the deposition equipment, and which could be doped to form p-type and n-type materials to form p-n junction transistors and devices superior in cost and/or operation to those produced by their crystalline counterparts. For many years such work was substantially unproductive. Amorphous silicon or germanium (Group IV) films are normally four-fold coordinated and were found to have microvoids and dangling bonds and other defects which produce a

high density of localized states in the energy gap thereof. The presence of a high density of localized states in the energy gap of amorphous silicon semiconductor films resulted in such films not being successfully doped or otherwise modified to shift the Fermi level close to the conduction or valence bands making them unsuitable for making p-n junctions for transistors and other current control device applications.

In an attempt to minimize the aforementioned problems involved with amorphous silicon and germanium, W.E. Spear and P. G. Le Comber of Carnegie Laboratory of Physics, University of Dundee, in Dundee, Scotland did some work on "Substitutional Doping of Amorphous Silicon", as reported in a paper published in Solid State Communications, Vol. 17, pp. 1193-1196, 1975, toward the end of reducing the localized states in the energy gap in amorphous silicon or germanium to make the same approximate more closely intrinsic crystalline silicon or germanium and of substitutionally doping the amorphous materials with suitable classic dopants, as in doping crystalline materials, to make them extrinsic and of p or n conduction types.

The reduction of the localized states was accomplished by glow discharge deposition of amorphous silicon films wherein a gas silane (SiH_4) was passed through a reaction tube where the gas was decomposed by an r.f. glow discharge and deposited on a substrate at a substrate temperature of about 500-600°K (227-327°C). The material so deposited on the substrate was an intrinsic amorphous material consisting of silicon and hydrogen. To produce amorphous material a gas of phosphine (PH_3) for n-type conduction or a gas of diborane (B_2H_6) for p-type conduction were premixed with the silane gas and passed through the glow discharge reaction tube under the same operating conditions. The gaseous concentration of the dopants used was between about 5×10^{-6} and 10^{-2} parts per volume. The material so deposited included supposedly substitutional phosphorus or boron dopant and was shown to be extrinsic and of n or p conduction type.

While it was not known by these researchers, it is now known by the work of others that the hydrogen in the silane combines at an optimum temperature with many of the dangling bonds of the

silicon during the glow discharge deposition, to substantially reduce the density of the localized states in the energy gap toward the end of making the electronic properties of the amorphous material approximate more nearly those of the corresponding crystalline material.

D.I. Jones, W.E. Spear, P.G. LeComber, S. Li, and R. Martins also worked on preparing a Ge:H from GeH_4 using similar deposition techniques. The material obtained gave evidence of a high density of localized states in the energy gap thereof. Although the material could be doped the efficiency was substantially reduced from that obtainable with a Si:H. In this work reported in Philosophical Magazine B. Vol. 39, p. 147 (1979) the authors conclude that because of the large density of gap states the material obtained is ". . . a less attractive material than a-Si for doping experiments and possible applications."

The incorporation of hydrogen in the above silane method not only has limitations based upon the fixed ratio of hydrogen to silicon in silane, but, most importantly, various Si:H bonding configurations introduce new antibonding states which

can have deleterious consequences in these materials. Therefore, there are basic limitations in reducing the density of localized states in these materials which are particularly harmful in terms of effective p as well as n doping. The resulting density of states of the silane deposited materials leads to a narrow depletion width which in turn limits the efficiencies of devices whose operation depends on the drift of free carriers. The method of making these materials by the use of only silicon and hydrogen also results in a high density of surface states which affects all the above parameters.

After the development of the glow discharge deposition of silicon from silane gas was carried out, work was done on the sputter deposition of amorphous silicon films in the atmosphere of a mixture of argon (required by the sputtering deposition process) and molecular hydrogen, to determine the results of such molecular hydrogen on the characteristics of the deposited amorphous silicon film. This research indicated that the hydrogen acted as a compensating agent which bonded in such a way as to reduce the localized states in the

energy gap. However, the degree to which the localized states in the energy gap were reduced in the sputter deposition process was much less than that achieved by the silane deposition process described above. The above described p and n dopant materials also were introduced in the sputtering process to produce p and n doped materials. These materials had a lower doping efficiency than the materials produced in the glow discharge process. Neither process produced efficient p-doped materials with sufficiently high acceptor concentrations for producing commercial p-n junction devices. The n-doping efficiency was below desirable acceptable commercial levels and the p-doping was particularly undesirable since it increased the number of localized states in the band gap.

Various methods of fabrication and construction of thin film transistors and devices have been proposed wherein the various films of the transistor are made of different materials having different electrical characteristics. For example, thin film transistors have been proposed utilizing nickel oxide films, silicon films, amorphous silicon films and amorphous silicon and hydrogen films

formed from silane as above mentioned. Also, various geometrical configurations have been proposed such as a planar-MOS construction.

The prior deposition of amorphous silicon, which has been altered by hydrogen from the silane gas in an attempt to make it more closely resemble crystalline silicon and which has been doped in a manner like that of doping crystalline silicon, has characteristics which in all important respects are inferior to those of doped crystalline silicon. As reported by Le Comber and Spear and others referenced above, in the silane based transistor devices the leakage current may be as low as 10^{-11} amperes, the saturation current appears to be about 5×10^{-6} amperes, the device switching frequency appears to be about 10^4 Hz and the stability is poor since the material degrades with time.

It has been proposed to make a solar cell which is essentially a photosensitive rectifier utilizing an amorphous alloy including silicon and fluorine in the aforementioned U.S. Patent No. 4,217,374, issued 8/12/80 for Amorphous Semiconductor Equivalent to Crystalline Semiconductors, Stanford R. Ovshinsky and Masatsugu Izu and U.S.

Patent No. 4,276,898, issued 10/7/80 of the same title, Stanford R. Ovshinsky and Arun Madan.

According to the present invention there is provided a thin film, field effect transistor device including a source region, a drain region, a gate insulator, a thin-film deposited semiconductor alloy coupled to the source region, the drain region and the gate insulator, and a gate electrode in contact with the gate insulator, the device having a V-MOS like construction.

The field effect transistor can have various geometries including a V-MOS like construction of the invention and can be deposited on various substrates with an insulator between the active regions of the thin film, field effect transistor and a conducting substrate such as a metal. The transistors can be deposited on an insulator, a semiconductor, an insulated metal or an insulated semiconductor substrate. Because of the capability be formed on various substrates and a low leakage and operating current, the transistors also can be formed on top of one another, i.e., stacked.

The thin film, field effect transistor can have various desirable characteristics depending upon the particular geometry chosen and thickness of the film of amorphous silicon fluorine material chosen such as, for example, a DC saturation curent as low as 10^{-6} amperes and up to or greater than 10^{-4} amperes, an upper cut off frequency at least above 10 MHz, a high OFF resistance: ON resistance ratio of about 10^{7}, and a very low leakage current of about 10^{-11} amps or less. Further, the alloy does not degrade with time.

The invention also includes a field effect transistor as described above wherein said drain region layer is formed on at least a portion of said substrate; said source region, said amorphous semiconductor alloy

layer and said drain region forming a diagonal surface; and said gate insulator being disposed substantially parallel to said diagonal surface and separating said gate electrode from said amorphous semiconductor alloy layer for controlling the current conduction through said current conduction channel.

The invention will now be described by way of example, with reference to the drawings accompanying this specification in which:

Fig. 1 is a vertical sectional view of one embodiment of thin film deposited, field effect transistor having metal source and drain regions similar to a planar MOS-type transistor.

Fig. 2 is a schematic circuit diagram of the transistor shown in Fig. 1.

Fig. 3 is a vertical sectional view through a second embodiment of a thim film deposited, field effect transistor similar to the transistor shown in Fig. 1, having semiconductor source and drain regions.

Fig. 4 is a schematic circuit diagram of the transistor shown in Fig. 3.

Fig. 5 is a vertical sectional view of another embodiment of thin film deposited, field effect transistor similar to the transistor shown in Fig. 1, having metal source and drain reqions similar to a V-MOS-type transistor.

Fig. 6 is a schematic circuit diagram of the transistor shown in Fig. 5.

Fig. 7 is a vertical sectional view through a second embodiment of a thin film deposited, field effect transistor similar to the transistor shown in Fig. 5, having semiconductor source and drain regions.

Fig. 8 is a schematic circuit diagram of the transistor shown in Fig. 7.

Fig. 9 is a vertical sectional view through a thin film deposited, field effect transistor, similar in function to the transistors shown in Figs.1-8 but having a different gemoetrical construction.

Referring noW to the figures in greater detail, there is illustrated in Fig. 1 a thin film, field effect transistor 10 formed on a substrate 12 of

insulating material which could be a silicon material, a layer of polymer material or an insulator on top of a metal. Deposited on the substrate 12 is a thin alloy layer 14 including silicon and fluorine which can also contain hydrogen and which can be doped to form an N or P type alloy. On top of this alloy layer 14 is a layer or band 16 of insulating material such as a field oxide and spaced therefrom is another layer or band 18 of insulating material such as a field oxide.

A channel or opening 20 is formed, as by conventional photolithography techniques, between the two bands 16 and 18. A source metal conductor 22 is deposited over the band 16 with a portion thereof in contact with the alloy layer 14 to form a Schottky barrier contact at the interface between the source metal 22 and the amorphous alloy layer 14.

In a similar manner a conductor or layer 24 of drain metal is deposited over the insulating band 18 with a portion thereof in contact with the alloy layer 14 spaced from the source of metal 22. The interface between the drain metal 24 and the amor-

phous layer 14 creates another Schottky barrier contact. A gate insulator layer 26 of insulating material such as gate oxide or gate nitride 26 is deposited over the source metal 22 and drain metal 24 and in contact with the amorphous alloy layer 14 between the source and drain metal. On this layer 26 of gate insulating material is deposited a gate conductor 28 which can be made of any suitable metal such as aluminum or molybdenum. On the gate conductor another layer 30 of insulating material is deposited to passivate the device, which is identified as a field oxide.

The insulating layers 16 and 30 would be joined before the next adjacent transistor with the source 22 connected to an external conductor. The insulating layer 16 forms the insulator for the next device similar to the insulator 18 of the transistor 10 shown.

The gate insulator layer 26 and the bands 16 and 18 of insulating material referred to as being a field oxide can be made of a metal oxide, silicon dioxide or other insulator such as silicon nitride. The source metal 22 and drain metal 24 can be formed of any suitable conductive metal such as alumi-

num, molybdenum or a high work function metal such as gold, paladium, platinum or chromium. The gate insulator can be a nitride, silicon dioxide or silicon nitride material.

An alloy containing silicon and fluorine which can also contain hydrogen is utilized for forming the amorphous alloy layer 14. This alloy provides the desirable characteristics enumerated before which can be utilized for many different circuits. The alloy layer 14 is preferably made of $a\text{-}Si_a:F_b:H_c$ where a is between 80 and 98 atomic percent, b is between 1 and 10 atomic percent and c is between 1 and 10 atomic percent.

The alloy can be doped with a dopant from Group V or Group III of the Periodic Table materials in an amount constituting between 10 and 1000 parts per million (ppm). The dopant materials and amount of doping can vary.

The thickness of the alloy layer 14 of amorphous material can be between 100 and 5000 Angstroms, one thickness utilized being approximately 1000 Angstroms. The source metal 22 and the drain metal 24 can also have thicknesses ranging from 500

to 20,000 Angstroms with one utilized thickness being of approximately 2000 Angstroms. The gate conductor 28 although described as being made of metal, can be made of a doped semiconductor material if desired.

Depending upon the geometry of the various layers and thicknesses of the various layers, a field effect transistor can be constructed as described above wherein the leakage current is approximately 10^{-11} amperes thereby to provide a high OFF resistance and a DC saturation current of approximately 10^{-4} amperes.

In constructing the thin film, field effect transistor 10 shown in Fig. 1, the layers of material, and particularly the alloy layer 14, are deposited by various deposition techniques, preferably by glow discharge.

A conventional schematic gate (G), source (S) and drain (D) circuit diagram of the field effect transistor 10 is illustrated in Fig. 2.

Referring now to Fig. 3, there is illustrated a planar constructed thin film, field effect transistor 40 which, like the transistor 10, is formed on an insulated substrate layer 42. On top of the

substrate material 42 is deposited, such as by glow discharge, an alloy layer 44 including silicon and fluorine which also preferably includes hydrogen and can be of the N or P type. On this alloy layer 44 are deposited two layers of insulating material 46 and 48 which are referred to in Fig. 3 as being made of a field oxide with an opening 50 formed therebetween. Above the insulating layers 46 and 48 are deposited, respectively, a source alloy layer 52 and a drain alloy layer 54 which also include silicon and fluorine and preferably include hydrogen. The source 52 and the drain alloy 54 are N or P type amorphous alloys. An N-P or P-N junction is then formed at the interface where the layers 52 and 54 make contact with the alloy layer 44.

After depositing the layers 52 and 54, a gate insulator layer 56 referred to as a gate oxide 56 is deposited over the source region 52, the exposed portion of the amorphous layer 44 and the drain region 54. Then a gate conductor 58 is deposited over the gate insulator 46 and a passivating insulating layer 60 is deposited on top of the gate conductor 58, identified as a field oxide.

A conventional schematic gate (G), source (S) and drain (D) circuit diagram of the transistor 40 is illustrated in Fig. 4.

The difference between the transistor 40 and the transistor 10 is that the drain and source regions or conductors 52 and 54 of the transistor 40 are made of a semiconductor material and preferably an a-Si:F:H alloy.

In Fig. 5 there is illustrated a new V-MOS like construction illustrated in a thin film, field effect transistor 70 made in accordance with the teachings of the present invention. On a substrate layer 72 is first deposited a layer or band of drain metal 74 which has a central portion thereof cut or etched away. On top of the drain metal 74 is deposited a thin layer or band of amorphous alloy 76 which has a central portion cut or etched away aligned with the cut away portion of layer 74. Similarly, a layer of source metal 78 is deposited on the layer 76 and a corresponding central portion thereof is cut away. Alternately, all the layers can be etched in one step following the deposition of all the layers. Then a gate insulator 80 referred to as a gate oxide is deposited over the

source metal 78 and into the resulting central V-cut space 82 and onto the inclined edges of the layer portions 74, 76 and 78 and over the exposed substrate 72. Then a gate conductor 84 is deposited on the gate insulator 82 and a layer 86 of insulating material identified as a field oxide is deposited over the gate metal conductor 84 as a passivating layer.

This particular V-MOS like construction with the open space 80 has the advantage that a very short distance L is established between the source metal 74 and the drain metal 78 through the alloy layer 76. The layer thickness or distance L results in a high operating frequency, and a higher saturation current than the transistor configuration of Figs. 1 and 3. The leakage current may increase over the configuration of Figs. 1 and 3.

A conventional schematic gate (G), source (S) and drain (D) diagram of the transistor 70 is shown in Fig. 6.

In Fig. 7 is illustrated another V-MOS like thin film, field effect transistor 90 formed on a substrate 92 with alloy layers 94, 96 and 98 having silicon and fluorine (N or P type) deposited on the

substrate 92. The respective layers 94, 96 and 98 have a central portion 100 cut or etched away thereof. Then a gate insulator 102 identified as a gate oxide is deposited over the edge of the layer 98 and contacts the exposed edges of the layers 94, 96, and 98 and also the exposed portion of the substrate 92 as shown. A gate conductor 104 is deposited over the insulator layer 102 and lastly a layer 106 of insulating material, such as a field oxide, is deposited over the gate conductor 104. The transistor 90 operates utilizing the oppositely biased P-N junctions formed between layers 94 and 96 and between 96 and 98.

The transistor 90 is similar to the transistor 70 as shown in Fig. 5 except that the source region 98 and drain region 94 is made of a semiconductor alloy, such as a-Si:F:H. The V-MOS like construction of the invention illustrated by transistors 70 and 90 is advantageously utilized with any deposited semiconductor material, such as but not only a silicon alloy containing at least hydrogen as deposited from silane.

A conventional schematic circuit diagram of the transistor 90 is illustrated in Fig. 8.

Referring now to Fig. 9, there is illustrated therein another field effect transistor 110.

The transistor 110 is formed on a metal substrate 111 which has deposited thereon a thin layer of insulating material 112 which separates the active components of the transistor 110 from the metal substrate 111 and yet is thin enough so that heat generated in the transistor 110 can flow to the metal substrate which forms a heat sink therefor.

The thin film, field effect transistor 110 is formed by depositing a source conductor layer 114 made of metal or N or P type semiconductor alloy. A drain conductor 116 is deposited on the insulating layer 112 and also is made of a metal or a P or N type semiconductor alloy. On top of the conductors 114 and 116 is deposited an intrinsic or lightly doped alloy layer 118, such as the a-Si:F:H alloy previously described.

On top of the alloy layer 118 is deposited a gate insulator 120 which can be a silicon oxide or a silicon nitride. On top of the gate insulator 120 is deposited a gate conductor layer 122 which

can be a metal or semiconductor material. A passivating layer 124 is deposited over the gate conductor 122.

The various transistors 10, 40, 70, 90, and 110 can be formed in a matrix so that either the source or drain region extends as a Y axis conductor across the deposited substrate 112. Then, the drain or source region is deposited to form a segregated drain or source region which is then connected to an X axis conductor. Then the gate electrode is deposited so as to extend parallel to the Y axis to form a Y axis gate conductor. In this way, the field effect transistors 10, 50, 70, 90, and 110 can be utilized in conjunction with PROM devices to form the isolating device in a memory circuit therefor which comprises a memory region and the isolating device.

The thin film, field effect transistor of the present invention and the various specific embodiments thereof described herein provide a transistor which is very small and yet has very good operating characteristics as enumerated above. The top insulating layer of the transistors, such as 124 in Fig. 9, can be utilized to form the insulating

layer for another transistor to be formed thereon to provide a stacked transistor configuration and hence further increase the packing density of the devices. This is possible because the layers are deposited and because of the low operating and leakage current of the devices.

From the foregoing description it will be apparent that a thin film, field effect transistor incorporating an alloy layer of a Si:F:H therein

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has a number of advantages.

The planar structures of Figs. 1, 3 and 9 also can be formed in inverse order to that shown with the gate on the bottom. The Schottky barriers also can be an MIS (metal insulator semiconductor) contact. Also, the gate conductor in a device can be metal, polysilicon or doped semiconductor material with a different metal or semiconductor drain material, instead of both being of the same metal or semiconductor material.

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CLAIMS

1. A thin film, field effect transistor device including a source region, a drain region, a gate insulator, a thin-film deposited semiconductor alloy coupled to the source region, the drain region and the gate insulator, and a gate electrode in contact with the gate insulator, the device having a V-MOS like construction.

2. A transistor device according to claim 1, wherein the transistor includes two adjacent surfaces that form a V-type structure.

3. A transistor device according to claim 1 or claim 2, wherein the V-MOS like construction includes the source region and the drain region being positioned one above the other, and vertically arrayed with respect to a substrate, and the deposited semiconductor alloy extending between and in contact with the source region and the drain region, and wherein the gate insulator and the gate electrode are positioned to apply an electric field to the semiconductor alloy between the source region and the drain region to cause electrical conduction therebetween.

4. A transistor device according to any one of the preceding claims, wherein the deposited semiconductor is an n-type semiconductor.

5. A transistor device according to any one of the preceding claims, wherein the deposited semiconductor is an amorphous alloy.

6. A transistor device according to claim 5, wherein the alloy includes fluorine.

7. A transistor device according to claim 5 or claim 6, wherein the alloy includes silicon and hydrogen.

8. A transistor device according to claim 7, wherein the alloy has the empirical formula $Si_aF_bH_c$ where a is between 80 and 98 atomic percent, b is between 1 and 10 atomic percent, and c is between 1 and 10 atomic percent.

9. A transistor device according to any one of the preceding claims, wherein the drain, and the source regions are deposited materials.

10. A transistor device according to any one of the preceding claims, wherein the drain region is a p-type semiconductor.

11. A transistor device according to any one of the preceding claims, wherein the drain region is a metal or an amorphous alloy.

12. A transistor device according to any one of the preceding claims, wherein the source region is a p-type semiconductor.

13. A transistor device according to any one of the preceding claims, wherein the source region is a metal or an amorphous alloy.

14. A transistor device according to any one of the preceding claims, wherein the deposited semiconductor has a thickness of between 100 and 5000 angstroms.

15. A transistor device according to any one of the preceding claims, wherein the drain region has a thickness of between 500 and 20,000 angstroms.

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16. A transistor device according to any one of the preceding claims, wherein the source region has a thickness of between 500 and 20,000 angstroms.

17. A transistor device according to any one of the preceding claims, wherein the gate insulator comprises an oxide layer.

18. A transistor device according to claim 17, wherein the gate insulator is a deposited layer.

19. A transistor device according to any one of the preceding claims, wherein the drain region is deposited on the substrate, and extends as a y-axis conductor across the substrate to an adjacent thin film, field effect transistor device; an x-axis conductor extends from another adjacent thin film, vertical field effect transistor device to the source; and the gate electrode extends horizontally parallel to the y-axis to an adjacent, thin film, vertical field effect transistor.

20. A transistor device according to any one of the preceding claims, comprising a covering insulating layer and a further thin film, vertical field effect transistor device stacked on top of the first transistor device.

21. A method of forming a thin film, field effect transistor device that has a source region, a drain region, a gate insulator, a thin-film deposited semiconductor alloy coupled to the source region, the drain region and the gate insulator, and a gate electrode in contact with the gate insulator, the device having a V-MOS like construction, the method including the steps of depositing the drain region on a substrate; depositing the semiconductor alloy on

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top of the drain region; depositing the source region on top of the semiconductor alloy whereby to form a vertical array with respect to the substrate; removing a portion of the deposits whereby to expose edges of the drain region, the semiconductor alloy, and the source region; depositing the gate insulator over the exposed edges of the drain region, the semiconductor alloy, and the source region; and depositing the gate electrode over the gate insulator.

22. A method according to claim 21, wherein the drain region is an amorphous, p-type semiconductor alloy.

23. A method according to claim 22, wherein the drain region alloy includes silicon.

24. A method according to claim 22 or claim 23, wherein the drain region alloy includes fluorine.

25. A method according to any one of claims 21 to 24, wherein the drain region is deposited by glow discharge.

26. A method according to any one of claims 21 to 25, wherein the semiconductor alloy includes fluorine.

27. A method according to claim 26, wherein the semiconductor alloy includes silicon and fluorine.

28. A method according to any one of claims 21 to 27, wherein the semiconductor alloy is deposited by glow discharge.

29. A method according to any one of claims 21 to 28, wherein the source region is an amorphous, p-type semiconductor alloy.

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30. A method according to claim 29, wherein the source region alloy includes silicon.

31. A method according to claim 29 or claim 30, wherein the source region alloy includes fluorine.

32. A method according to any one of claims 21 to 31, wherein the source region is deposited by glow discharge.

33. A method according to any oine of claims 21 to 32, wherein the drain region is deposited to a thickness of between 500 and 20,000 angstroms.

34. A method according to any one of claims 21 to 33, wherein the semiconductor alloy is deposited to a thickness of between 100 and 5000 angstroms.

35. A method according to any one of claims 21 to 34, wherein the source region is deposited to a thickness of between 500 and 20,000 angstroms.

36. A method according to any one of claim 21 to 35, including the steps of depositing the drain region on the substrate as a y-axis conductor to an adjacent, thin film, vertical, field effect transistor device; depositing the source region as an x-axis conductor to another adjacent, thin film, vertical, field effect transistor device; and depositing the gate electrode horizontally parallel to the y-axis conductor to an adjacent, thin film, vertical, field effect transistor device; whereby to form a filed effect transistor matrix.

37. A method according to any one of claims 21 to 36, further including the steps of depositing an insulating layer on top of the gate electrode and the

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source region; and forming another thin film, vertical, field effect transistor device on top of the first transistor device, whereby to form a transistor stack.