

Description

This invention relates to video display systems, and more particularly to an apparatus for the on-line verification of the functionality of the various subsystems within the video display system.

In existing video display systems which include logic such as raster scan logic, counters, video memories, and shift registers, verification of the system while still on-line is accomplished by displaying a test pattern for the user to examine. It is left for the user to observe the test pattern and conclude that everything is functioning properly if the test pattern conforms to the expected display. This technique has worked whenever the user is looking for something wrong, but the first drawback is that the user has to think something is wrong. The present invention takes the user out of the loop for determining if something is wrong and verifies that the system is functioning properly on-line without interfering with the information being displayed, and without intervention by the user.

Accordingly, it is an object of the present invention to provide an apparatus for automatic on-line verification of a display system.

Accordingly the invention provides a display monitor comprising:

- a memory for storing display information;
- scan logic which accesses the memory at locations corresponding to the position of the scan beam of the monitor;
- a generator which receives display information from the memory and generates display control information; and
- a controller;

characterized in that

the memory has an inactive portion storing test data, and, during blank periods when the scan beam of the monitor is being repositioned to the start, the scan logic accesses the test data, the test data is passed through the generator to a test register, and the content of the test register is passed to the controller for checking against the expected result to thereby detect any malfunction of the display monitor.

A test pattern and video stimuli generator has been described by B.F. Wilensky and J.A. Maggi, entitled "Programmable Video Test Pattern Generator for Avionic CRT Displays", in 1982 IEEE International Automatic Testing Conf., Dayton, Ohio, 1982, pp. 526-535. A diagnostic system for a raster scan type display device is described in EP-(A) 132 925. They describe off-line testing. Test patterns are displayed during the useful, or visible, part of the raster. The testing occurs during a large number of successive raster scans, precluding use of the scan during such time. Test pattern data are stored in the portion of the display RAM which is

otherwise used for the storage of useful data to be displayed.

EP-(A) 132 925 offers a limited facility of on-line testing whereby the diagnostics is initiated by inserting a test pattern, which spans only eight pixels, at the end of a raster line of the visible display with possible impairment of the display picture in the on-line mode. It is, however, desirable to perform a more significant test of the display circuitry by testing a substantial portion of the raster, not just a few pixels at the end of one line. To accomplish this, the test pattern must be moved about the raster, and this moving is accomplished, according to the above mentioned EP-document, by vertical and horizontal smooth scrolling. Because the test pattern substantially interferes with the display picture in this scrolling mode if done on-line, an effective testing of the raster can only be done in an off-line mode.

An embodiment of the invention will now be described, by way of example, with reference to the drawings, in which:-

Figure 1 shows a display generator system;

Figure 2 shows the organization of a pixel memory of the system;

Figure 3 shows the layout of the CRT display for the system as it corresponds to the pixel memory organization;

Figure 4 shows some of the logic of the system utilized for displaying the information stored in the display memories;

Figure 5 is a partial functional logic block diagram of the raster scan logic of the system; and
Figure 6 is a block diagram of the apparatus added to the system to provide the on-line verification function.

INTRODUCTORY SUMMARY

The present system comprises apparatus for the on-line verification of the functionality of a video display system. A display generation system has a monitor for providing a visual display projected on a display surface by a scan beam associated with the monitor in response to position control signals and information control signals, and apparatus for on-line verification of the display generation system, comprising a memory with a display portion and an inactive portion, the display portion of the memory being utilized for storing display information to be displayed on the monitor, and the inactive portion being utilized for storing test data. Scan logic, connected to the memory, controls the monitor, including providing the position control signals to the monitor. The scan logic accesses the memory at a predetermined location corresponding to a predetermined position of the scan beam of the monitor. A generator, connected to the memory,

generates display control information from the display information, the display control information being coupled to the monitor to provide the information control signals to the scan beam thereby providing the visual display corresponding to the display information stored in the display portion of the memory. A register, connected to the generator, stores display control information generated from the test data stored in the inactive portion of the memory, the register being enabled by a control signal generated from the scan logic indicating the end of a display frame. The control signal corresponds in time to when the test data is being accessed by the scan logic. The scan logic is operative during a period of time that the monitor is blanked the scan beam of the monitor is being positioned to a beginning point of the visual display. An element, connected to the register, compares the display control information stored in the register corresponding to test data with an expected result, the comparison being performed during the period of time the monitor is blanked, thereby verifying on-line that the display generation system is functioning correctly and indicating an error when the match fails.

DETAILED DESCRIPTION

Figure 1 shows a display generation system. A graphics processor 10 includes a microprocessor and an associated RAM (not shown), and interfaces with a video display generator 11 which provides the necessary signals to generate displays on and to control a raster scan CRT monitor (not shown). The video display generator 11 includes various display and control memories 22 and 16, a cursor display logic 18, raster scan logic 20, colour lookup address generator logic 28, and a D/A converter 32. A pixel clock 24 is included to produce the required clocking signals for the video display generator. Latches and shift registers 26 and 30 are coupled to the display memory 22, and along with the clocking signals from the pixel clock 24, are shifted in a synchronous fashion to correspond to the scanning of the beam of the CRT monitor in order to produce the desired display.

There is also a loopback register 34 and a snapshot register 36. The loopback register 34 provides the capability for the graphics processor 10 to write various data patterns into the loopback register 34 and read the data back, to accomplish the verification of the data paths to and from the graphics processor 10. The snapshot register 36 stores an 8-bit output generated by the colour lookup address generator 28 based on a predetermined input, the predetermined input being known information stored in display memories 22 by the graphics processor 10. The 8-bit output stored in

snapshot register 36 is checked by the graphics processor 10 to determine if the correct output has been generated, thereby verifying several of the logic blocks within the video display generator 11. These added registers permit the video display generator 11 to be tested while continuing to provide operational displays on the CRT monitor, i.e., the testing is performed in an on-line mode.

The raster scan logic 20 generates all of the timing and sync signals for the raster scan CRT monitor (not shown) and the necessary timing and control signals for all accesses of the display memories 22. Counters (not shown) in the raster scan logic 20 determine which displayable element on the raster scan CRT monitor is currently being displayed and which address to access in the display memories 22.

The display memories 22 are organized in two different forms referred to as the picture element (pixel) memory 12 and the alphagraphic memory (also referred to as the graphic memory) 14, described in more detail later.

The cursor display logic 18 generates a visible cursor which can be positioned anywhere on the display under control of the graphic controller 10.

The colour lookup address generation logic 28 determines if the current displayable element is a pixel, alphagraphic, or cursor element (based on the display priority) and uses this determination along with the proper index bits (pixel or alphagraphic) to access a location in the colour lookup memory 16. The colour lookup memory 16, at locations having addresses corresponding to the colour addresses applied by the colour lookup address generator logic 28, has stored colour control signals which are used to control the intensity of the electron beams of the colour guns of a conventional colour CRT monitor (not shown) and which determine the colour and intensity of each picture element of the display array as it is scanned. Eight-bit bytes are stored in the colour lookup memory 16 at locations corresponding to the colour addresses applied. In synchronism with the scanning of each pixel of the display, the colour control signal is read out of colour lookup memory 16 and applied to D to A converters 32, which convert 6 of the 8 bits into analog signals for controlling intensity of the red, green, and blue electron beam guns of the conventional CRT monitor. In addition, two bits of the colour control signal are applied to a fourth D to A converter which converts these two bits into a monochrome analog signal which can be used to produce a permanent record of the raster display using conventional equipment, as is well known in the art.

Before proceeding with describing the on-line verification, an understanding of the operation of some of the components of the video display gen-

erator 11 is in order.

Figure 2 shows the organization of the pixel memory 12 and Figure 3 shows the layout of the CRT monitor display. The pixel memory 12 stores characteristic information for each pixel element; namely, planes 0-2 contains colour information, plane 3 contains intensity information, and plane 4 contains blink information. There is a similar organization for graphic memory 14. The active display area of the CRT monitor is divided into 640 horizontal elements and 448 vertical elements. The character size is a 5X9 character in an 8X16 character cell (i.e., 8 horizontal pixels by 16 vertical pixels). The pixel memory 12 contains five planes, p0, p1, p2, p3, and p4. Each plane is an 8-bit wide by 64K memory. Each location of each plane contains 8 bits of information relating to 8 corresponding picture elements. Hence, location 0 of the pixel memory 12 contains information relating to picture elements 0,0 to 0,7 of the display. The first bit of location 0 of pixel memory 12 contains information relating to picture element 0,0 of the display, the second bit of location 0 of pixel memory 12 contains information relating to picture element 0,1 of the display, etc.

In order to display the information of the display memory 22, it is necessary that the information in display memory 22 correspond to the position of the sweep of the CRT monitor (not shown). In raster scan CRT monitors, generally the sweep is a horizontal sweep from left to right, top to bottom, in which the sweep starts at location 0,0 and moves horizontally across the display to location 0,639. Thus, the information fetched from display memory 22 for display must correspond to the positioning of the sweep of the CRT monitor. Namely, location 0 of display memory 22 is fetched which corresponds to picture elements 0,0 to 0,7, then location 512 of display memory 22 is fetched which corresponds to the picture elements 0,8 to 0,15, then location 1024 is fetched, etc., up to location 40448 which corresponds to picture elements 0,632 to 0,639. The next line of the display (picture element 1, 0 to 1, 639) is scanned and the corresponding information is fetched from the display memory 22 at locations 1, 513, 1025, etc. When line 447 is completed, the display has been completed and the scanning is restarted at line 0.

The hole area in memory corresponds to the display area 448 - 511. Hence, locations 448 to 511, 960 to 1023, 1472 to 1535, etc., of display memory 22 have no corresponding active display area. The fetch of the information from display memory 22 is performed by logic in the raster scan logic 20. By adding 1 to bit 9 (i.e., to the 512 bit position) of an address counter, the correct addressing scheme is generated corresponding to the

CRT beam as it is swept across a horizontal line. By allowing the hole area in memory, the implementation of incrementing the counter of the raster scan logic is simplified. The area of the display from 640 to 1023 also corresponds to a memory hole area from locations 40960 to 64K (i.e., 65535). The apparent inefficient use of memory is more than negated by the ease of implementing an addressing scheme corresponding to the display layout.

Although a line by line scanning of the display area has been described, alternative vertical scanning techniques are well known. Interlace scanning is implemented with the organization of the display memory 22 just described. The raster scan logic is implemented such that the low order bit position of the counter for accessing the display memory 22 is alternately set between a 1 and a 0 on successive vertical scans as will be described hereinafter.

The alphagraphic memory 14 also corresponds to a display which is 640 horizontal elements and 448 vertical elements. The graphic memory 14 consists of 2 memory planes with each plane organized such that each 8-bit byte corresponds to 8 horizontal elements by 1 vertical element. In a first plane, denoted a dot memory, each bit determines if the picture element is a foreground or background colour. In a second plane, denoted the behavior memory, each 8 bit location determines the behavior index of an entire associated location in the dot memory, and the display priority between the pixel memory 12 and the alphagraphic memory 14. Of the 8 bits, a behavior index is 6 bits and a display priority is 2 bits. The 6 bits representing the behavior index and the 1 bit identification of each foreground or background colour results in a 7 bit value used as an index into the colour lookup memory 16. The 2 priority bits determine the priority of the pixel display with respect to the alphagraphic display.

Figure 4 shows some of the logic of the video display generator 11 utilized for displaying the information stored in the display memories 22. The raster scan logic 20 reads the alphagraphic memory 14 and the pixel memory 12 at the same location; in the example shown in Figure 5, location 0 is being read. The 8 bits from the dot memory 14' are loaded into a shift register 26B and the 8 bits from location 0 of the behavior memory 14" are loaded into a latch 26A. Likewise, the contents of location 0 of each plane of the pixel memory 12 are loaded into a corresponding shift register. Thus, the 8 bits of location 0 from plane 0 are loaded into shift register SR-0, the 8 bits from location 0 of plane 1 are loaded into SR-1, etc., up to the 8 bits from location 0 of plane 4 which are loaded into SR-4.

All of the shift registers are shifted such that

the colour lookup address generation logic 28 processes the information related to picture element 0,0 from both the pixel memory 12 and the dot memory 14'. Processing is performed to correspond to the information contained in latch 26A. At this point in time the sweep of the CRT monitor is at location 0,0 of the display. Synchronized by the clocking signal, the display moves to the next position, i.e., picture element 0,1 of the display and likewise the information corresponding to location 0,1 is shifted into the colour lookup address generation logic 28 from the shift registers 30 and the shift register 26B. Again, this information is processed by the colour lookup address generation logic 28 as defined by the information latched in latch 26A, which is valid for the 8 bits of location 0. The process continues until the sweep of the CRT monitor has displayed the 8 picture elements of a horizontal line. The next element to be displayed is location 0,8 which corresponds to address 512. The raster scan logic 20 causes a read of location 512 from the graphic memory 14 and the pixel memory 12 into the shift registers and latch and the above process continues until the entire line is displayed, and then continues as described above until the entire display area has been processed for display.

Figure 5 is a partial functional logic block diagram of the raster scan logic 20. The counters shown in Figure 5 are part of the raster scan logic 20 which is verified by the verification apparatus, and include a divide-by-eight circuit 42 for the pixel clock signal, horizontal address counter 44, vertical address counter 46, an odd/even frame counter 48, an end-of-line detector 50, and an end-of-frame detector 52. The outputs of the horizontal address counter 44, vertical address counter 46, and odd/even frame counter 48 are coupled to the display memory 22 for addressing the display memory. The outputs of the horizontal address counter 44, the vertical address counter 46, and the odd/even frame counter 48, make up the display memory address. The output of the odd/even frame counter 48 makes up the least significant bit portion, the 8 bits outputted from the vertical address counter 46 makes up the next least significant bits of the memory address, and the 7 bits outputted from the horizontal address counter make up the most significant bit portion of the display memory address.

The pixels are read from the display memory 22 in groups of eight pixels at a time and loaded into shift registers and latches 26, 30 as described above, therefore requiring the pixel clock signal to be divided by eight when clocking the horizontal address counter 44. The horizontal address counter 44 is allowed to continue to count during horizontal retrace, the count being used for generating syn-

chronizing signals. The retrace count for the horizontal address counter 44 is 16 cells, which results in a total count of 768 for each horizontal line. When the end-of-line detector 50 determines that the horizontal address counter 44 is at the end of a current scan line, the end-of-line detector 50 sends an end-of-line signal back to the horizontal address counter 44 which resets the counters to a value of -14. While the counters are incrementing from -14 to 0 the display is blanked and the video display generator 11 is generating horizontal synchronization signals to the CRT monitor (not shown). Also, when the end-of-line detector 50 sends the end-of-line signal, the vertical address counter 46 is incremented.

The video display generator 11 is an interlace system, two frames of the display comprising a single complete display. One frame is all of the even horizontal lines of the display and the other frame is all of the odd horizontal lines of the display. During successive vertical scans of the CRT monitor, the frames are alternated as a result of the odd/even frame counter 48. The vertical address counter 46 is similar in operation to the horizontal address counter 44 except that the vertical address counter 46 is only incremented at the end of each horizontal scan line. When the end-of-frame detector 52 senses that the display is at the end of the frame an end-of-frame signal is generated, the vertical address counter 46 is reset to -16, and the odd/even frame counter 48 is toggled. While the vertical address counter 46 is counting from the count of -16 to 0, the CRT display is blanked and the video display generator 11 is generating the synchronization signals to the CRT monitor.

What has been described thus far is the normal operation of the video display generator 11. Figure 6 shows the apparatus added to the video display generator 11 to provide the on-line verification function. In order to permit the on-line verification of the video display generator 11, the end-of-frame signal is utilized as a vertical retrace interrupt signal back to the microprocessor of the graphics processor 10. Referring back to Figures 2 and 3, when the video sweep has reached the point 447, 639, the odd frame is completed and the vertical retrace signal is generated (point 446, 639 is the last point for the even frame). Since the horizontal address counter 44 and the vertical address counter 46 continue to count during retrace, the logic will address location 449 of the display memories 22 which corresponds to the points 449,0 to 449,7 (for the even frame the location to be addressed and accessed is location 448 which corresponds to points 448,0 to 448,7). Although locations 448,0-7 and 449,0-7 are in the "hole" area of display memory 22 (i.e., there is no corresponding active dis-

play area for these locations), test data is prestored into locations 448 and 449. Since the logic of the video display generator 11 is active, the counters of raster scan 20 are counting during the retrace period, and the locations in the hole area are being accessed.

Referring back to Figure 6, the end-of-frame signal (or vertical retrace interrupt which is active for 8 pixel times, i.e., 8 bits) enables a serial-to-parallel shift register 39 during a portion of the retrace period while location 449 is being addressed (location 448 for the even frame). The address information contained on the data lines from colour lookup address generator 28 corresponds to the 8 bits of address information generated by the counters and shift registers of the logic of video display generator 11 based on the test data stored in location 449 (location 448 for the even frame retrace). An interrupt routine in the graphics processor 10 sets up the loopback register 34 such that a MUX 37 sequentially inputs the generated address information from the colour lookup address generator 28 into the serial-to-parallel shift register 39. When the shift register 39 is full the data is read by the graphics processor 10 and compared to an expected result. The test data stored in the display memory 22 is varied by the graphics processor 10 to different patterns to ensure all the logic of the video display generator 11 is adequately tested. Since the colour lookup memory is a RAM, the colour lookup memory 16 can be tested by reading and writing into the RAM. The loopback register 34 is utilized to verify the data paths from the graphics processor 10 to the video display generator 11 and can be done in an off-line as well as an on-line mode. Thus, all the logic of the video display generator 11 can be verified on-line up to the inputs to the D to A converters 32. If the data read from the shift register 39 does not contain the expected result an error signal can be raised, or a number of retries can be executed until a hard failure is signalled, the determination of the hard failure being a design choice.

In the present system, eight vertical frames are necessary to verify the test word addresses generated by the colour lookup address generator 28. The choice to capture the generated addresses in the above described manner results in less hardware and is a matter of design choice. Thus, for example, in the present system, during the first retrace, loopback register 34 is set up to select bit 0 of the output of colour lookup address generator 28, and the results stored in the shift register 39 are for the first pixel, bit 0, second pixel, bit 0, etc., to the eighth pixel, bit 0. For the next vertical retrace, loopback register is set up by graphic controller 10 to read bit 1, etc., until the eighth retrace when bit 7 for all eight pixels of the test

word are read.

Claims

- 5 1. A display monitor comprising:
 - a memory (22) for storing display information;
 - scan logic (20) which accesses the memory at locations corresponding to the position of the scan beam of the monitor;
 - a generator (16, 26, 28, 30, 32) which received display information from the memory and generates display control information; and
 - a controller (10);characterized in that
- the memory has an active portion (HOLE) storing test data, and, during vertical blank periods when the scan beam of the monitor is being repositioned to the start, the scan logic accesses the test data, the test data is passed through the generator to a test register (36), and the content of the test register is passed to the controller (10) for checking against the expected result to thereby detect any malfunction of the display monitor.

Revendications

- 30 1. Moniteur d'affichage comprenant :
 - une mémoire (22) pour mémoriser une information d'affichage;
 - une unité logique de balayage (20) qui accède à la mémoire à des emplacements correspondant à la position du faisceau de balayage du moniteur;
 - un générateur (16,26,28,30,32) qui reçoit une information d'affichage de la part de la mémoire et produit une information de commande d'affichage; et
 - un dispositif de commande (10),

caractérisé en ce que

la mémoire possède une partie active (HOLE) mémorisant des données de test, et pendant des périodes de suppression verticale, lorsque le faisceau de balayage du moniteur est repositionné au départ, l'unité logique de balayage accède aux données de test, les données de test sont transmises par le générateur à un registre de tests (36) et le contenu du registre de tests est transféré au dispositif de commande (10) pour l'exécution d'un contrôle par rapport au résultat attendu, afin de détecter ainsi tout défaut de fonctionnement du moniteur d'affichage.

Patentansprüche

play area for these locations), test data is prestored into locations 448 and 449. Since the logic of the video display generator 11 is active, the counters of raster scan 20 are counting during the retrace period, and the locations in the hole area are being accessed.

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- 25 repositioned to the start, the scan logic ac-
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 - une unité logique de balayage (20) qui
 - un générateur (16,26,28,30,32) qui reçoit
 - un dispositif de commande (10),caractérisé en ce que
- 35 la mémoire possède une partie active
- 40 (HOLE) mémorisant des données de test, et
- 45 pendant des périodes de suppression verticale,
- lorsque le faisceau de balayage du moniteur
- est repositionné au départ, l'unité logique de
- balayage accède aux données de test, les
- données de test sont transmises par le généra-
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- du registre de tests est transféré au dispositif
- de commande (10) pour l'exécution d'un
- contrôle par rapport au résultat attendu, afin
- 55 de détecter ainsi tout défaut de fonctionnement du
- moniteur d'affichage.

Patentansprüche

1. Anzeigevorrichtung, die aufweist:

- einen Speicher (22) zum Speichern von Anzeigeeinformation;
- eine Abtastlogik (20), die auf den Speicher an Orten zugreift, die der Position des Abtaststrahls der Vorrichtung entsprechen;
- einen Generator (16, 26, 28, 30, 32), der Anzeigeeinformation von dem Speicher empfängt und Anzeigesteuerinformation erzeugt; und
- eine Steuerung (10),



dadurch gekennzeichnet,

daß der Speicher einen aktiven Teil (HOLE) aufweist, der Testdaten speichert, und daß, während vertikaler Austastperioden, wenn der Abtaststrahl der Vorrichtung wieder an den Anfang positioniert wird, die Abtastlogik auf die Testdaten zugreift, die Testdaten durch den Generator zu einem Testregister (36) geführt werden, und daß der Inhalt des Testregisters zu der Steuerung (10) geführt wird zum Prüfen gegenüber dem erwarteten Ergebnis, um dadurch irgendeinen Fehler der Anzeigevorrichtung zu erfassen.

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