CLAIMS

1. An apparatus, comprising:

a first capacitor including a first plate, a second plate, and a ferroelectric material disposed between the first and second plates, the first plate coupled to a plate line structure;

a second capacitor including a first plate, a second plate, and a ferroelectric material disposed between the first and second plates, the first plate coupled to the plate line structure;

a first transistor vertically displaced relative to the first capacitor and coupled to the second plate of the first capacitor;

a second transistor vertically displaced relative to the second capacitor and coupled to the second plate of the second capacitor; and

a shared digit line coupled to a first source/drain region of the first transistor and a first source/drain region of the second transistor, wherein the second plate of the first capacitor is coupled to a second source/drain region of the first transistor, and wherein the second plate of the second capacitor is coupled to a second source/drain region of the second transistor.

2. The apparatus of claim 1, wherein the second plate of the first capacitor is a first container-shaped outer plate configured to fit the first plate of the first capacitor, and wherein the second plate of the second capacitor is a second container shaped outer plate configured to fit the second plate of second capacitor.

3. The apparatus of claim 1, further comprising:

a memory controller configured to activate the shared digit line.

4. The apparatus of claim 3, wherein the memory controller comprises a biasing component configured to apply the respective voltages to the shared digit line.

5. The apparatus of claim 1, wherein the first transistor includes a first semiconductor pillar extending upwardly from the shared digit line, the first semiconductor pillar including the first source/drain region of the first transistor.

6. The apparatus of claim 5, wherein the first semiconductor pillar further includes a third source/drain region of the first transistor, the third source/drain region coupled to the second plate of the first capacitor.

7. The apparatus of claim 1, wherein the second transistor includes a second semiconductor pillar extending downwardly from the shared digit line, the second semiconductor pillar including the second source/drain region of the second transistor.

8. The apparatus of claim 7, wherein the second semiconductor pillar further includes a fourth source/drain region of the second transistor, the fourth source/drain region coupled to the second plate of the second capacitor.

9. The apparatus of claim 1 wherein the first transistor and the second transistor are vertically displaced relative to one another.

10. The apparatus of claim 1 wherein the first and second transistors include respective gates coupled to respective word lines.

11. An apparatus, comprising:
a first memory cell; and
a second memory cell;
wherein each memory cell comprises:
a first transistor;
a first ferroelectric capacitor including a ferroelectric material, coupled to the first transistor and vertically stacked relative to the first transistor;
a second transistor; and
a second ferroelectric capacitor coupled to the second transistor and vertically stacked relative to the second transistor; and
a plate line structure shared by the first and second memory cells.

12. The apparatus of claim 11, wherein the first and second memory cells are laterally displaced relative to one another.

13. The apparatus of claim 11, further comprising:
a first digit line shared by the first and second memory cells; and
a second digit line shared by the first and second memory cells.

14. A method of accessing a memory cell, comprising:
activating first and second transistors of the memory cell;

applying a voltage to a plate line coupled to first and second ferroelectric capacitors, the first ferroelectric capacitor coupled to the first transistor and vertically displaced relative to the first transistor and the second ferroelectric capacitor coupled to the second transistor and vertically displaced relative to the second transistor; and

comparing a first voltage developed at a first digit line coupled to the first ferroelectric capacitor to a second voltage developed at a second digit line coupled to the second ferroelectric capacitor.

15. The method of claim 14, further comprising:

determining a stored state of the memory cell based the comparison of the first voltage developed at the first digit line coupled to the first ferroelectric; capacitor to the second voltage developed at the second digit line coupled to the second ferroelectric capacitor.

16. The method of claim 15, wherein determining the stored state of the memory cell comprises:

detecting a high logic state when the first voltage developed at the first digit line is higher than a reference voltage; and

detecting a low logic state when the first voltage developed at the first digit line is lower than the reference voltage.

17. The method of claim 14, wherein comparing the first voltage developed at the first digit line coupled to the first ferroelectric capacitor to the second voltage developed at the second digit line coupled to the second ferroelectric capacitor comprises amplifying a difference between the first voltage developed at the first digit line and the second voltage developed at the second digit line.

18. The method of claim 14, further comprising:

discharging a first stored voltage at the first ferroelectric capacitor onto the first digit line or a second stored voltage at the second ferroelectric capacitor onto the second digit line.