[0005] A carrier ring of the pedestal typically contacts the substrate in a narrow band along a radially outer edge of the substrate. Typically, the narrow band has a width of 1.0 to 1.5 mm. Minimum contact area (MCA) pins are used to support a center region of the substrate. The MCA pins at the center of the substrate lift the center of the substrate higher than the narrow band supporting an outer edge of the substrate to create a substrate bowing condition. In other words, top surfaces of the MCA pins are raised higher than a planar surface defined by the narrow band. The substrate edge contacts the carrier ring with tangent line or line contact. This requires precise alignment of the substrate and the pedestal during delivery and processing. Due to the precision required and the limits of 'on-site' setup, the pins and the carrier ring do not typically block deposition on a back side of the substrate sufficiently. Since the amount of contact with the backside edge of the substrate is also limited, this approach is also less tolerant with respect to off-center substrate placement.

SUMMARY

[0006] A pedestal for a substrate processing system includes a pedestal body including a substrate-facing surface. An annular band that is arranged on the substrate-facing surface is configured to support a radially outer edge of the substrate. A cavity is defined in the substrate-facing surface of the pedestal body and is located radially inside of the annular band. The cavity creates a volume between a bottom surface of the substrate and the substrate-facing surface of the pedestal body. A plurality of vents pass through the pedestal body and are in fluid communication with the cavity to equalize pressure on opposing faces of the substrate during processing.

[0007] In other features, the band has a width in a range from 4 mm to 12 mm. The band has a width in a range from 5 mm to 9 mm. The band has a width in a range from 6 mm to 7 mm. The band has a surface roughness (Ra) in a range from 2 to 32. The surface roughness (Ra) in a range from 2 to 24. The surface roughness (Ra) in a range from 2 to 16.

[0008] In other features, the plurality of vents include a first vent portion extending radially inwardly from a radially outer side of the pedestal body and a second vent portion extending from a radially inner edge of the first vent portion to the cavity.

[0009] In other features, the plurality of vents include a first vent portion extending axially from a bottom side of the pedestal body towards the cavity and a second vent portion including a plurality of holes connecting the first vent portion to the cavity.

[0010] In other features, the band is made of a material selected from a group consisting of a dielectric coating formed on a surface of a conductive material, an uncoated conductive material, an uncoated metal, and an uncoated dielectric material.

[0011] In other features, a ring is arranged radially outside of the substrate and the band. A top surface of the ring is arranged above a top surface of the substrate. The ring is made of a dielectric material.

[0012] In other features, the dielectric material is selected from a group consisting of alumina, aluminum nitride, sapphire, quartz, and silicon oxide. A ring includes a radially inner surface arranged radially inside of and below the substrate and a radially outer surface arranged radially outside of the substrate. A top surface of the ring is parallel to a top surface of the substrate. The ring is made of a dielectric material.

[0013] In other features, the dielectric material is selected from a group consisting of alumina, aluminum nitride, sapphire, quartz, and silicon oxide. The pedestal body includes an annular notch around a radially outer edge thereof. A ring is arranged in the annular notch. A bottom surface of the ring lies below a bottom surface of the substrate. A top surface of the ring lies below a top surface of the substrate. The ring is made of a dielectric material.

[0014] In other features, the dielectric material is selected from a group consisting of alumina, aluminum nitride, sapphire, quartz, and silicon oxide.

[0015] In other features, a plurality of pins is arranged in the cavity to support a center of the substrate. A top surface of the pins is one of below, parallel to or above a top surface of the annular band during processing.

[0016] In other features, a plurality of projections supports a center of the substrate. A top surface of the projections is one of below, parallel to or above a top surface of the annular band. A backside surface of the substrate along the radially outer edge of the substrate is parallel to the band during processing.

[0017] A substrate processing system includes a processing chamber and the pedestal. The pedestal is arranged in the processing chamber. An RF generator is arranged in the processing chamber.

[0018] In other features, a plurality of minimum contact area (MCA) pins extends from the pedestal body. A controller is configured to extend the MCA pins during processing such that a top surface of the MCA pins is one of below, parallel to or above the band.

processing volume of a processing chamber to a volume of the cavity under the substrate. In some examples, MCA pins are used to support the center of the substrate. In other examples, a plurality of fixed projections extends from the upper surface of the pedestal in the cavity to support the center of the substrate.

[0035] A ring of dielectric material may be arranged radially outside of the annular band. A radially inner portion of the ring may be located radially inside of, adjacent to or radially outside of an outer diameter of the substrate. A top surface of the ring may be located above, parallel to or below a top surface of the substrate.

[0036] The annular band of the pedestal according to the present disclosure provides a wider contact area at the edge of the backside of the substrate, which increases the substrate position tolerance. The vents provide pressure equalization between the volume in the cavity and the main processing volume. The vents can be radially directed to an outer diameter of the pedestal or axially directed from a bottom of the pedestal. The number of vents and the size of vent passages will vary depending on the process pressure and gas flows that are used in a particular process.

[0037] The width of the annular band varies depending on the process temperatures and chemistries used to deposit film on the substrate. The geometry and location of the ring varies relative to the substrate diameter and the pedestal to tune process variables for a particular film to be deposited. The thickness, volume and shape of the ring may be varied depending on the process variables for a particular film to be deposited.

[0038] Referring now to FIG. 1, an example of a substrate processing system for performing deposition described herein is shown. While specific examples of substrate processing systems are shown, other substrate processing systems can be used. In

(collectively mass flow controllers 46) to a manifold 48. An output of the manifold 48 is fed to the processing chamber 12. For example only, the output of the manifold 48 is fed to the showerhead 14.

[0042] A heater 50 may be connected to a heater coil (not shown) arranged in the pedestal assembly 16. The heater 50 may be used to control a temperature of the pedestal assembly 16 and the substrate 18. A valve 60 and pump 62 may be used to evacuate reactants from the processing chamber 12. A controller 70 may be used to control components of the substrate processing system 10. For example only, the controller 70 may be used to control flow of process gases, monitoring of process parameters such as temperature, pressure, power, etc, striking and extinguishing plasma, removal of reactants, etc.

[0043] In some examples, minimum contact area (MCA) pins 71 are used to support a center region of the substrate 18 during processing. If used, the controller 70 may also be used to actuate the MCA pins 71. In some examples, a top surface of the MCA pins 71 are positioned at a height that is below, parallel to or above a top surface of the annular band to provide parallel contact between the substrate and the annular band. In some examples, the MCA pins 71 are made of sapphire, although other materials can be used. The MCA pins can be set such that the height is above, parallel, or below the annular band in order to modify the contact force between the substrate (wafer) and the annular ring (seal band). Higher contact force can ensure reduced backside deposition on the substrate by reducing the gap between substrate and annular ring. There are limits on both how far above and below the MCA pins can be to the annular ring; in both

moves less when venting is used. As the substrate moves relative to the ring, localized differences in deposition may occur. When there is decreased movement of the substrate 18, there is less variation in deposition.

[0055] Referring now to FIGs. 9-11, various example arrangements for the ring 132 are shown. The ring 132 has a generally annular shape and can be made of a dielectric material. In some examples, the dielectric material is selected from alumina, aluminum nitride, sapphire, quartz, and silicon oxide. In FIG. 9, the ring 132-1 is arranged radially outside an outer diameter (OD) of the substrate and the annular band 122. The ring 132-1 includes a lower portion 313 that is received in a notch 315 of the pedestal body 110. The ring 132-1 further includes an upper portion 317. In some examples, the upper portion 317 of the ring 132-1 has a larger radial thickness as compared to the lower portion 313. The ring 132-1 includes a radially inner surface 300-1 that is spaced radially outside of the outer edge 128 of the annular band 122 and the radially outer edge of the substrate 18. A top surface 310-1 of the ring 132-1 is located above, parallel to or below a top surface of the substrate 18.

[0056] In FIG. 10, the ring 132-2 includes a first annular notch 330 that at least partially lies underneath a radially outer edge of the substrate 18. The first annular notch 330 is arranged radially inside of an outer diameter of the substrate 18 and radially outside of the annular band 122. The ring 132-2 further includes a radially innermost surface 334 that is spaced radially inside of the radially outer edge of the substrate 18. A radially inner top surface 332 of the ring 132-2 provides relief to accommodate the radially outer edge of the substrate 18. A top surface 310-2 of the ring 132-2 is located below, above

or parallel to a top surface of the substrate 18. In some examples, the top surface 310-2 lies in a plane that is parallel to a plane including the top surface of the substrate 18.

[0057] In FIG. 11, the pedestal body 110 includes an annular recess 340 arranged around a radially outer edge of the pedestal body 110. A ring 132-3 has an annular shape and includes a lower portion 342 having an axial height d2 that is greater than an axial height d1 of the annular recess 340. A top surface 350 of the ring 132-3 is arranged in a plane that is parallel to a top surface of the substrate 18 or above or below a top surface of the substrate 18 by a distance d3.

[0058] The ring 132 modifies an ionization rate and electron density adjacent to an edge of the substrate 18. The ring 132 lowers the occurrence of unwanted plasma discontinuities in this area. The ring 132 also physically constrains movement of the substrate 18 on the pedestal body 110. The ring 132 reduces plasmoids that may occur at the edge of the substrate 18 when using some gas species, the band and/or venting. The proximity of the ring 132 at the outer diameter of the substrate 18 can reduce the electron density and ionization rates near the edge of the substrate.

[0059] The foregoing description is merely illustrative in nature and is in no way intended to limit the disclosure, its application, or uses. The broad teachings of the disclosure can be implemented in a variety of forms. Therefore, while this disclosure includes particular examples, the true scope of the disclosure should not be so limited since other modifications will become apparent upon a study of the drawings, the specification, and the following claims. It should be understood that one or more steps within a method may be executed in different order (or concurrently) without altering the principles of the present disclosure. Further, although each of the embodiments is

described above as having certain features, any one or more of those features described with respect to any embodiment of the disclosure can be implemented in and/or combined with features of any of the other embodiments, even if that combination is not explicitly described. In other words, the described embodiments are not mutually exclusive, and permutations of one or more embodiments with one another remain within the scope of this disclosure.

[0060] Spatial and functional relationships between elements (for example, between modules, circuit elements, semiconductor layers, etc.) are described using various terms, including “connected,” “engaged,” “coupled,” “adjacent,” “next to,” “on top of,” “above,” “below,” and “disposed.” Unless explicitly described as being “direct,” when a relationship between first and second elements is described in the above disclosure, that relationship can be a direct relationship where no other intervening elements are present between the first and second elements, but can also be an indirect relationship where one or more intervening elements are present (either spatially or functionally) between the first and second elements. As used herein, the phrase at least one of A, B, and C should be construed to mean a logical (A OR B OR C), using a non-exclusive logical OR, and should not be construed to mean “at least one of A, at least one of B, and at least one of C.”

[0061] In some implementations, a controller is part of a system, which may be part of the above-described examples. Such systems can comprise semiconductor processing equipment, including a processing tool or tools, chamber or chambers, a platform or platforms for processing, and/or specific processing components (a substrate pedestal, a gas flow system, etc.). These systems may be integrated with electronics for

controlling their operation before, during, and after processing of a semiconductor substrate or substrate. The electronics may be referred to as the “controller,” which may control various components or subparts of the system or systems. The controller, depending on the processing requirements and/or the type of system, may be programmed to control any of the processes disclosed herein, including the delivery of processing gases, temperature settings (e.g., heating and/or cooling), pressure settings, vacuum settings, power settings, radio frequency (RF) generator settings, RF matching circuit settings, frequency settings, flow rate settings, fluid delivery settings, positional and operation settings, substrate transfers into and out of a tool and other transfer tools and/or load locks connected to or interfaced with a specific system.

[0062] Broadly speaking, the controller may be defined as electronics having various integrated circuits, logic, memory, and/or software that receive instructions, issue instructions, control operation, enable cleaning operations, enable endpoint measurements, and the like. The integrated circuits may include chips in the form of firmware that store program instructions, digital signal processors (DSPs), chips defined as application specific integrated circuits (ASICs), and/or one or more microprocessors, or microcontrollers that execute program instructions (e.g., software). Program instructions may be instructions communicated to the controller in the form of various individual settings (or program files), defining operational parameters for carrying out a particular process on or for a semiconductor substrate or to a system. The operational parameters may, in some embodiments, be part of a recipe defined by process engineers to accomplish one or more processing steps during the fabrication of one or

more layers, materials, metals, oxides, silicon, silicon dioxide, surfaces, circuits, and/or dies of a substrate.

[0063] The controller, in some implementations, may be a part of or coupled to a computer that is integrated with the system, coupled to the system, otherwise networked to the system, or a combination thereof. For example, the controller may be in the “cloud” or all or a part of a fab host computer system, which can allow for remote access of the substrate processing. The computer may enable remote access to the system to monitor current progress of fabrication operations, examine a history of past fabrication operations, examine trends or performance metrics from a plurality of fabrication operations, to change parameters of current processing, to set processing steps to follow a current processing, or to start a new process. In some examples, a remote computer (e.g. a server) can provide process recipes to a system over a network, which may include a local network or the Internet. The remote computer may include a user interface that enables entry or programming of parameters and/or settings, which are then communicated to the system from the remote computer. In some examples, the controller receives instructions in the form of data, which specify parameters for each of the processing steps to be performed during one or more operations. It should be understood that the parameters may be specific to the type of process to be performed and the type of tool that the controller is configured to interface with or control. Thus as described above, the controller may be distributed, such as by comprising one or more discrete controllers that are networked together and working towards a common purpose, such as the processes and controls described herein. An example of a distributed controller for such purposes would be one or more integrated

circuits on a chamber in communication with one or more integrated circuits located remotely (such as at the platform level or as part of a remote computer) that combine to control a process on the chamber.

[0064] Without limitation, example systems may include a plasma etch chamber or module, a deposition chamber or module, a spin-rinse chamber or module, a metal plating chamber or module, a clean chamber or module, a bevel edge etch chamber or module, a physical vapor deposition (PVD) chamber or module, a chemical vapor deposition (CVD) chamber or module, an atomic layer deposition (ALD) chamber or module, an atomic layer etch (ALE) chamber or module, an ion implantation chamber or module, a track chamber or module, and any other semiconductor processing systems that may be associated or used in the fabrication and/or manufacturing of semiconductor substrates.

[0065] As noted above, depending on the process step or steps to be performed by the tool, the controller might communicate with one or more of other tool circuits or modules, other tool components, cluster tools, other tool interfaces, adjacent tools, neighboring tools, tools located throughout a factory, a main computer, another controller, or tools used in material transport that bring containers of substrates to and from tool locations and/or load ports in a semiconductor manufacturing factory.

CLAIMS

1. A pedestal for a substrate processing system, comprising:

a pedestal body including a substrate-facing surface;

an annular band arranged on the substrate-facing surface that is configured to support a radially outer edge of the substrate; and

a cavity that is defined in the substrate-facing surface of the pedestal body and that is located radially inside of the annular band, wherein the cavity creates a volume between a bottom surface of the substrate and the substrate-facing surface of the pedestal body; and

a plurality of vents passing through the pedestal body and in fluid communication with the cavity to equalize pressure on opposing faces of the substrate during processing.

2. The pedestal of claim 1, wherein the annular band has a width in a range from 4 mm to 12 mm.

3. The pedestal of claim 1, wherein the annular band has a width in a range from 5 mm to 9 mm.

4. The pedestal of claim 1, wherein the annular band has a width in a range from 6 mm to 7 mm.

5. The pedestal of claim 1, wherein the annular band has a surface roughness (R_a) in a range from 2 to 32.

6. The pedestal of claim 5, wherein the surface roughness (Ra) in a range from 2 to 24.

7. The pedestal of claim 5, wherein the surface roughness (Ra) in a range from 2 to 16.

8. The pedestal of claim 1, wherein the plurality of vents include:

a first vent portion extending radially inwardly from a radially outer side of the pedestal body; and

a second vent portion extending from a radially inner edge of the first vent portion to the cavity.

9. The pedestal of claim 1, wherein the plurality of vents include:

a first vent portion extending axially from a bottom side of the pedestal body towards the cavity; and

a second vent portion including a plurality of holes connecting the first vent portion to the cavity.

10. The pedestal of claim 1, wherein the annular band is made of a material selected from a group consisting of a dielectric coating formed on a surface of a conductive material, an uncoated conductive material, an uncoated metal, and an uncoated dielectric material.

11. The pedestal of claim 1, further comprising:

a ring arranged radially outside of the substrate and the annular band,

wherein a top surface of the ring is arranged above a top surface of the substrate, and

wherein the ring is made of a dielectric material.

12. The pedestal of claim 11, wherein the dielectric material is selected from a group consisting of alumina, aluminum nitride, sapphire, quartz, and silicon oxide.

13. The pedestal of claim 1, further comprising:

a ring including a radially inner surface arranged radially inside of and below the substrate and a radially outer surface arranged radially outside of the substrate,

wherein a top surface of the ring is parallel to a top surface of the substrate, and

wherein the ring is made of a dielectric material.

14. The pedestal of claim 13, wherein the dielectric material is selected from a group consisting of alumina, aluminum nitride, sapphire, quartz, and silicon oxide.

15. The pedestal of claim 1, wherein the pedestal body includes an annular notch around a radially outer edge thereof and further comprising:

a ring arranged in the annular notch,

wherein a bottom surface of the ring lies below a bottom surface of the substrate,

wherein a top surface of the ring lies below a top surface of the substrate, and

wherein the ring is made of a dielectric material.

16. The pedestal of claim 15, wherein the dielectric material is selected from a group consisting of alumina, aluminum nitride, sapphire, quartz, and silicon oxide.

17. The pedestal of claim 1, further comprising:

a plurality of pins arranged in the cavity to support a center of the substrate,

wherein a top surface of the pins is one of below, parallel to or above a top surface of the annular band during processing.

18. The pedestal of claim 1, further comprising:

a plurality of projections to support a center of the substrate,

wherein a top surface of the projections is one of below, parallel to or above a top surface of the annular band.

19. The pedestal of claim 1, wherein a backside surface of the substrate along the radially outer edge of the substrate is parallel to the annular band during processing.

20. A substrate processing system comprising:

a processing chamber;

the pedestal of claim 1, wherein the pedestal is arranged in the processing chamber; and

an RF generator arranged in the processing chamber.

21. The substrate processing system of claim 20, further comprising:

a plurality of minimum contact area (MCA) pins extendable from the pedestal body; and

a controller configured to extend the MCA pins during processing such that a top surface of the MCA pins is one of below, parallel to or above the annular band.

22. The pedestal of claim 1, further comprising a plurality of projections extending upwardly from the pedestal body in the cavity.