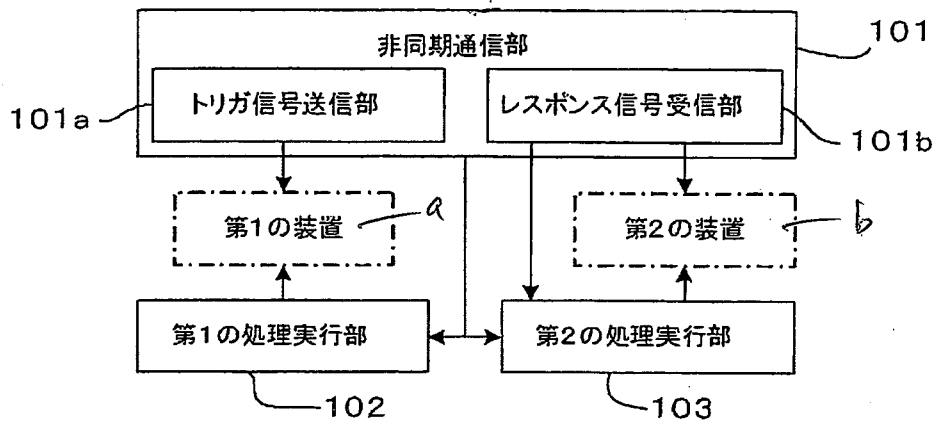


Fig. 1
 1-1
 (a)



(b)

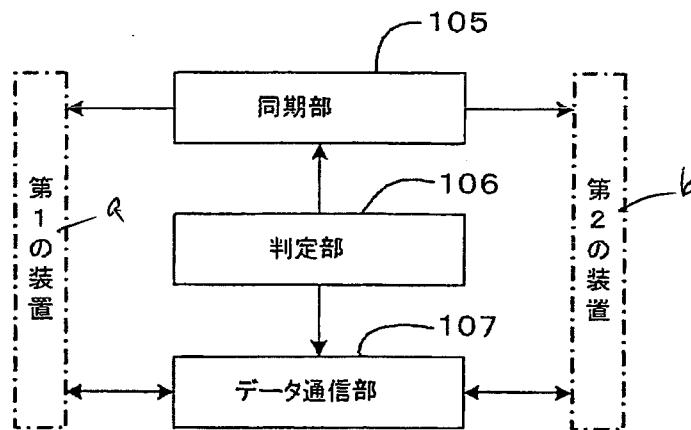


Fig. 2
 2-2

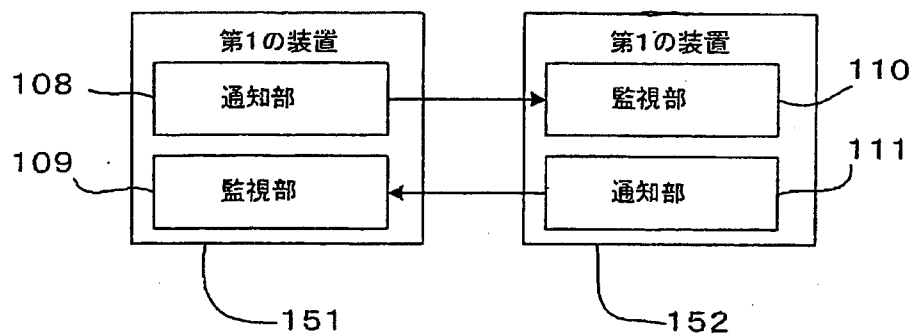


Fig. 3

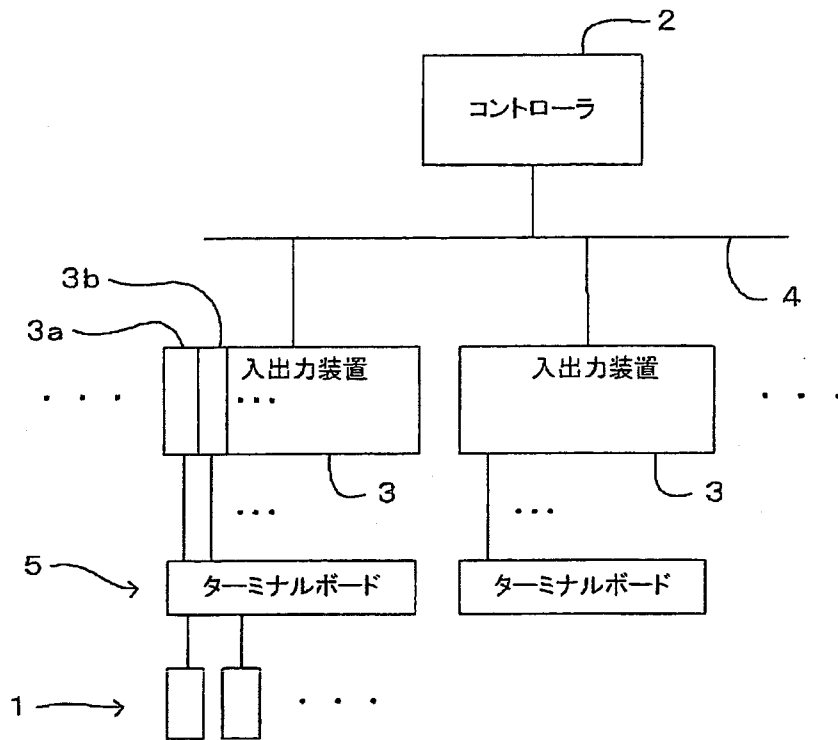


Fig. 4

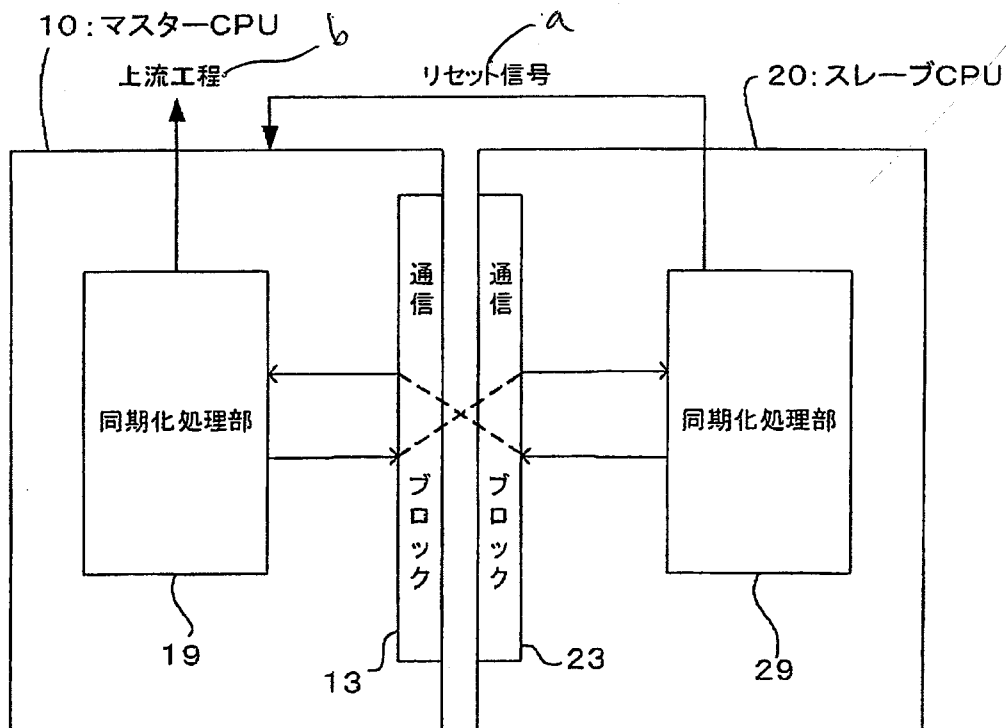


Fig. 5

[図5]

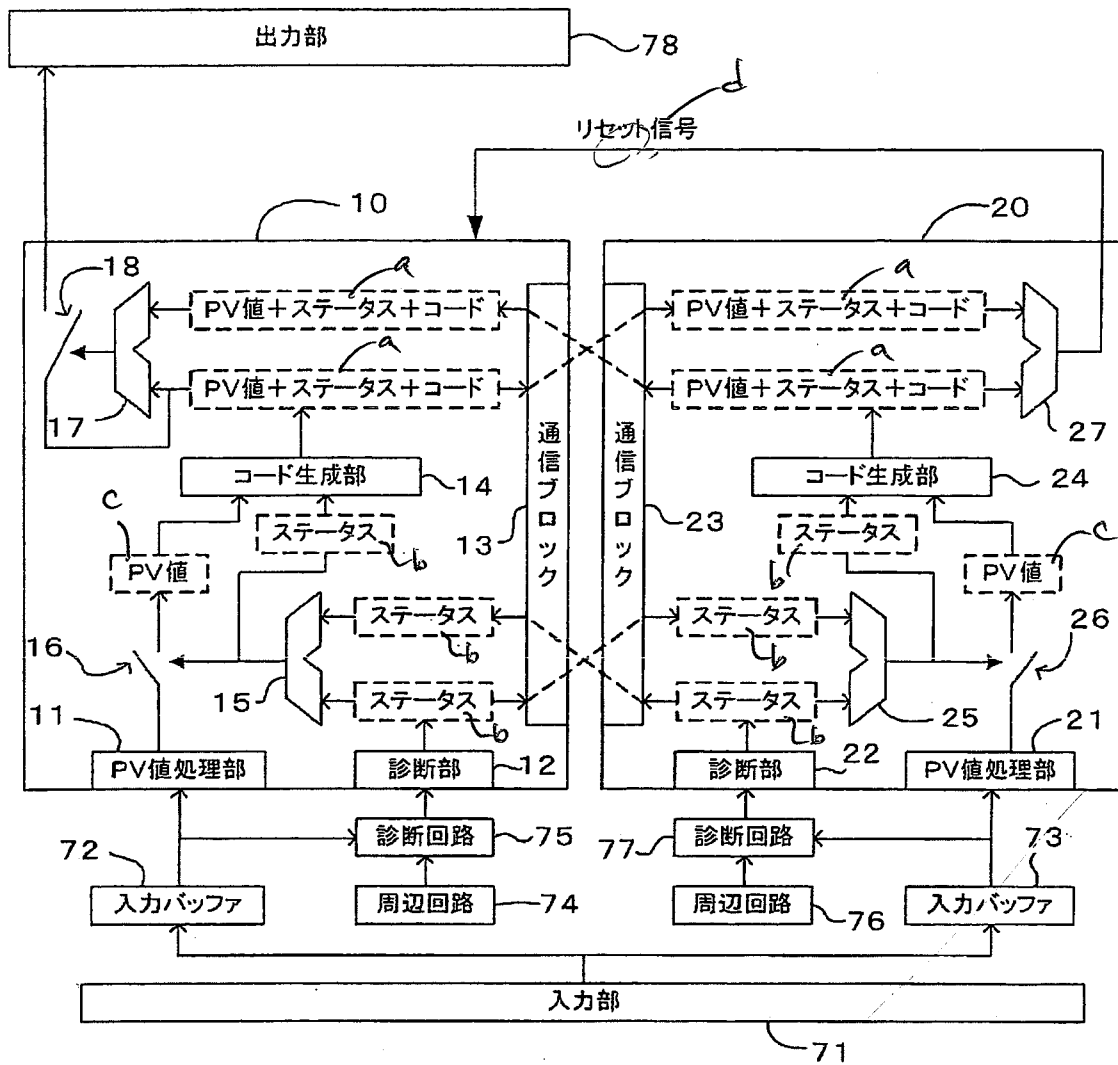


Fig. 6

[図6]

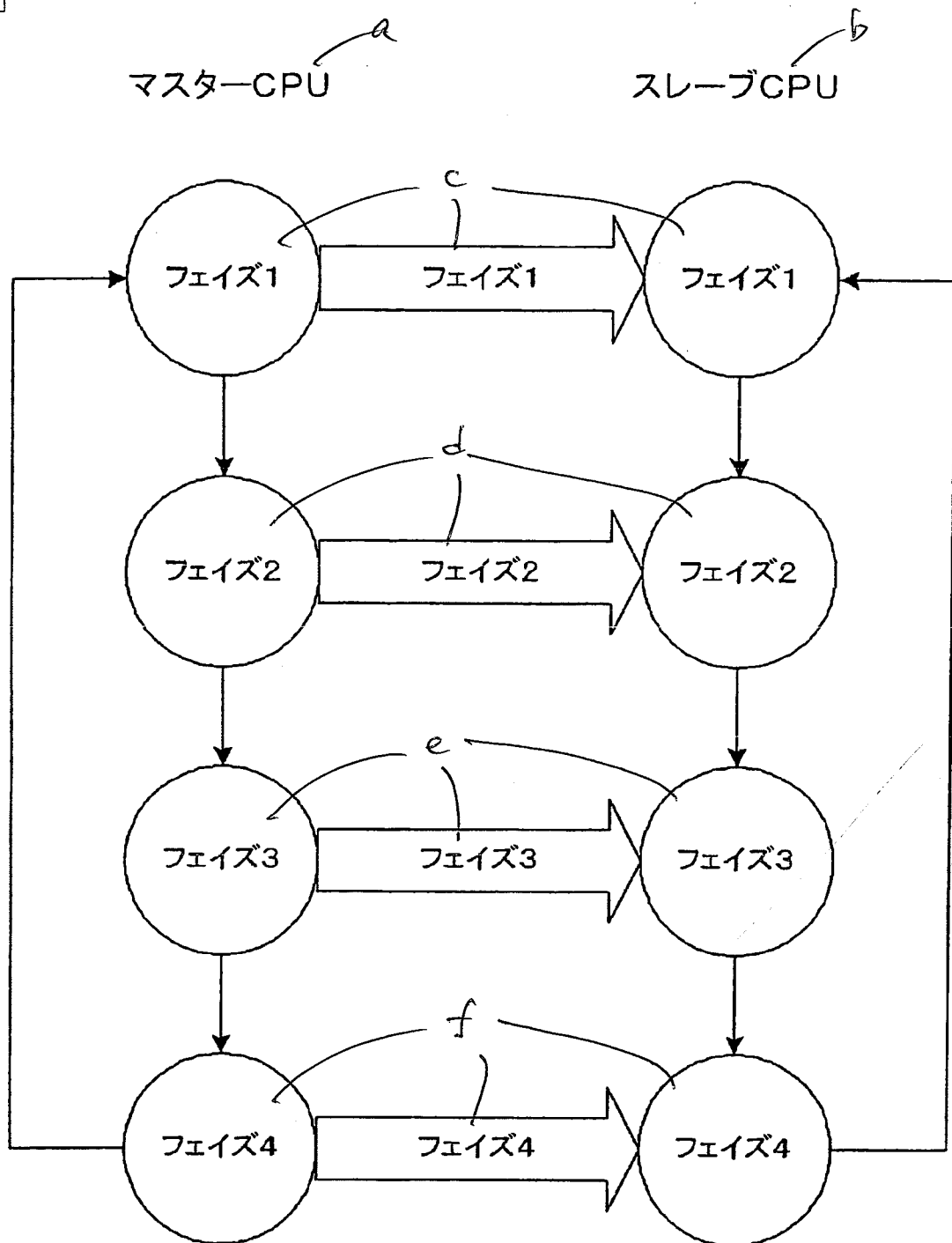


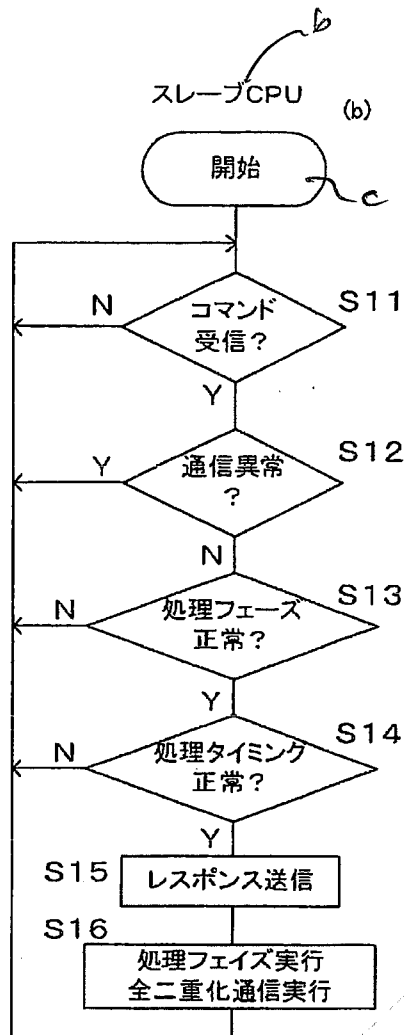
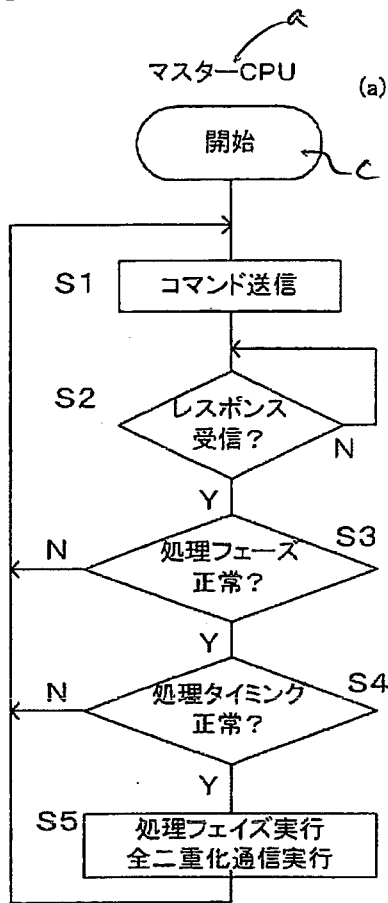
Fig. 7
[図7]

Fig. 8

[図8]

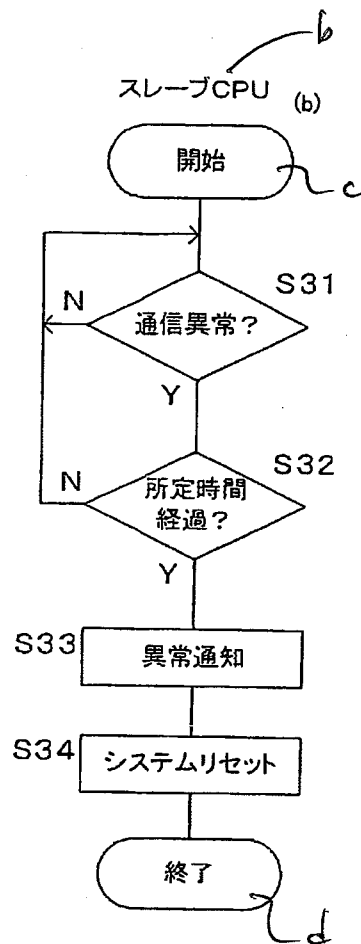
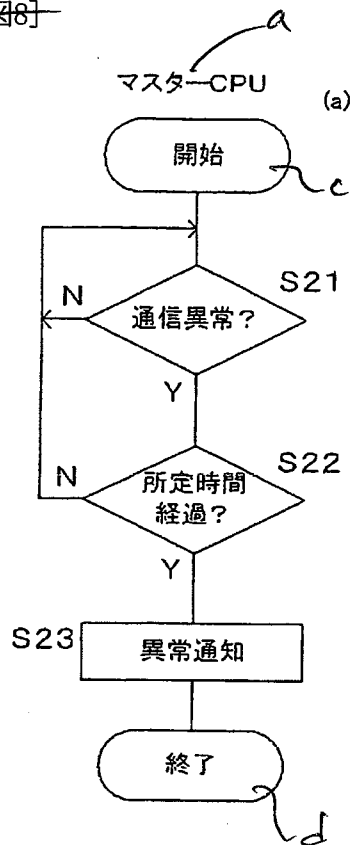


Fig. 9

[図9]

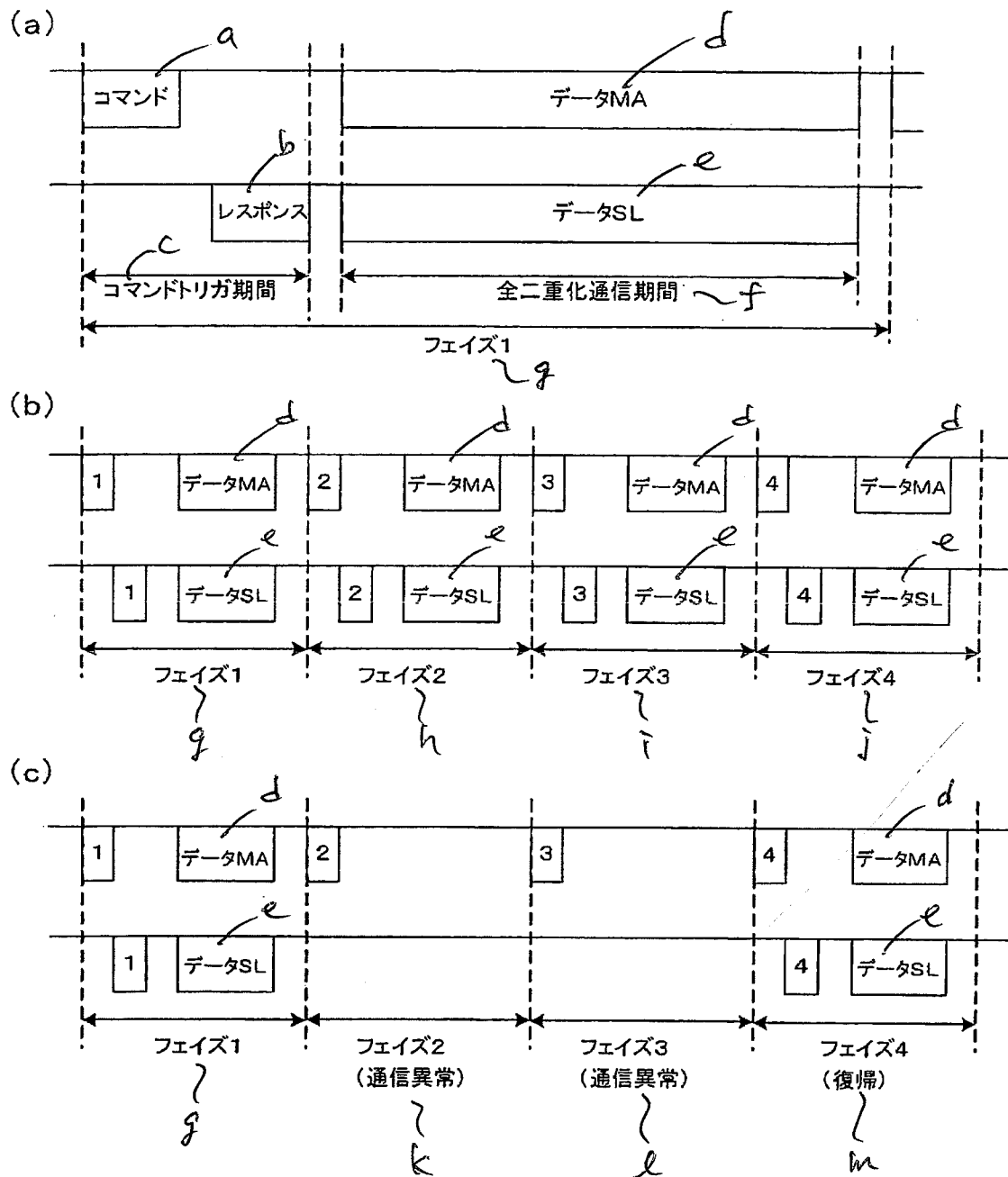


Fig. 10
[図10]

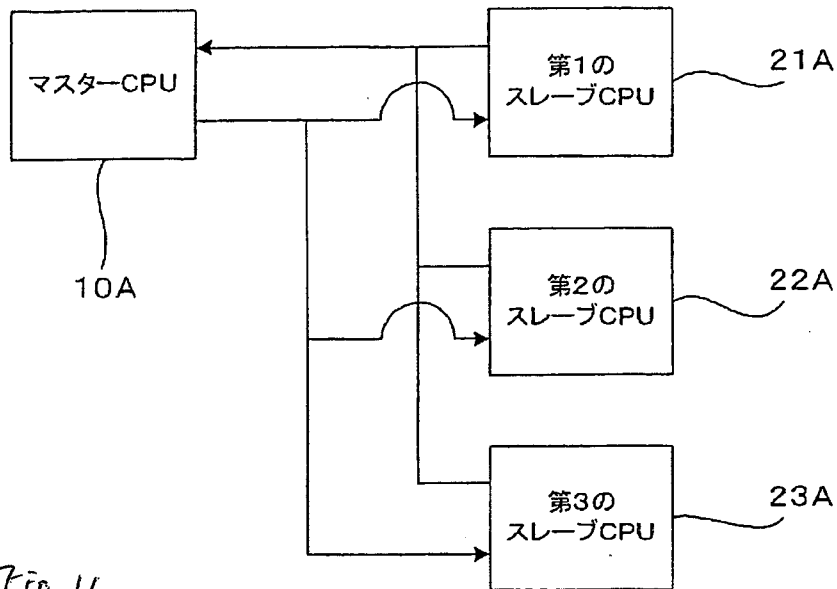


Fig. 11
[図11]

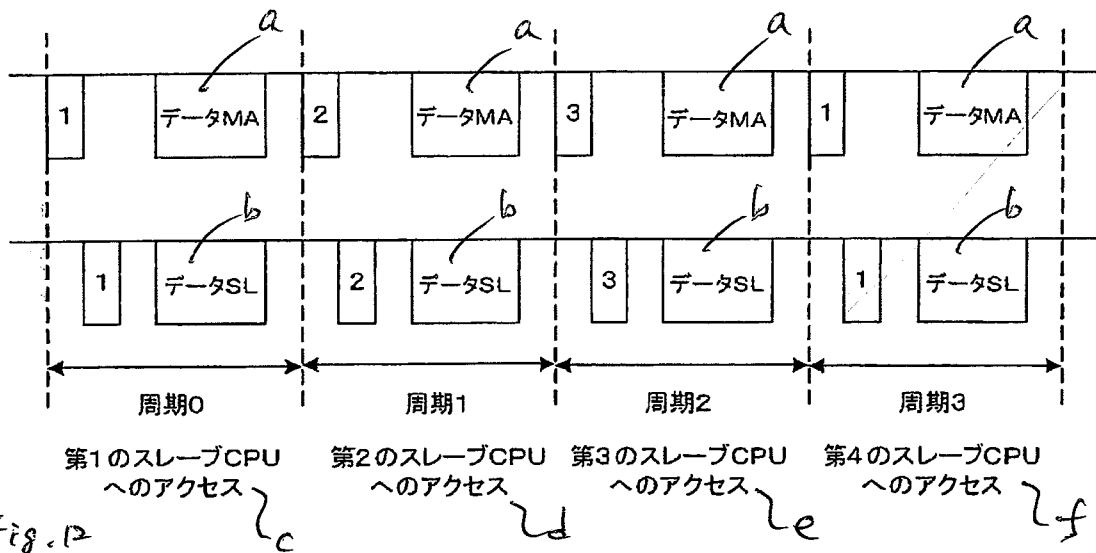


Fig. 12
[図12]

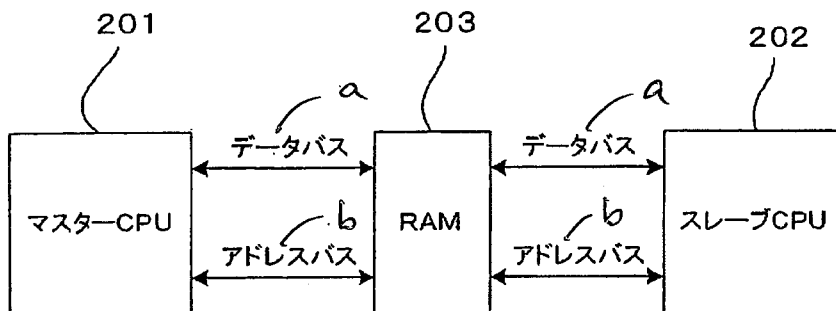


Fig. 1:

- a first device
- b second device
- 101 asynchronous communicating part
- 101a trigger signal sending part
- 101b response signal receiving part
- 102 first process executing part
- 103 second process executing part
- 105 synchronizing part
- 106 determining part
- 107 data communicating part

Fig. 2:

- 108 notifying part
- 109 monitoring part
- 110 monitoring part
- 111 notifying part
- 151 first device
- 152 first device

Fig. 3:

- 2 controller
- 3 input-output device
- 5 terminal board

Fig. 4:

- a reset signal
- b upstream process
- 10 master CPU
- 20 slave CPU
- 13 communication block
- 19 synchronization processing part
- 23 communication block
- 29 synchronization processing part

Fig. 5:

- a PV value + status + code
- b status
- c PV value
- d reset signal
- 11 PV value processing part
- 12 diagnostic part
- 13 communication block
- 14 code generating part
- 21 PV value processing part
- 22 diagnostic part
- 23 communication block
- 24 code generating part
- 71 input part
- 72 input buffer

- 73 input buffer
- 74 peripheral circuit
- 75 diagnostic circuit
- 76 peripheral circuit
- 77 diagnostic circuit
- 78 output part

Fig. 6:

- a master CPU
- b slave CPU
- c phase 1
- d phase 2
- e phase 3
- f phase 4

Fig. 7:

- a master CPU
- b slave CPU
- c start
- S1 send command
- S2 Is response received?
- S3 Is processing phase normal?
- S4 Is processing timing normal?
- S5 execute processing phase execute full-duplexing communication
- S11 Is command received?

- S12 Is communication abnormal?
- S13 Is processing phase normal?
- S14 Is processing timing normal?
- S15 send response
- S16 execute processing phase execute full-duplexing communication

Fig. 8:

- a master CPU
- b slave CPU
- c start
- d end
- S21 Is communication abnormal?
- S22 Has predetermined time elapsed?
- S23 abnormal notification
- S31 Is communication abnormal?
- S32 Has predetermined time elapsed?
- S33 abnormal notification
- S34 system reset

Fig. 9:

- a command
- b response
- c command trigger period
- d data MA
- e data SL

f	full-duplexing communication period
g	phase 1
h	phase 2
i	phase 3
j	phase 4
k	phase 2 (communication abnormality)
l	phase 3 (communication abnormality)
m	phase 4 (return)

Fig. 10:

10A	master CPU
21A	first slave CPU
22A	second slave CPU
23A	third slave CPU

Fig. 11:

a	data MA
b	data SL
c	cycle 0 access to first slave CPU
d	cycle 1 access to second slave CPU
e	cycle 2 access to third slave CPU
f	cycle 3 access to fourth slave CPU

Fig. 12:

a	data bus
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b address bus
201 master CPU
202 slave CPU