

ABSTRACT

A memory device including a first substrate including a cell region and a peripheral region disposed around the cell region; a memory cell array disposed in the cell region of the first substrate; a second
5 substrate disposed on the memory cell array; peripheral transistors disposed on the second substrate and connected to the memory cell array; a first insulating layer disposed in a trench that is located in the peripheral region of the first substrate, and including high density plasma oxide; and a second insulating layer on the first insulating layer.

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FIG. 5