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I-02010 Vazia, RI (IT). **VALI, Tommaso** [IT/IT]; Via
Piagge Marine, I-04018 Sezze, Latina (IT).

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(74) Agent: **BOLVIN, Kenneth, W.**; LEFFERT, JAY & POL-
GLAZE, P.A., P.O. Box 581009, Minneapolis, MN 55458-
1009 (US).

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(71) Applicant (for all designated States except US): **MICRON
TECHNOLOGY, INC.** [US/US]; 8000 So. Federal Way,
Boise, ID 83716 (US).

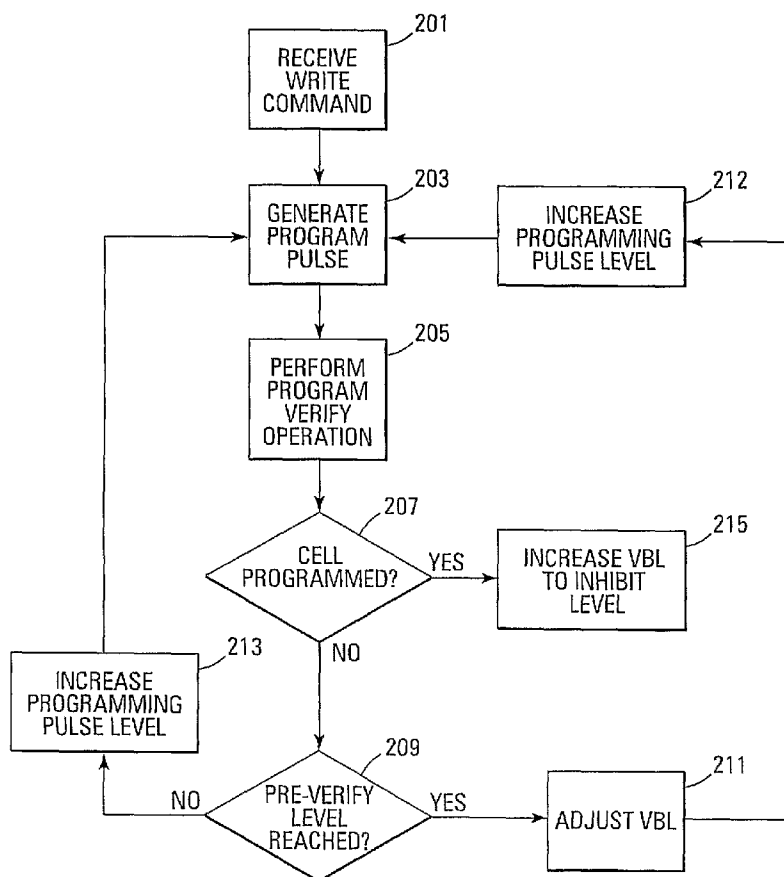
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(72) Inventors; and

(75) Inventors/Applicants (for US only): **INCARNATI,
Michele** [IT/IT]; Via Calvario 5, I-67055 Gioia Del Marsi
(AQ) (IT). **SANTIN, Giovanni** [IT/IT]; Via Marche 3,

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(54) Title: SELECTIVE SLOW PROGRAMMING CONVERGENCE IN A FLASH MEMORY DEVICE



(57) Abstract: A plurality of memory cells are programmed with incrementally increased programming pulses applied to word lines to which the memory cells are coupled. After each pulse, a verify operation determines the threshold voltage for each cell. When the threshold voltage reaches a pre-verify threshold, only the bit line connected to that particular cell is biased with an intermediate voltage that slows down the change in the V_t of the cell. The other cells continue to be programmed at their normal pace. As the V_t for each cell reaches the pre-verify level, it is biased with the intermediate voltage. All of the bit lines are biased with an inhibit voltage as their threshold voltages reach the verify voltage threshold.



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