WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

an interlayer insulating layer disposed on a substrate;

a plurality of middle interconnections disposed in the interlayer insulating layer;

a plurality of middle plugs disposed in the interlayer insulating layer and between the plurality of middle interconnections;

an upper insulating layer disposed on the interlayer insulating layer;

a first upper plug disposed in the upper insulating layer and connected to one middle interconnection of the plurality of middle interconnections, the one middle interconnection having a first thickness;

a first upper interconnection disposed in the upper insulating layer on the first upper plug and having a second thickness, wherein the second thickness is greater than the first thickness;

a second upper plug disposed in the upper insulating layer on the first upper interconnection;

a second upper interconnection disposed in the upper insulating layer on the second upper plug and having a third thickness, wherein the third thickness is greater than the first thickness; and

an opening configured to pass through the upper insulating layer to expose the second upper interconnection,

wherein the third thickness is in the range of 2 to 100 times the first thickness,

wherein the second upper interconnection comprises a material different from that of the second upper plug,

wherein the upper insulating layer comprises:

a first upper insulating layer;

a second upper insulating layer disposed on the first upper insulating layer and comprising a material different from that of the first upper insulating layer; and

a third upper insulating layer disposed on the second upper insulating layer and comprising a material different from that of the second upper insulating layer,

wherein the first upper insulating layer, the second upper insulating layer, and the third upper insulating layer are disposed between the first upper interconnection and the second upper interconnection, and

wherein the second upper plug passes through the first upper insulating layer, the second upper insulating layer, and the third upper insulating layer and contacts the first upper interconnection and the second upper interconnection.

2. The semiconductor device of claim 1, wherein the third thickness is greater than or equal to the second thickness.

3. The semiconductor device of claim 1 or claim 2, wherein the third thickness is in the range of 2 μm to 10 μm.

4. The semiconductor device of any one of claims 1 to 3,

wherein each of the plurality of middle plugs has a first height,

wherein the first upper plug has a second height greater than the first height, and

wherein the second upper plug has a third height greater than the first height.

5. The semiconductor device of claim 4, wherein the third height is greater than or equal to the second height.

6. The semiconductor device of any one of claims 1 to 5, wherein each of the first upper interconnection and the second upper interconnection comprises a material layer different from that of the plurality of middle interconnections.

7. The semiconductor device of any one of claims 1 to 6,

wherein the plurality of middle interconnections comprise a copper (Cu) layer, and

wherein the second upper interconnection comprises an aluminum (Al) layer.

8. The semiconductor device of any one of claims 1 to 7, wherein the first upper interconnection comprises an Al layer.

9. The semiconductor device of any one of claims 1 to 8, wherein the second upper plug comprises a tungsten (W) layer.

10. The semiconductor device of any one of claims 1 to 9,

wherein the first upper insulating layer comprises an oxide layer,

wherein the second upper insulating layer comprises a nitride layer, and

wherein the third upper insulating layer comprises an oxide layer.

11. The semiconductor device of any one of claims 1 to 10, further comprising a through electrode extending into the substrate and connected to the plurality of middle interconnections.

12. The semiconductor device of claim 11, wherein the through electrode has a diameter of 1 μm to 20 μm.

13. The semiconductor device of any one of claims 1 to 12, further comprising:

a lower insulating layer disposed between the substrate and the interlayer insulating layer; and

a memory cell disposed in the lower insulating layer.

14. The semiconductor device of claim 13, wherein the memory cell comprises a dynamic random access memory (DRAM) cell, a static RAM (SRAM) cell, a flash memory cell, a magneto-resistive RAM (MRAM) cell, a phase-change RAM (PRAM) cell, a ferroelectric RAM (FeRAM) cell, a resistive RAM (RRAM) cell, or a combination thereof.

15. A semiconductor device comprising:

a plurality of semiconductor chips sequentially stacked on a printed circuit board (PCB),

wherein at least one of the plurality of semiconductor chips comprises:

a lower insulating layer disposed on a substrate;

a memory cell disposed in the lower insulating layer;

an interlayer insulating layer disposed on the lower insulating layer;

a plurality of middle interconnections disposed in the interlayer insulating layer;

a plurality of middle plugs disposed in the interlayer insulating layer and between the plurality of middle interconnections;

an upper insulating layer disposed on the interlayer insulating layer;

a first upper plug disposed in the upper insulating layer and connected to one middle interconnection of the plurality of middle interconnections, the one middle interconnection having a first thickness;

a first upper interconnection disposed in the upper insulating layer on the first upper plug and having a second thickness, wherein the second thickness is greater than the first thickness;

a second upper plug disposed in the upper insulating layer and on the first upper interconnection;

a second upper interconnection disposed in the upper insulating layer on the second upper plug and having a third thickness, wherein the third thickness is greater than the first thickness;

a bump disposed on the upper insulating layer, the bump extending into the upper insulating layer and contacting the second upper interconnection; and

a through electrode extending into the substrate and connected to the plurality of middle interconnections,

wherein the third thickness is in the range of 2 to 100 times the first thickness, and

wherein the second upper interconnection comprises a material different from that of the second upper plug.

16. The semiconductor device of claim 15, wherein the bump has a diameter of 10 μm to 50 μm.

17. The semiconductor device of claim 15 or claim 16, wherein the third thickness is greater than or equal to the second thickness.

18. The semiconductor device of any one of claims 15 to 17,

wherein each of the plurality of middle plugs has a first height,

wherein the first upper plug has a second height greater than the first height, and

wherein the second upper plug has a third height greater than the first height.

19. A semiconductor device comprising:

a relay substrate;

a microprocessor disposed on the relay substrate;

a buffer chip disposed on the relay substrate; and

a plurality of semiconductor chips sequentially stacked on the buffer chip,

wherein at least one of the plurality of semiconductor chips comprises:

a lower insulating layer disposed on a substrate;

a memory cell disposed in the lower insulating layer;

an interlayer insulating layer disposed on the lower insulating layer;

a plurality of middle interconnections disposed in the interlayer insulating layer;

a plurality of middle plugs disposed in the interlayer insulating layer and between the plurality of middle interconnections;

an upper insulating layer disposed on the interlayer insulating layer;

a first upper plug disposed in the upper insulating layer and connected to one middle interconnection of the plurality of middle interconnections, the one middle interconnection having a first thickness;

a first upper interconnection disposed in the upper insulating layer on the first upper plug and having a second thickness, wherein the second thickness is greater than the first thickness;

a second upper plug disposed in the upper insulating layer and on the first upper interconnection;

a second upper interconnection disposed in the upper insulating layer on the second upper plug and having a third thickness, wherein the third thickness is greater than the first thickness;

a bump disposed on the upper insulating layer, the bump extending into the upper insulating layer and contacting the second upper interconnection; and

a through electrode extending into the substrate and connected to the plurality of middle interconnections,

wherein the third thickness is in the range of 2 to 100 times the first thickness, and

wherein the second upper interconnection comprises a material different from the second upper plug.