

Method and System for Stabilising a Signal

Technical Field

The present invention relates to signal processing and more particularly to a method and system for stabilising a signal.

5 Background of the Invention

Signal averaging is a signal processing technique that is commonly employed in measuring periodical signals. This technique involves accumulating a number of repeated segments of a periodical signal. Signal averaging exploits the fact that if a periodical signal is coherently summed, the signal accumulates while
10 noise tends to cancel itself out due to its randomness. This phenomenon enhances the signal-to-noise ratio (SNR) of a signal, that is, the ratio of the power of the signal to the power of noise, thereby improving the accuracy of the measured signal. For example, the SNR of an input signal, which provides a measure of how accurately the signal can be measured, may be increased from,
15 say, 10 to 20 decibels (dB) by accumulating (or averaging) ten (10) neighbouring periods of the signal.

SNR enhancement by signal averaging is based on the assumption that the period of the input signal is known and constant. In reality, however, this assumption often does not hold true. In most application environments, the period
20 of the signal is often irregular due, for example, to jitter and frequency drift of the oscillator used in signal generation or, in more severe cases, sampling of the signal at a lower sampling rate than the frequency of the signal. In the latter instance, the period of the sampled signal is often less stable than that of the original signal. When signal averaging is performed on a signal with irregular
25 periodicity, the waveform of the accumulated signal is unstable and SNR is not significantly enhanced. As such, the periodicity of a signal is usually stabilised with a conventional phase-locked loop (PLL) circuit prior to signal averaging. The

conventional PLL circuit compares the input signal with a reference (local) signal to obtain a phase error signal. However, as this requires prior knowledge of the waveform shape of the input signal as reference, signal stabilisation using a conventional PLL circuit is often ineffective in real applications as the exact
5 waveform shape of the input signal is often not known in advance in a real environment because it changes over time due, for example, to multi-path propagation.

Thus, a need exists for a method and system for stabilising a signal that does not require prior knowledge of the waveform shape of an input signal to
10 generate phase error signals. There also exists a need for a method and system for stabilising a signal that is independent of waveform changes caused, for example, by multi-path propagation.

Summary of the Invention

Accordingly, the present invention provides, in a first aspect, a method for
15 stabilising a signal, the method comprising: receiving an input signal; generating a plurality of delayed signals based on the input signal; comparing a segment of the input signal with a segment of each of the delayed signals; generating an error signal based on the comparison; and performing signal period adjustment based on the error signal.

20 Advantageously, because the error signal is generated from segments of the input signal, the invention is independent of waveform distortion caused, for example, by multi-path propagation and does not require prior knowledge of the waveform shape of the input signal to generate phase error signals.

In a preferred embodiment, a correlation calculation is performed between
25 the segment of the input signal and a corresponding segment of each of the delayed signals. An optimal delay value corresponding to a maximum correlation value calculated may be determined from the correlation calculation performed.

The optimal delay value may be determined from a correlation curve generated based on the correlation calculation performed. The error signal may be generated by determining a difference between the optimal delay values for successive segments of the input signal.

5 The delayed signals may be generated by introducing a range of delay values into the input signal. The range of delay values may be between about $\bar{D} - \Delta$ and about $\bar{D} + \Delta$, where $\bar{D}$ represents an optimal delay estimate and Δ represents a margin of error. The optimal delay estimate $\bar{D}$ may be approximately equal to one (1) period of the input signal and Δ may represent a
10 margin of period error.

Signal period adjustment may be performed by reducing a clock frequency such as, for example, the clock frequency to a sampler or from a memory writing clock module, when the error signal indicates that a period of a current segment of the input signal is of a longer duration than a period of a preceding segment of the
15 input signal, and increasing the clock frequency when the error signal indicates that the period of the current segment is of a shorter duration than the period of the preceding segment.

Preferably, a fast change part of the input signal is filtered out. This makes error signal estimation more stable. The input signal may be sampled. A timing of
20 the sampled signal may be isolated. This allows implementation of the signal stabilising method in a larger system.

The input signal may be a continuous periodical signal or a packet-based signal.

In a second aspect, the invention further provides a signal averaging
25 method, comprising: receiving an input signal; generating a plurality of delayed signals based on the input signal; comparing a segment of the input signal with a segment of each of the delayed signals; generating an error signal based on the

comparison; performing signal period adjustment based on the error signal; and performing waveform accumulation after signal period adjustment.

Advantageously, because waveform accumulation is performed after signal period adjustment (and hence signal period stabilisation), the shape of the accumulated waveform is stable and SNR of the accumulated waveform is enhanced.

In the second aspect, corresponding advantages are obtained as previously described in respect of the first aspect. Moreover, corresponding further features as described above in respect of the first aspect may also be employed.

In a third aspect, the invention further provides a system for stabilising a signal, the system comprising: a delay line configured to generate a plurality of delayed signals based on an input signal; an error signal generation module configured to generate an error signal based on a comparison of a segment of the input signal with a segment of each of the delayed signals; and an adjustment module configured to perform signal period adjustment based on the error signal.

In the third aspect, corresponding advantages are obtained as previously described in respect of the first aspect.

In a preferred embodiment, the error signal generation module includes a correlation module configured to perform a correlation calculation between the segment of the input signal and a corresponding segment of each of the delayed signals. The correlation module may be configured to determine an optimal delay value corresponding to a maximum correlation value calculated. The correlation module may be configured to determine the optimal delay value from a correlation curve generated based on the correlation calculation performed. The error signal generation module may be configured to determine a difference between the optimal delay values for successive segments of the input signal.

The delay line may be configured to introduce a range of delay values into the input signal. Preferably, the delay line is configured to introduce the range of delay values between about $\overline{D} - \Delta$ and about $\overline{D} + \Delta$, where $\overline{D}$ represents an optimal delay estimate and Δ represents a margin of error, into the input signal.

5 Preferably, $\overline{D}$ is approximately equal to one (1) period of the input signal and Δ represents a margin of period error.

The adjustment module may be configured to reduce a clock frequency such as, for example, the clock frequency to a sampler or from a memory writing clock module, when the error signal indicates that a period of a current segment of the input signal is of a longer duration than a period of a preceding segment of the input signal, and to increase the clock frequency when the error signal indicates that the period of the current segment is of a shorter duration than the period of the preceding segment.

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In a preferred embodiment, a filter is configured to filter out a fast change part of the input signal. The filter may be an envelope detection module.

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In a preferred embodiment, a sampler is configured to sample the input signal. The sampler may be an Analog to Digital Converter (ADC). A buffer may be configured to isolate a timing of the sampled signal. The buffer may be a First In First Out (FIFO) memory.

In a fourth aspect, the invention further provides a signal averaging system, comprising: a delay line configured to generate a plurality of delayed signals based on an input signal; an error signal generation module configured to generate an error signal based on a comparison of a segment of the input signal with a segment of each of the delayed signals; an adjustment module configured to perform signal period adjustment based on the error signal; and an accumulator configured to perform waveform accumulation after signal period adjustment.

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In the fourth aspects, corresponding advantages are obtained as previously described in respect of the second aspect. Moreover, corresponding further features as described above in respect of the third aspect may also be employed.

Other aspects and advantages of the invention will become apparent from
5 the following detailed description, taken in conjunction with the accompanying drawings, illustrating by way of example the principles of the invention.

Brief Description of the Drawings

The following detailed description of preferred embodiments of the invention will be better understood when read in conjunction with the appended drawings.
10 The present invention is illustrated by way of example and is not limited by the accompanying figures, in which like references indicate similar elements.

FIG. 1 is a schematic diagram of a signal averaging system in accordance with one embodiment of the present invention;

FIG. 2 is a schematic flow diagram of a signal averaging method in
15 accordance with one embodiment of the present invention;

FIG. 3 is a waveform diagram showing a waveform of a sampled signal in accordance with one embodiment of the present invention;

FIG. 4 is a schematic diagram of an approach to determining the error signal in accordance with one embodiment of the present invention;

20 FIG. 5 is a waveform diagram showing a plurality of correlation curves generated in respect of successive segments i , $i+1$, $i+2$ and $i+3$ of the input signal $r(t)$;

FIG. 6A is a waveform diagram showing a clock signal from the clock circuit of FIG. 1 prior to any frequency adjustment;

FIG. 6B is a waveform diagram showing the clock signal of FIG. 6A after frequency reduction when the input signal period t_1 is greater than a set optimal signal period t_2 ;

FIG. 6C is a waveform diagram showing the clock signal of FIG. 6A after frequency increment when the input signal period t_1 is less than a set optimal signal period t_2 ;

FIG. 7 is a schematic diagram of a signal averaging system in accordance with another embodiment of the present invention;

FIG. 8 is a schematic flow diagram of a signal averaging method in accordance with another embodiment of the present invention;

FIG. 9A is a waveform diagram showing an Ultra-Wideband (UWB) pulse waveform under a first set of conditions prior to period adjustment and accumulation;

FIG. 9B is a waveform diagram showing the UWB pulse waveform of FIG. 9A after period adjustment and accumulation;

FIG. 10A is a waveform diagram showing nine (9) individual waveforms under the first set of conditions prior to period adjustment and accumulation;

FIG. 10B is a waveform diagram showing the 9 individual waveforms of FIG. 10A after period adjustment and accumulation;

FIG. 11A is a waveform diagram showing nine (9) individual waveforms under a second set of conditions prior to period adjustment and accumulation; and

FIG. 11B is a waveform diagram showing the 9 individual waveforms of FIG. 11A after period adjustment and accumulation.

Detailed Description of the Invention

The detailed description set forth below in connection with the appended drawings is intended as a description of the presently preferred embodiments of the invention, and is not intended to represent the only form in which the present invention may be practiced. It is to be understood that the same or equivalent
5 functions may be accomplished by different embodiments that are intended to be encompassed within the scope of the invention.

Referring now to FIG. 1, a signal averaging system 10 is shown. The system 10 includes an ADC 12 driven by a clock frequency 14 generated by a clock circuit 16 (and modified by an adjustment module 30 as explained below).
10 The ADC 12 is configured to sample an input signal $r(t)$. A FIFO memory 18 having an independent write and read clock (not shown) is coupled to an output of the ADC 12. The FIFO memory 18 is configured to isolate a timing of the sampled signal. An envelope detection module 20 and a waveform accumulator 22 are coupled to an output of the FIFO memory 18. The envelope detection module 20
15 is configured to filter out a fast change part of the input signal $r(t)$ and the waveform accumulator 22 is configured to perform waveform accumulation. A delay line 24, coupled to an output of the envelope detection module 20, is configured to generate a plurality of delayed signals based on the input signal $r(t)$. An error signal generation module 26 is respectively coupled to the outputs of the
20 envelope detection module 20 and the delay line 24. The error signal generation module 26 is configured to generate an error signal 28 based on a comparison of a segment of the input signal $r(t)$ with a segment of each of the delay signals. An adjustment module 30, coupled to an input of the ADC 12 and to outputs of the clock circuit 16 and the error signal generation module 26, is configured to perform
25 signal period adjustment based on the error signal 28 it receives from the error signal generation module 26.

The input signal $r(t)$ is a continuous periodical signal represented by the following equation:

$$r(t) = \sum_{i=-\infty}^{\infty} S[t + i(T + \Delta)] + n(t), \quad (1),$$

where $S(t)$ is modelled by the following equation:

$$S(t) = \begin{cases} s(t) & 0 < t < T + \Delta \\ 0 & \text{otherwise} \end{cases} \quad (2),$$

$s(t)$ represents a waveform of one (1) segment of the input signal $r(t)$, T represents an ideal period of the input signal $r(t)$, Δ represents a margin of period error, $n(t)$ represents the noise in the input signal $r(t)$, and values of i represent respective segments in the input signal $r(t)$. Because the input signal $r(t)$ is continuous, the number of signal segments is infinite, therefore i extends from $-\infty$ to ∞ .

10 Having described the various components of the signal averaging system 10, the operation of these components will now be described in greater detail below with reference to FIGS. 1 through 5.

FIG. 2 shows a signal averaging method 100. In a first step 102, an input signal $r(t)$ is received and sampled by the ADC 12. Sampling changes the continuous periodical signal received into a discrete signal. FIG. 3 shows a waveform of a sampled signal 32. As can be seen from FIG. 3, the sampled signal 32 includes a plurality of pulses 34 having a period P therebetween.

Referring again to FIGS. 1 and 2, the input signal $r(t)$ is sampled at a sampling rate determined by the clock frequency 14 received at the ADC 12 (i.e. the clock frequency 14 generated by the clock circuit 16 and adjusted by the adjustment module 30). The number of samples drawn from one (1) period of the input signal $r(t)$ is dependent on the period of the input signal $r(t)$ and the sampling rate.

Because the clock frequency 14 generated by the clock circuit 16 is dynamically adjustable by the adjustment module 30, the clock frequency 14 received at the ADC 12 is not uniform and is therefore unsuitable for driving the other modules in the signal averaging system 10 that are driven by a uniform clock frequency, for example, the envelope detection module 20, the waveform accumulator 22, the delay line 24 and the error signal generation module 26. Accordingly, the sampled signal is passed through the FIFO memory 18 to isolate the timing of the sampled signal from that of the other modules at step 104. The FIFO memory 18 acts as a buffer to align the timing of the signal output from the ADC 12 with that of the other modules. The timing of the signal output from the FIFO memory 18 is thus uniform and aligned with the other modules in the signal averaging system 10.

At step 106, a fast change part of the input signal $r(t)$ is filtered out by the envelope detection module 20 as noise. This makes error signal estimation more stable.

A plurality of delayed signals is generated at step 108 by the delay line 24 based on the input signal $r(t)$. The delayed signals are generated by introducing a range of delay values into the input signal $r(t)$, the range of delay values being between about $\bar{D} - \Delta$ and about $\bar{D} + \Delta$, where $\bar{D}$ represents an optimal delay estimate and Δ represents a margin of error. In the present embodiment, the optimal delay estimate $\bar{D}$ is approximately equal to one (1) period of the input signal $r(t)$ and Δ represents a margin of period error.

At step 110, the error signal generation module 26 compares a segment of the input signal $r(t)$ with a segment of each of the delayed signals and generates an error signal 28 based on the comparison.

Referring now to FIG. 4, an approach 50 to determining the error signal 28 is shown. This approach 50 involves generating at step 52 a plurality of delayed

signals 54 by introducing a range of delay values $[\bar{D} - \Delta, \bar{D} + \Delta]$ into the input signal $r(t)$.

At step 56, a correlation calculation is performed between a segment of the input signal $r(t)$ and a segment of each of the delayed signals 54. As shown in FIG. 4, the error signal generation module 26 in this approach 50 includes a correlation module 36 configured to perform the correlation calculation between the segment of the input signal $r(t)$ and a corresponding segment of each of the delayed signals 54. The correlation calculation is performed with the following equation:

$$C(D) = \int_{t=0}^Q f(t)f(t+D)dt \quad (3),$$

where C represents a calculated correlation value, $f(t)$ represents a waveform of a segment of the input signal $r(t)$, $f(t+D)$ represents a waveform of a corresponding segment of each of the delayed signals 54, Q represents a duration of the segment of the input signal $r(t)$, and D represents a delay value introduced into the input signal $r(t)$ and has a value between zero (0) and the duration of the segment Q (i.e. $0 < D < Q$). The correlation value C provides a measure of the similarity between the segment of the input signal $r(t)$ and the corresponding segment of each of the delayed signals 54.

An optimal delay value D_{opt} corresponding to a maximum correlation value calculated is determined at step 58. In one embodiment, the optimal delay value D_{opt} is determined from a correlation curve generated based on the correlation calculation performed. This is exemplified in FIG. 5 which shows a plurality of correlation curves generated in respect of successive segments i , $i+1$, $i+2$ and $i+3$ of the input signal $r(t)$. Each of the correlation curves is obtained from a plot of the calculated correlation values C versus the respective delay values D . The

optimal delay value D_{opt} for each of the segments i , $i+1$, $i+2$ and $i+3$ of the input signal $r(t)$ is determined by reading off the delay value D corresponding to the maximum correlation value for each of the correlation curves. The optimal delay value D_{opt} for each segment i of the input signal $r(t)$ is stored in a memory
 5 (not shown). In an alternative embodiment, the optimal delay value D_{opt} is determined at step 58 with the following equation:

$$D_{opt} = \arg \max_{\bar{D}-\Delta < D < \bar{D}+\Delta} \{C(D)\} \quad (4),$$

where $[\bar{D} - \Delta, \bar{D} + \Delta]$ represents the range of delay values introduced into the input signal $r(t)$.

10 The error signal 28 is generated at step 60 by determining a difference between the optimal delay values D_{opt} for successive segments of the input signal $r(t)$. This is modelled by the following equation:

$$e_i = D_{opt_i} - D_{opt_{i-1}} \quad (5),$$

where e_i represents the error signal 28 for the i th segment of the input signal $r(t)$,
 15 D_{opt_i} represents the optimal delay value for the i th segment of the input signal $r(t)$, and $D_{opt_{i-1}}$ represents the optimal delay value for the $i-1$ th segment of the input signal $r(t)$.

Referring again to FIGS. 1 and 2, signal period adjustment is performed by the adjustment module 30 at step 112 based on the error signal 28 received from
 20 the error signal generation module 26. More particularly, the adjustment module 30 increases or decreases the clock frequency 14 to the ADC 12 according to the error signal 28 it receives. Adjustment of the clock frequency 14 by the adjustment module 30 is described in greater detail below with reference to FIGS. 6A-6C.

FIG. 6A shows a clock frequency 14 from the clock circuit 16 of FIG. 1 prior to any frequency adjustment.

When the error signal 28 indicates that a period of a current segment i of the input signal $r(t)$ is of a longer duration than a period of a preceding segment $i-1$ of the input signal $r(t)$ (i.e. $e_i > 0$), the adjustment module 30 reduces the clock frequency 14 to the ADC 12 to reduce the period of the sampled signal. This is exemplified in FIG. 6B which shows the clock frequency 14 of FIG. 6A after frequency reduction to reduce the sampling rate when the input signal period t_1 is greater than a set optimal signal period t_2 . As can be seen from FIG. 6B, the clock frequency 14 to the ADC 12 is reduced by removing several sampling clock pulses from the clock frequency 14 shown in FIG. 6A.

On the contrary, when the error signal 28 indicates that the period of the current segment i of the input signal $r(t)$ is of a shorter duration than the period of the preceding segment $i-1$ (i.e. $e_i < 0$), the adjustment module 30 increases the clock frequency 14 to the ADC 12 to increase the period of the sampled signal. This is exemplified in FIG. 6C which shows the clock frequency 14 of FIG. 6A after frequency increment to increase the sampling rate when the input signal period t_1 is less than the set optimal signal period t_2 . As can be seen from FIG. 6C, the clock frequency 14 to the ADC 12 is increased by adding several sampling clock pulses 38 to the clock frequency 14 shown in FIG. 6A.

Referring again to FIGS. 1 and 2, the error signal detection method is repeated and signal period adjustment is continually performed until the difference between the optimal delay values D_{opt} for successive segments of the input signal $r(t)$ is eliminated (i.e. $e_i = 0$).

The waveform accumulator 22 performs waveform accumulation at step 114 after signal period adjustment. More particularly, the waveform accumulator 22 accumulates the sampled signal at step 114 after signal period adjustment.

By performing closed-loop dynamical adjustment of the clock frequency 14 to the ADC 12, the period of the sampled signal is stabilised prior to waveform accumulation. This stabilises the shape and enhances the SNR of the accumulated waveform.

Referring now to FIG. 7, a signal averaging system 150 in accordance with another embodiment of the invention is shown. The system 150 includes an ADC 152 driven by a clock frequency generated by a first clock circuit 154. The ADC 152 is configured to sample an input signal $r(t)$. An output of the ADC 152 is coupled via a switch 156 controlled by a pulse acquisition module 158 to an envelope detection module 160 and a memory 162 for storing samples of the input signal $r(t)$. The envelope detection module 160 is configured to filter out a fast change part of the input signal $r(t)$. A delay line 164, coupled to an output of the envelope detection module 160, is configured to generate a plurality of delayed signals based on the input signal $r(t)$. An error signal generation module 166 is respectively coupled to the outputs of the envelope detection module 160 and the delay line 164. The error signal generation module 166 is configured to generate an error signal 168 based on a comparison of a segment of the input signal $r(t)$ with a segment of each of the delay signals. An adjustment module 170, coupled to an input of the memory 162 and to outputs of the error signal generation module 166 and a second clock circuit 172, is configured to perform signal period adjustment based on the error signal 168 it receives from the error signal generation module 166. A waveform accumulator 174 coupled to the memory 162 is configured to perform waveform accumulation.

The input signal $r(t)$ in this embodiment is a burst or packet-based signal represented by the following equation:

$$r(t) = \sum_{i=0}^N S[t + i(T + \Delta)] + n(t), \quad (6),$$

where $S(t)$ is modelled by equation (2), $s(t)$ represents a waveform of one (1) segment of the input signal $r(t)$, T represents an ideal period of the input signal $r(t)$, Δ represents a margin of period error, $n(t)$ represents noise in the input
 5 signal $r(t)$, and i represents a number of segments in the input signal $r(t)$. Because the input signal $r(t)$ is a burst or packet-based signal, it comprises only $(N+1)$ periods. Accordingly, the number of signal segments i is limited to 0 to N .

Having described the various components of the signal averaging system
 150, the operation of these components will now be described in greater detail
 10 below with reference to FIGS. 7 and 8.

FIG. 8 shows a signal averaging method 200. In a first step 202, an input signal $r(t)$ is received by a receiver (not shown) and sampled by the ADC 152. The input signal $r(t)$ is sampled at a sampling rate determined by the clock frequency generated by the first clock circuit 154.

15 The burst or packet-based input signal $r(t)$ is not continuous and is received packet by packet. Each packet typically comprises a header and a data load. The header typically includes a preamble and ID information. The data load of each packet is typically only several signal periods long. When a packet is received, the receiver synchronizes the packet using the preamble in the header of
 20 the packet and verifies if the packet is at its destination at step 204 by checking the ID information in the packet. If it is determined that the packet is at its destination, the switch 156 is switched to an ON position by the pulse acquisition module 158 to transmit the data load of the packet to the envelope detection module 160. Otherwise, the packet is discarded.

At step 206, a fast change part of the acquired input signal $r(t)$ is filtered out by the envelope detection module 160 as noise. This makes error signal estimation more stable.

A plurality of delayed signals is generated at step 208 by the delay line 164 based on the input signal $r(t)$. The delayed signals are generated by introducing a range of delay values into the input signal $r(t)$, the range of delay values being between about $\bar{D} - \Delta$ and about $\bar{D} + \Delta$, where $\bar{D}$ represents an optimal delay estimate and Δ represents a margin of error. In the present embodiment, the optimal delay estimate $\bar{D}$ is approximately equal to one (1) period of the input signal $r(t)$ and Δ represents a margin of period error.

At step 210, the error signal generation module 166 compares a segment of the input signal $r(t)$ with a segment of each of the delayed signals and generates an error signal 168 based on the comparison. More particularly, a correlation calculation is performed between a segment of the input signal $r(t)$ and a corresponding segment of each of the delayed signals with the following equation:

$$C(\delta) = \sum_{x=0}^{I-1} f(x)f(x+\delta) \quad (7),$$

where C represents a calculated correlation value, $f(x)$ represents a waveform of a segment of the input signal $r(t)$, $f(x+\delta)$ represents a waveform of a corresponding segment of each of the delayed signals, values of x represent respective samples in the segment of the input signal $r(t)$, I is an integer representing the number of samples in the segment of the input signal $r(t)$ and is expressed by the following equation:

$$I = \frac{Q}{d} \quad (8),$$

where Q represents a duration of the segment of the input signal $r(t)$ and d represents a period between the samples in the segment, and δ in equation (7) represents a delay value introduced into the input signal $r(t)$ and has a value between zero (0) and the number of samples in the segment I (i.e. $0 < \delta < I$).

5 The correlation value C provides a measure of the similarity between the segment of the input signal $r(t)$ and the corresponding segment of each of the delayed signals. An optimal delay value δ_{opt} corresponding to a maximum correlation value calculated is determined either from a correlation curve generated based on the correlation calculation performed or with the following equation:

$$10 \quad \delta_{opt} = \arg \max_{\overline{D}-\Delta < D < \overline{D}+\Delta} \{C(\delta)\} \quad (9),$$

where $[\overline{D} - \Delta, \overline{D} + \Delta]$ represents the range of delay values introduced into the input signal $r(t)$. The error signal 168 is then generated by determining a difference between the optimal delay values δ_{opt} for successive segments of the input signal $r(t)$. This is modelled by the following equation:

$$15 \quad e_i = \delta_{opt_i} - \delta_{opt_{i-1}} \quad (10),$$

where e_i represents the error signal 168 for the i th segment of the input signal $r(t)$, δ_{opt_i} represents the optimal delay value for the i th segment of the input signal $r(t)$, and $\delta_{opt_{i-1}}$ represents the optimal delay value for the $i-1$ th segment of the input signal $r(t)$.

20 Signal period adjustment is performed by the adjustment module 170 at step 212 based on the error signal 168 received from the error signal generation module 166. Because adjustment of the first clock circuit 154 driving the ADC 152 affects packet head acquisition, the second clock circuit 172 is adjusted by the adjustment module 170 instead. The second clock circuit 172 functions as a

memory writing clock module that generates a clock frequency for memory writing. The clock frequency generated by the second clock circuit 172 is stable prior to period adjustment. In one embodiment, the second clock circuit 172 functions also as a system clock. The adjustment module 170 increases or decreases the clock frequency generated by the second clock circuit 172 according to the error signal 168 it receives. More particularly, the clock frequency from the second clock circuit 172 is reduced when the error signal 168 indicates that a period of a current segment i of the input signal $r(t)$ is of a longer duration than a period of a preceding segment $i-1$ of the input signal $r(t)$ (i.e. $e_i > 0$) and increased when the error signal 168 indicates that the period of the current segment i of the input signal $r(t)$ is of a shorter duration than the period of the preceding segment $i-1$ (i.e. $e_i < 0$). When the clock frequency generated by the second clock circuit 172 is increased, one or more samples in the current segment of the input signal $r(t)$ are saved into the memory 162 more than once. Conversely, when the clock frequency generated by the second clock circuit 172 is reduced, not all the samples in the segment of the input signal $r(t)$ are saved into the memory 162. In this manner, a period-adjusted signal is stored in the memory 162; the signal stored in the memory 162 has substantially the same number of samples in each segment.

The waveform accumulator 174 performs waveform accumulation at step 214 after signal period adjustment. More particularly, all the segments in one (1) packet of the input signal $r(t)$ stored in the memory 162 are summed at step 214 by the waveform accumulator 174 to obtain an accumulated result. Advantageously, because waveform accumulation is performed after signal period adjustment (and hence signal period stabilisation), the shape of the accumulated waveform is stable and SNR of the accumulated waveform is enhanced.

As is apparent from the foregoing description, the period of the input signal $r(t)$ is instantly detected in the signal averaging system 150. Consequently, each

and every period segment of the input signal $r(t)$ in a burst duration can be added together to increase SNR.

Two experiments were conducted to test the performance of the signal averaging system 150 in a Field Programmable Gate Array (FPGA) implementation.

Experiment 1

The set of conditions employed in Experiment 1 are as follows:

1. 10 millisecond (ms) pulse sequence + 10 ms silent period
2. 20 pulses in 10 ms duration
- 10 3. 40 dB attenuation between transmitter and receiver
4. A continuous UWB transceiver

FIG. 9A shows a UWB pulse waveform under the first set of conditions prior to period adjustment and accumulation. FIG. 9B shows the UWB pulse waveform of FIG. 9A after period adjustment and accumulation. The waveform of FIG. 9B is accumulated 15 times. As can be seen from FIGS. 9A and 9B, the accumulated waveform of FIG. 9B has a higher SNR and therefore produces a clearer signal compared to the waveform of FIG. 9A. The peak value of the accumulated waveform shown in FIG. 9B is about ten (10) times that of the waveform shown in FIG. 9A. This result is relatively close to the ideal peak value of fifteen (15) times the original waveform.

FIG. 10A shows 9 individual waveforms under the first set of conditions prior to period adjustment and accumulation. FIG. 10B shows the 9 individual waveforms of FIG. 10A after period adjustment and accumulation. As can be seen, the waveforms of FIG. 10A exhibit poor repeatability: both the period and shape of the waveforms shown in FIG. 10A are substantially dissimilar. In

contrast, the waveforms of FIG. 10B exhibit good repeatability: the period and shape of the waveforms shown in FIG. 10B are stable. Statistical results providing an indication of the stability of the waveforms of FIGS. 10A and 10B are shown in Table 1 below.

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Table 1

	SNR¹ (dB)	Normalized max point STD²	Normalized correlation STD³	Mean waveform similarity⁴
Waveform before period adjustment and accumulation	30.9529	0.0438	0.0116	0.2765
Waveform after period adjustment and accumulation	37.6108	0.0170	0.0015	0.9845

Notes:

1: The SNR of the pulse waveform is estimated on the assumption that the signal and noise are independent of each other and the means of the signal and noise are zero (0), with the following equation:

$$10 \quad SNR = \frac{S_{om}^2 - S_{o0}^2}{S_{o0}^2} \quad (11),$$

where S_{om}^2 represents the power of the signal in the observed peak signal area and is calculated with the following equation:

$$S_{om}^2 = (s_M + n)^2 = s_M^2 + n^2 + 2s_M n = P_M + N0 \quad (12),$$

s_M represents the peak signal amplitude, n represents the noise amplitude, P_M represents the peak signal power, $N0$ represents the noise power, and S_{o0}^2 represents the power of the signal in the signal silent area (i.e. the noise contribution) and is calculated with the following equation:

$$S_{o0}^2 = (s_0 + n)^2 = s_0^2 + n^2 + 2s_0n = N0 \quad (13);$$

2: standard deviation of the peak signal value is calculated as follows:

$$STD(\max(\text{waveform}_i) / \text{Globalmaximum}, i = 1 \text{ to } n);$$

3: standard deviation of the correlation between waveforms is calculated as follows:

$$STD(\max(\text{waveform}_1 \otimes \text{waveform}_i) / \text{mean}(\max(\text{waveform}_1 \otimes \text{waveform}_i)); i = 1 \text{ to } n),$$

where $\otimes$ represents convolution;

4: average similarity of the waveforms is calculated as follows:

$$\text{mean}(\text{sum}(\text{waveform}_1 .* \text{waveform}_i)^2 / (\text{sum}(\text{waveform}_1)^2 \cdot \text{sum}(\text{waveform}_i)^2), i = 2 \text{ to } n),$$

where $.*$ represents respective multiplication of each element in the first vector with each element in the second vector.

Experiment 2

The set of conditions employed in Experiment 2 are as follows:

1. 10 ms pulse sequence + 11 ms silent period
2. 20 pulses in 10 ms duration
3. A packet-based UWB transceiver

4. Distance from the transmitter to receiver: 3.2 metre (m).

FIG. 11A shows 9 individual waveforms under the second set of conditions prior to period adjustment and accumulation. FIG. 11B shows the 9 individual waveforms of FIG. 11A after period adjustment and accumulation. The waveforms of FIG. 11B are accumulated 15 times. As can be seen, the waveforms of FIG. 11A exhibit poor repeatability: both the period and shape of the waveforms shown in FIG. 11A are substantially dissimilar. In contrast, the waveforms of FIG. 11B exhibit good repeatability: the period and shape of the waveforms shown in FIG. 11B are stable. Statistical results providing an indication of the stability of the waveforms of FIGS. 11A and 11B are shown in Table 2 below.

Table 2

	SNR⁰ (dB)	Normalized max point STD¹	Normalized correlation STD²	Mean waveform similarity³
Waveform before period adjustment and accumulation	25.8064	0.0381	0.0136	0.2616
Waveform after period adjustment and accumulation	29.2890	0.0460	0.0062	0.8627

As is evident from the foregoing discussion, the present invention provides a system and method that stabilises a signal received in a communication system. The present invention also provides a signal averaging system and method that yields a higher SNR. Advantageously, the present invention facilitates accurate parameter estimation and data detection at a lower bit error rate. Further advantageously, the present invention is operable independent of multipath distortion.

Unless the context clearly requires otherwise, throughout the description and the claims, the words "comprise", "comprising" and the like are to be construed in an inclusive as opposed to an exclusive or exhaustive sense; that is to say, in the sense of "including, but not limited to".

5 References

- [1]. Phase locked loop principle:
 <http://www.uoguelph.ca/~antoon/gadgets/pll/pll.html>.
- [2]. Yugang Ma, "Multi-Path Suppression Technique for a UWB Positioning System". SRL-ER-FY05-16.
- 10 [3]. John L. Stdnby, Phase-Locked Loops: theory and applications, CRC Pree LLC, 1997.

Claims

1. A signal stabilising method comprising:
receiving an input signal;
generating a plurality of delayed signals based on the input signal;
comparing a segment of the input signal with a segment of each of the delayed signals;
generating an error signal based on the comparison; and
performing signal period adjustment based on the error signal, thereby producing a stabilised version of the input signal.
2. A signal averaging method, comprising:
receiving an input signal;
generating a plurality of delayed signals based on the input signal;
comparing a segment of the input signal with a segment of each of the delayed signals;
generating an error signal based on the comparison;
performing signal period adjustment based on the error signal; and
performing waveform accumulation after signal period adjustment.
3. The method according to claim 1 or 2, further comprising performing a correlation calculation between the segment of the input signal and a corresponding segment of each of the delayed signals.
4. The method according to claim 3, further comprising determining an optimal delay value corresponding to a maximum correlation value calculated.
5. The method according to claim 4, wherein the optimal delay value is determined from a correlation curve generated based on the correlation calculation performed.

6. The method according to claim 5, wherein the step of generating the error signal comprises determining a difference between the optimal delay values for successive segments of the input signal.

7. The method according to any one of the preceding claims, wherein the step of generating the delayed signals comprises introducing a range of delay values into the input signal.

8. The method according to claim 7, wherein the range of delay values is between about $\bar{D} - \Delta$ and about $\bar{D} + \Delta$, where $\bar{D}$ represents an optimal delay estimate and Δ represents a margin of error.

9. The method according to claim 8, wherein the optimal delay estimate $\bar{D}$ is approximately equal to one (1) period of the input signal and Δ represents a margin of period error.

10. The method according to any one of the preceding claims, wherein the step of performing signal period adjustment comprises reducing a clock frequency when the error signal indicates that a period of a current segment of the input signal is of a longer duration than a period of a preceding segment of the input signal, and increasing the clock frequency when the error signal indicates that the period of the current segment is of a shorter duration than the period of the preceding segment.

11. The method according to any one of the preceding claims, further comprising filtering out a fast change part of the input signal.

12. The method according to any one of the preceding claims, further comprising sampling the input signal.

13. The method according to claim 12, further comprising isolating a timing of the sampled signal.

14. The method according to any one of the preceding claims, wherein the input signal is one of a continuous periodical signal and a packet-based signal.

15. A signal stabilising system comprising:
a delay line configured to generate a plurality of delayed signals based on an input signal;
an error signal generation module configured to generate an error signal based on a comparison of a segment of the input signal with a segment of each of the delayed signals; and
an adjustment module configured to perform signal period adjustment based on the error signal, thereby producing a stabilised version of the input signal.

16. A signal averaging system, comprising:
a delay line configured to generate a plurality of delayed signals based on an input signal;
an error signal generation module configured to generate an error signal based on a comparison of a segment of the input signal with a segment of each of the delayed signals;
an adjustment module configured to perform signal period adjustment based on the error signal; and
an accumulator configured to perform waveform accumulation after signal period adjustment.

17. The system according to claim 15 or 16, wherein the error signal generation module includes a correlation module configured to perform a correlation calculation between the segment of the input signal and a corresponding segment of each of the delayed signals.

18. The system according to claim 17, wherein the correlation module is configured to determine an optimal delay value corresponding to a maximum correlation value calculated.

19. The system according to claim 18, wherein the correlation module is configured to determine the optimal delay value from a correlation curve generated based on the correlation calculation performed.

20. The system according to claim 19, wherein the error signal generation module is configured to determine a difference between the optimal delay values for successive segments of the input signal.

21. The system according to any one of claims 15 to 20, wherein the delay line is configured to introduce a range of delay values into the input signal.

22. The system according to claim 21, wherein the delay line is configured to introduce the range of delay values between about $\bar{D} - \Delta$ and about $\bar{D} + \Delta$, where $\bar{D}$ represents an optimal delay estimate and Δ represents a margin of error, into the input signal.

23. The system according to claim 21 or 22, wherein the delay line is configured to introduce the range of delay values between about $\bar{D} - \Delta$ and about $\bar{D} + \Delta$, where $\bar{D}$ is approximately equal to one (1) period of the input signal and Δ represents a margin of period error, into the input signal.

24. The system according to any one of claims 15 to 23, wherein the adjustment module is configured to reduce a clock frequency when the error signal indicates that a period of a current segment of the input signal is of a longer duration than a period of a preceding segment of the input signal, and to

increase the clock frequency when the error signal indicates that the period of the current segment is of a shorter duration than the period of the preceding segment.

25. The system according to any one of claims 15 to 24, further comprising a filter configured to filter out a fast change part of the input signal.

26. The system according to claim 25, wherein the filter comprises an envelope detection module.

27. The system according to any one of claims 15 to 26, further comprising a sampler configured to sample the input signal.

28. The system according to claim 27, wherein the sampler comprises an Analog to Digital Converter (ADC).

29. The system according to claim 27 or 28, further comprising a buffer configured to isolate a timing of the sampled signal.

30. The system according to claim 29, wherein the buffer comprises a First In First Out (FIFO) memory.