CLAIMS

1. A semiconductor package assembly, comprising:

a base plate, having a first surface;

a chip stacking structure, located on the base plate, wherein the chip stacking structure comprises a plurality of chips sequently stacked in a direction perpendicular to the base plate, and is electrically connected to the first surface of the base plate;

an interposer, located on the chip stacking structure and having a first interconnection surface, wherein the first interconnection surface has a first interconnection region and a second interconnection region, and the second interconnection region is electrically connected to the base plate; and

a molding compound, sealing the chip stacking structure, the interposer and the first surface of the base plate, wherein the first interconnection region is not sealed by the molding compound, the second interconnection region is sealed by the molding compound, and there is a preset height between a top surface of the molding compound on the second interconnection region and the first interconnection region;

wherein the base plate further comprises a first signal transmission region, a second signal transmission region and a third signal transmission region, the first signal transmission region and the second signal transmission region are respectively located on two opposite sides of the base plate, the first signal transmission region is electrically connected to the chip stacking structure, the second signal transmission region is electrically connected to the interposer, the first signal transmission region and the second signal transmission region are not connected to each other, the first signal transmission region and the third signal transmission region are connected to each other, the third signal transmission region and the second signal transmission region are not connected to each other;

wherein each chip has a first connection end, the first connection end and the first signal transmission region are located on the same side, a first conductive wire is led out from the first connection end to the first signal transmission region;

wherein a plurality of first pads are formed on the first interconnection region, a plurality of second pads are formed on the second interconnection region, a second conductive wire is led out from the second pads to the second signal transmission region.

2. The semiconductor package assembly of claim 1, wherein

a number of the second pads is greater than a number of the first pads; and an area of each of the second pads is less than an area of each of the first pads.

3. The semiconductor package assembly of claim 1, wherein

an included angle between a sidewall between the top surface of the molding compound and the first interconnection region and a direction perpendicular to the base plate is a first included angle; and the first included angle is greater than or equal to 0° and less than 90°.

4. The semiconductor package assembly of claim 1, wherein

the interposer comprises a base; and an electromagnetic shielding layer is provided in the base.

5. The semiconductor package assembly of claim 1, wherein

in a direction perpendicular to the base plate, the base plate has a first thickness, and the interposer has a second thickness; and the first thickness is greater than the second thickness.

6. The semiconductor package assembly of claim 1, further comprising:

a second package structure, comprising a first solder ball, wherein the first solder ball is electrically connected to the first interconnection region, and a height of the first solder ball is greater than the preset height.

7. A method for manufacturing a semiconductor package assembly, comprising:

providing a base plate, wherein the base plate has a first surface;

forming a chip stacking structure on the base plate, wherein the chip stacking structure comprises a plurality of chips sequently stacked in a direction perpendicular to the base plate, each chip has a first connection end, and is electrically connected to the first surface of the base plate;

forming an interposer on the chip stacking structure, wherein the interposer has a first interconnection surface, the first interconnection surface has a first interconnection region and a second interconnection region, and the second interconnection region is electrically connected to the base plate;

forming a molding compound, wherein the molding compound seals the chip stacking structure, the interposer and the first surface of the base plate, wherein the first interconnection region is not sealed by the molding compound, the second interconnection region is sealed by the molding compound, and there is a preset height between a top surface of the molding compound on the second interconnection region and the first interconnection region;

wherein the base plate further comprises a first signal transmission region, a second signal transmission region and a third signal transmission region, the first signal transmission region and the second signal transmission region are respectively located on two opposite sides of the base plate, the first signal transmission region is electrically connected to the chip stacking structure, the second signal transmission region is electrically connected to the interposer, the first signal transmission region and the second signal transmission region are not connected to each other, the first signal transmission region and the third signal transmission region are connected to each other, the third signal transmission region and the second signal transmission region are not connected to each other, the first connection end and the first signal transmission region are located on the same side;

forming a first conductive wire, the first conductive wire is led out from the first connection end to the first signal transmission region, wherein each chip is electrically connected to the base plate via the first conductive wire; and

forming a plurality of first pads on the first interconnection region, forming a plurality of second pads on the second interconnection region, forming a second conductive wire, the second conductive wire is led out from the second pads to the second signal transmission region, wherein the second interconnection region is electrically connected to the base plate via the second conductive wire.

8. The method of claim 7, wherein the forming an interposer on the chip stacking structure comprises:

providing the interposer, wherein a bottom of the interposer is provided with an adhesive layer, and the interposer is adhered to the chip stacking structure via the adhesive layer.

9. The method of claim 7, wherein

a number of the second pads is greater than a number of the first pads, and an area of each of the second pads is less than an area of each of the first pads.

10. The method of claim 7, further comprising:

forming the interposer, and then forming a covering layer with a preset height on the first interconnection region of the interposer, wherein an included angle between a sidewall of the covering layer and the direction perpendicular to the base plate is a first included angle; and the first included angle is greater than or equal to 0° and less than 90°.

11. The method of claim 10, further comprising:

forming the covering layer, and then forming a first packaging mold, wherein a surface of the first packaging mold is parallel to a surface of the base plate, the first packaging mold is located above the covering layer and has a certain distance from the covering layer.

12. The method of claim 11, further comprising:

forming a molding compound pre-layer for sealing the chip stacking structure, the interposer, the covering layer and the first surface of the base plate by using the first packaging mold as a mask;

exposing the covering layer by removing part of the molding compound pre-layer; and

exposing the first interconnection region by removing the covering layer.

13. The method of claim 7, further comprising:

forming a second package structure, and forming a first solder ball on the second package structure, wherein the first solder ball is electrically connected to the first interconnection region, and a height of the first solder ball is greater than the preset height.