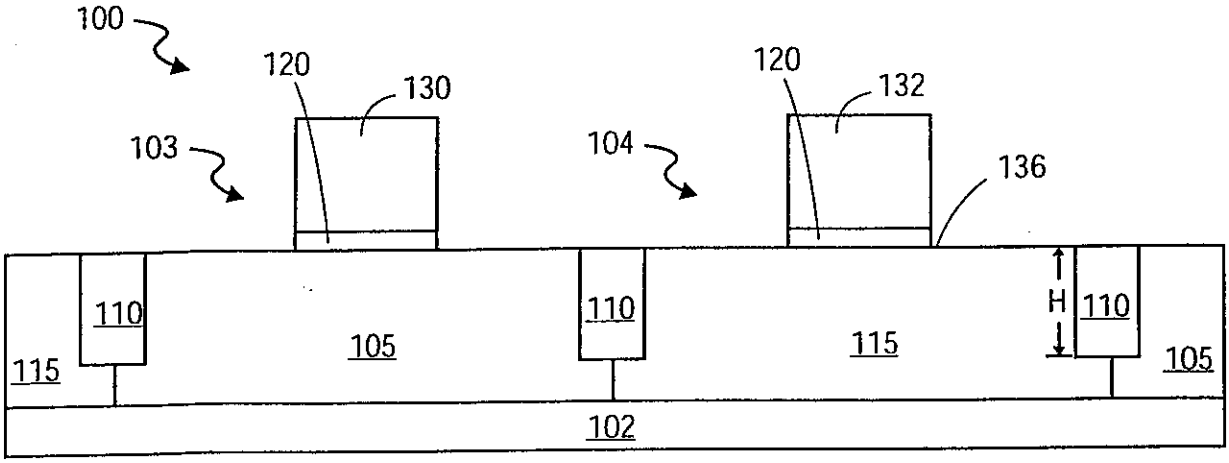

100
120
130
103
104
120
132
136
110
110
H
110
105
115
115
105
102

FIG. 1

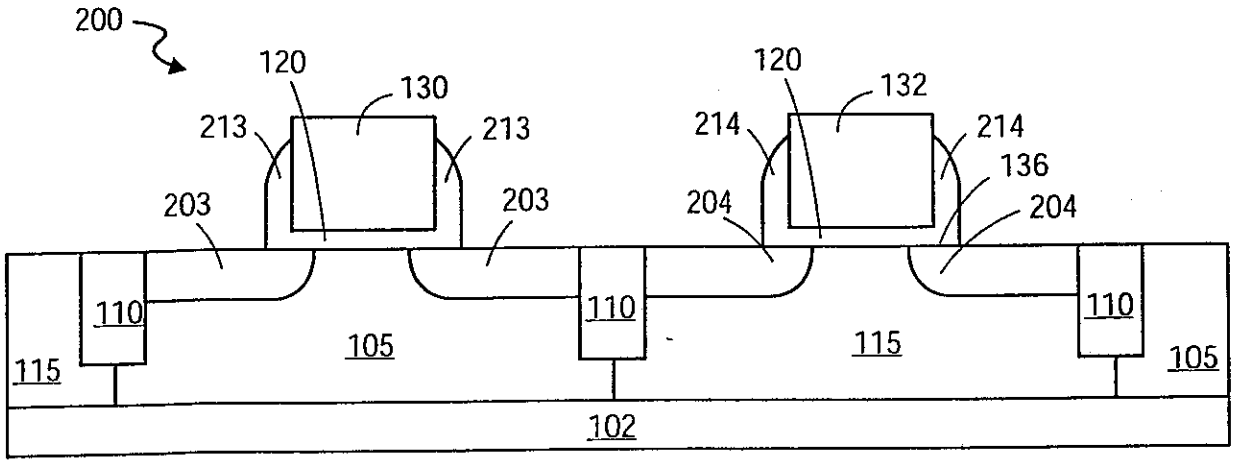

200
120
130
213
213
203
203
120
132
214
214
136
204
204
110
110
110
105
115
115
105
102

FIG. 2

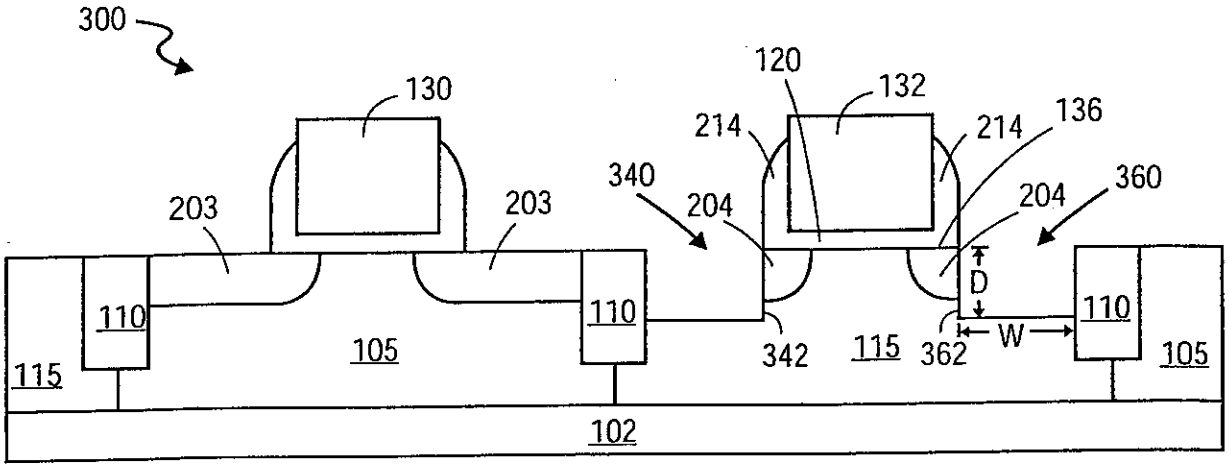


FIG. 3

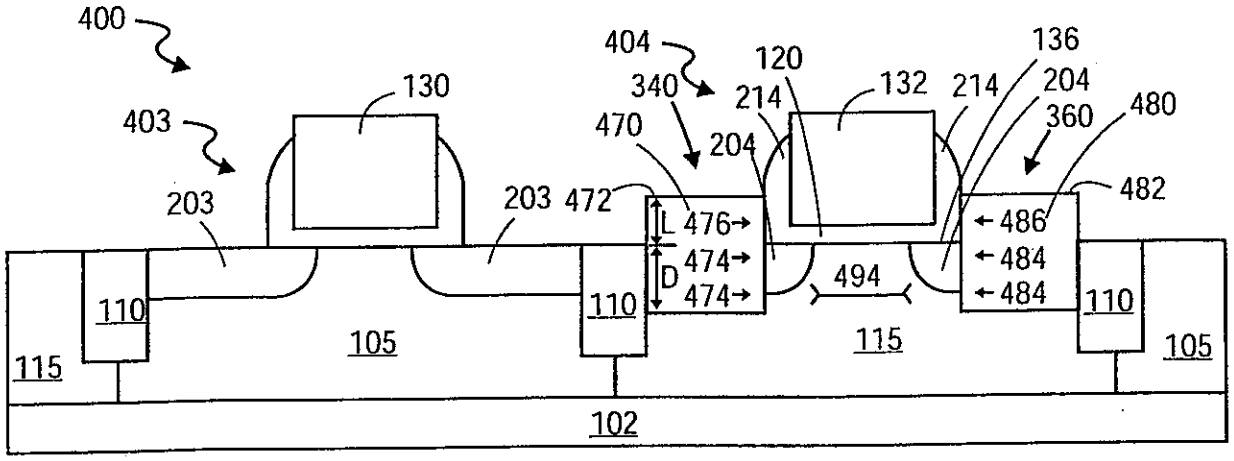


FIG. 4

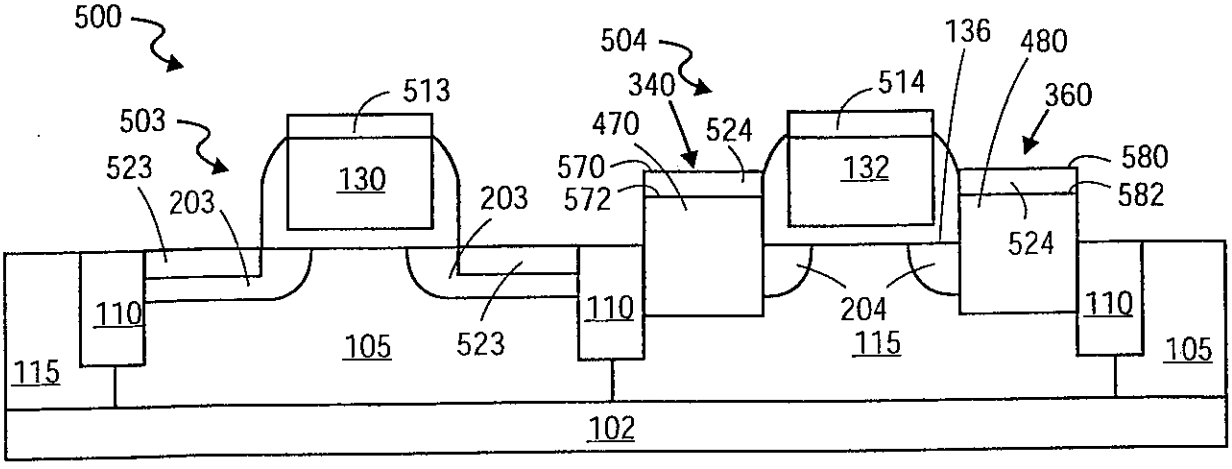


FIG. 5

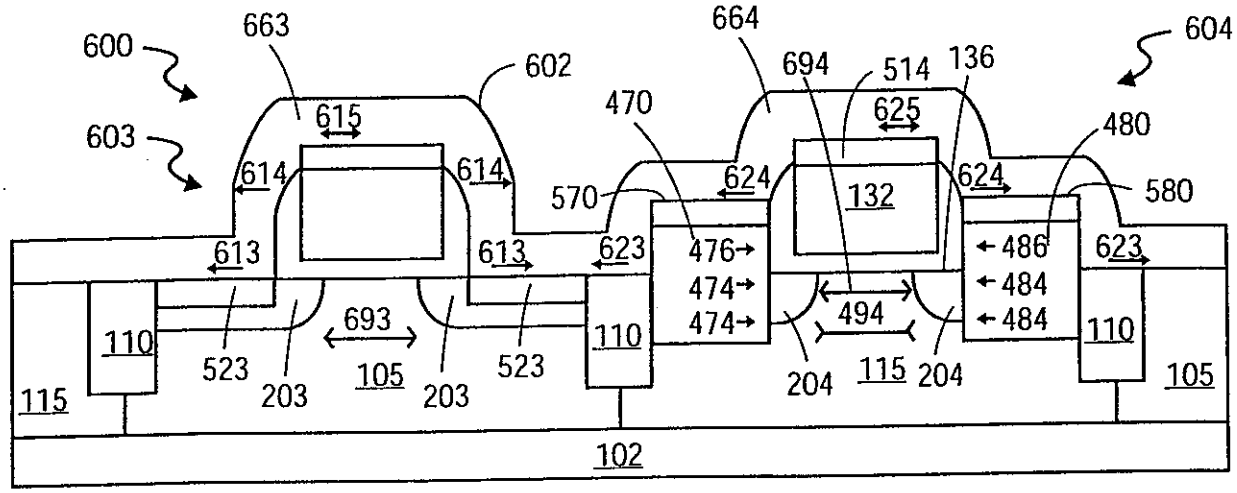

600
603
663
615
614
614
602
613
613
623
664
694
514
136
604
625
480
470
570
624
624
580
132
476→
474→
474→
←486
←484
←484
623
494
693
105
523
203
203
523
110
110
110
115
115
204
204
105
102

FIG. 6

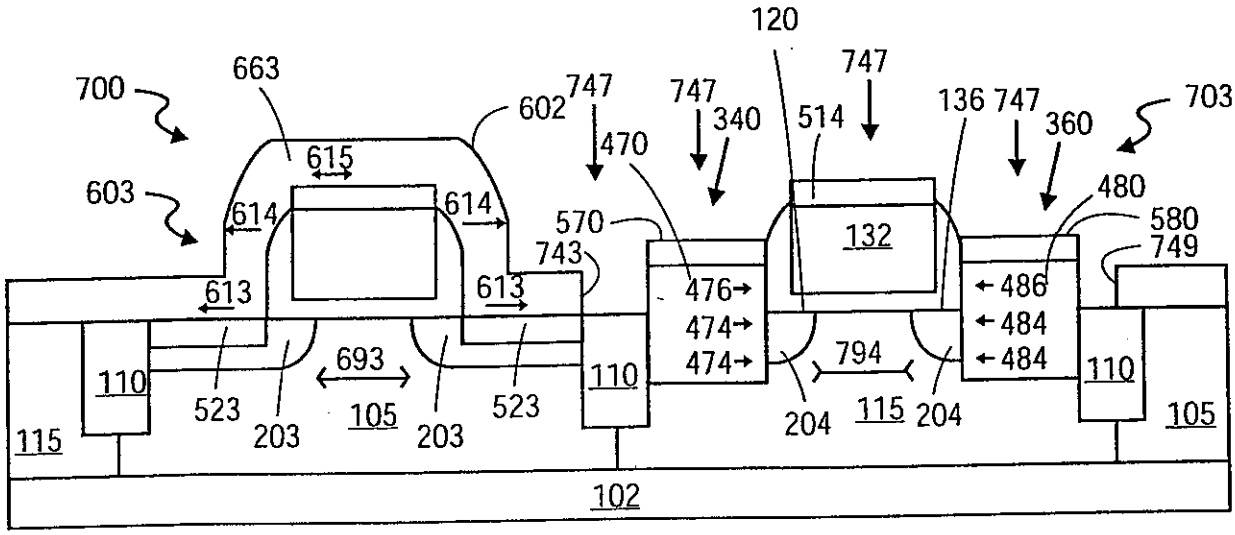

700
603
663
615
614
614
602
747
747
747
120
747
136
747
703
340
514
360
470
480
570
580
132
743
749
613
613
476→
474→
474→
←486
←484
←484
794
693
105
523
203
203
523
110
110
110
115
115
204
204
105
102

FIG. 7

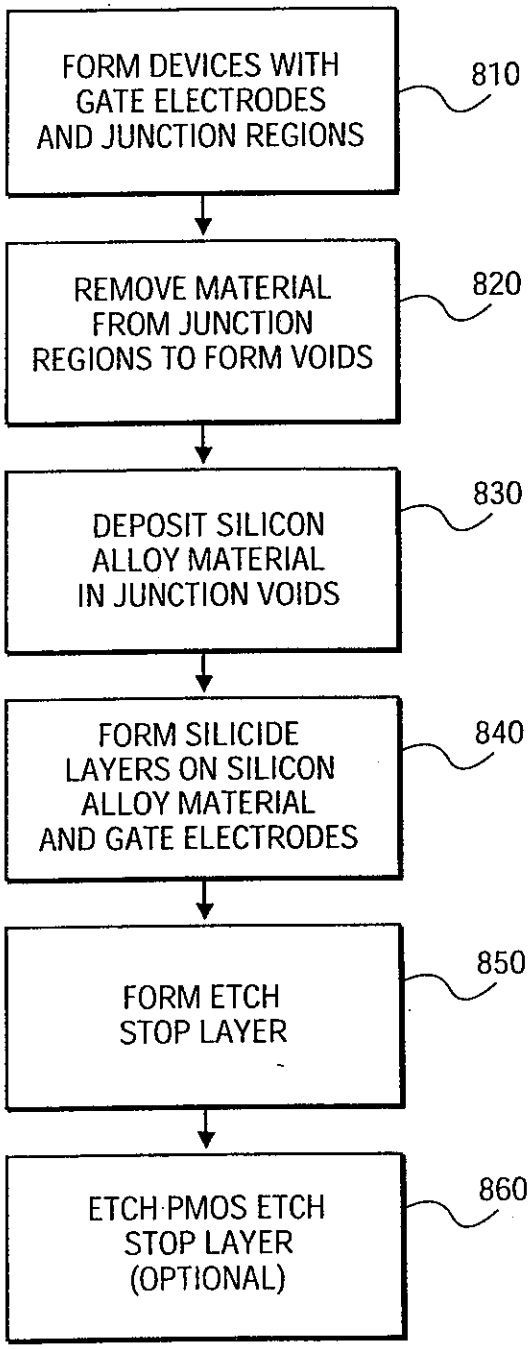

FORM DEVICES WITH GATE ELECTRODES AND JUNCTION REGIONS
810
REMOVE MATERIAL FROM JUNCTION REGIONS TO FORM VOIDS
820
DEPOSIT SILICON ALLOY MATERIAL IN JUNCTION VOIDS
830
FORM SILICIDE LAYERS ON SILICON ALLOY MATERIAL AND GATE ELECTRODES
840
FORM ETCH STOP LAYER
850
ETCH PMOS ETCH STOP LAYER (OPTIONAL)
860

FIG. 8