

CLAIMS

1. A structure comprising:
 - an array of memory cells, a memory cell comprises:
 - at least one metal-oxide-semiconductor (MOS) element, wherein a source terminal of the at least one MOS element is connected to a drain terminal of the MOS element, the source terminal being connected to the drain terminal causes the at least one MOS element to exhibit capacitive behavior for storing electrical energy;
 - a first transistor connected to the at least one MOS element, wherein activation of the first transistor facilitates a write operation to the memory cell; and
 - a second transistor connected to the at least one MOS element, wherein activation of the second transistor facilitates a read operation from the memory cell.
2. The structure of claim 1, wherein the electrical energy being stored in a column of the memory cells is accumulated to represent a weight in an artificial neural network.
3. The structure of claim 1, wherein the at least one MOS element comprises a first p-channel metal-oxide-semiconductor (PMOS) transistor, a second PMOS transistor, a first NMOS transistor, and a second NMOS transistor.
4. The structure of claim 3, wherein the first PMOS transistor and the second PMOS transistor are connected in parallel, the first NMOS transistor and the second NMOS transistor are connected in parallel.
5. The structure of claim 1, wherein:
 - the first transistor is a first NMOS transistor;
 - the second transistor is a second NMOS transistor;
 - a drain terminal of the first NMOS transistor is connected to a bit line true (BLT) wire;
 - a source terminal of the first NMOS transistor is connected to the at least one MOS element;
 - a drain terminal of the second NMOS transistor is connected to the at least one MOS element; and
 - a source terminal of the second NMOS transistor is connected to a bit line complimentary (BLC) wire.
6. The structure of claim 5, wherein:
 - a gate of the first NMOS transistor is controlled by a first clock signal;
 - a gate of the second NMOS transistor is controlled by a second clock signal;
 - in response to the first clock signal activating the first NMOS transistor, an input from the BLT wire is transmitted to the at least one MOS element; and
 - in response to the second clock signal activating the second NMOS, a voltage difference between the BLT wire and the BLC wire is outputted.

7. The structure of claim 1, further comprising at least one circuit configured to bias the capacitance of the at least one MOS element.
8. The structure of claim 1, wherein the array of memory cells is integrated with a non-volatile memory.
9. The structure of claim 1, further comprising a plurality of analog circuits configured to accumulate and store electrical energy outputted from a corresponding column of memory cells.
10. A system comprising:
 - a memory;
 - a processor configured to be in communication with the memory;
 - a structure as claimed in any preceding claim, configured to be in communication with the memory and the processor.
11. A memory device comprising:
 - a non-volatile memory configured to store data; and,
 - a structure as claimed in any of claims 1 to 9 coupled to the non-volatile memory.