



HIGH SPEED DYNAMIC BINARY INCREMENTER

ABSTRACT

6 A high speed dynamic binary incrementer (100) is provided that requires only
two stages regardless of the bit width of the incrementer (100). The binary incrementer
(100) utilizes the inverse of logical carry expressions to provide for a first stage. A
sum stage receives the inverted carry and the input signals to provide the incremented
value. Dynamic wired OR Logic is utilized advantageously to provide the dynamic
10 binary incrementer (100).

Figure 2