CLAIMS

1. A read-write conversion circuit, comprising:

a read-write conversion module, configured to perform a read-write operation in response to a read-write control signal;

a control module, configured to output a variable read-write control signal in response to a read-write speed configuration signal to control a speed of the read-write operation of the read-write conversion module to be variable; and

a local data line, a local complementary data line, and a global data line, wherein, during the read-write operation, data transmission is performed between each of the local data line and the local complementary data line and the global data line, and data signals of the local data line and the local complementary data line are opposite in phase;

wherein the read-write conversion module comprises a local read-write unit, configured to perform a local read-write operation in response to a local read-write control signal in the read-write control signal;

wherein the local read-write unit comprises a local write conversion circuit, configured to transmit data of the global data line to the local data line and the local complementary data line in response to a local write control signal in the local read-write control signal, wherein the local write conversion circuit comprises:

a fifth NMOS transistor, a sixth NMOS transistor, and a seventh NMOS transistor, wherein a drain of the fifth NMOS transistor is connected with the local complementary data line, a gate of the fifth NMOS transistor is connected with a source of the seventh NMOS transistor, and a source of the fifth NMOS transistor is connected with a drain of the sixth NMOS transistor, wherein a gate of the sixth NMOS transistor receives a local write signal in the local write control signal, while a source is grounded,

wherein a drain of the seventh NMOS transistor is connected with the local data line, while a gate receives the local write signal.

2. The read-write conversion circuit of claim 1, further comprising a speed configuration module, connected with the control module and configured to output the read-write speed configuration signal to the control module.

3. The read-write conversion circuit of claim 2, wherein the read-write control signal comprises a read control signal and a write control signal, the read-write conversion module performs a read operation in response to the read control signal, and performs a write operation in response to the write control signal,

Wherein the speed configuration module comprises:

a read speed configuration unit, configured to output a read speed configuration signal in the read-write speed configuration signal to the control module to cause the control module to output a variable read control signal in response to the read speed configuration signal to control a speed of the read operation to be variable, and

a write speed configuration unit, configured to output a write speed configuration signal in the read-write speed configuration signal to the control module to cause the control module to output a variable write control signal in response to the read speed configuration signal to control a speed of the write operation to be variable.

4. The read-write conversion circuit of claim 1, wherein the control module comprises a local control unit, configured to output a variable local read-write control signal in response to a local read-write speed configuration signal in the read-write speed configuration signal to control a speed of the local read-write operation of the local

read-write unit to be variable.

5. The read-write conversion circuit of claim 4, further comprising a local speed configuration module, connected with the local control unit and configured to output the local read-write speed configuration signal to the local control unit.

6. The read-write conversion circuit of claim 4, further comprising a sense amplifier, connected with the local read-write unit through the local data line and the local complementary data line and configured to sense a voltage of a bit line.

7. The read-write conversion circuit of claim 6, wherein a same local read-write unit is connected with multiple sense amplifiers through the local data line and the local complementary data line.

8. The read-write conversion circuit of claim 6, wherein a write data path is from the local read-write unit to the sense amplifier via the local data line and the local complementary data line, and then to the bit line via the sense amplifier; and a read data path is from the bit line to the local data line and the local complementary data line via the sense amplifier, and then to the local read-write unit via the local data line and the local complementary data line.

9. The read-write conversion circuit of claim 1, wherein the read-write conversion module comprises a global read-write unit, configured to perform a global read-write operation in response to a global read-write control signal in the read-write control

signal; and the control module comprises a global control unit, configured to output a variable global read-write control signal in response to a global read-write speed configuration signal in the read-write speed configuration signal to control a speed of the global read-write operation of the global read-write unit to be variable.

10. The read-write conversion circuit of claim 9, further comprising a global speed configuration module, connected with the global control unit and configured to output the global read-write speed configuration signal to the global control unit.

11. The read-write conversion circuit of claim 4, wherein the local read-write unit comprises a local amplifier, connected between the local data line and the local complementary data line and configured to amplify data of the local data line and data of the local complementary data line.

12. The read-write conversion circuit of claim 11, wherein the local amplifier comprises: a first phase inverter, wherein a first input end of the first phase inverter is electrically connected with the local data line, and a first output end of the first phase inverter is electrically connected with the local complementary data line; and a second phase inverter, wherein a second input end of the second phase inverter is electrically connected with the first output end of the first phase inverter and the local complementary data line, and a second output end of the second phase inverter is electrically connected with the first input end of the first phase inverter and the local data line.

13. The read-write conversion circuit of claim 12, wherein the first phase inverter

comprises a first P-channel Metal Oxide Semiconductor (PMOS) transistor and a first N-channel Metal Oxide Semiconductor (NMOS) transistor, wherein a gate of the first PMOS transistor is connected with a gate of the first NMOS transistor to serve as the first input end of the first phase inverter, a source of the first PMOS transistor is connected with working power, and a drain of the first PMOS transistor is connected with a drain of the first NMOS transistor to serve as the first output end of the first phase inverter; wherein the second phase inverter comprises a zeroth PMOS transistor and a zeroth NMOS transistor, wherein a gate of the zeroth PMOS transistor is connected with a gate of the zeroth NMOS transistor to serve as the second input end of the second phase inverter, a source of the zeroth PMOS transistor is connected with the working power, and a drain of the zeroth PMOS transistor is connected with a drain of the zeroth NMOS transistor to serve as the second output end of the second phase inverter.

14. The read-write conversion circuit of claim 4, wherein the local read-write unit comprises a local read conversion circuit, configured to transmit the data of the local data line and the local complementary data line to the global data line in response to a local read control signal in the local read-write control signal, wherein the local read conversion circuit comprises:

a third NMOS transistor and a fourth NMOS transistor, wherein a drain of the third NMOS transistor is connected with the global data line, a gate of the third NMOS transistor is connected with the local complementary data line, and a source of the third NMOS transistor is connected with a drain of the fourth NMOS transistor, wherein a gate of the fourth NMOS transistor receives a local read signal in the local read control signal, while a source is grounded.

15. The read-write conversion circuit of claim 14, further comprising a global

complementary data line, wherein during the read operation data signals of the global complementary data line and data signals of the global data line are opposite in phase; wherein the local read conversion circuit further comprises an eighth NMOS transistor and a ninth NMOS transistor, wherein a drain of the eighth NMOS transistor is connected with the global complementary data line, a gate of the eighth NMOS transistor is connected with the local data line, and a source of the eighth NMOS transistor is connected with a drain of the ninth NMOS transistor, wherein a gate of the ninth NMOS transistor receives the local read signal, while a source is grounded.

16. The read-write conversion circuit of claim 1, further comprising a global complementary data line, wherein during the read-write operation data signals of the global complementary data line and data signals of the global data line are opposite in phase; wherein the local write conversion circuit further comprises a tenth NMOS transistor, an eleventh NMOS transistor, and a twelfth NMOS transistor, wherein a drain of the tenth NMOS transistor is connected with the local data line, a gate of the tenth NMOS transistor is connected with a source of the twelfth NMOS transistor and the global complementary data line, and a source of the tenth NMOS transistor is connected with a drain of the eleventh NMOS transistor, wherein a gate of the eleventh NMOS transistor receives the local write signal, while a source is grounded, wherein a drain of the twelfth NMOS transistor is connected with the local complementary data line, while a gate receives the local write signal.

17. The read-write conversion circuit of claim 4, wherein the local read-write unit further comprises a precharging circuit, connected between the local data line and the local complementary data line and configured to precharge the local data line and the local complementary data line in response to a precharging control signal.

18. A memory, comprising the read-write conversion circuit of any one of claims 1-17.