## CLAIMS

WHAT IS CLAIMED IS:

1. A flip-flop comprising:

an input switching circuit configured to,

output an intermediate signal based on an input signal and at least one of a phase of a clock signal or a phase of an inverted clock signal, the phase of the inverted clock signal being opposite to the phase of the clock signal, and

block application of a driving voltage to at least one circuit element of the input switching circuit in response to receiving a reset signal representing a reset operation of the flip-flop; and

a latch circuit configured to generate an output signal based on the intermediate signal according to the at least one of the phase of the clock signal or the phase of the inverted clock signal,

wherein the input switching circuit comprises:

a switching circuit configured to output the intermediate signal based on the input signal and the at least one of the phase of the clock signal or the phase of the inverted clock signal; and

a blocking circuit configured to selectively block application of the driving voltage to the switching circuit according to a logic level of the reset signal.

2. The flip-flop of claim 1, wherein the blocking circuit comprises:

a PMOS transistor including a gate configured to receive the reset signal, a source connected to a driving voltage node, and a drain connected to the switching circuit.

3. The flip-flop of claim 1 or claim 2, wherein the switching circuit comprises:

a tri-state inverter configured to output the input signal inverted based on the clock signal and the inverted clock signal as the intermediate signal.

4. The flip-flop of claim 1, wherein the input switching circuit comprises:

a ground connecting circuit connected between a ground node and a middle node, the middle node being connected to the input switching circuit and the latch circuit, and the ground connecting circuit being configured to selectively connect the middle node to the ground node according to the logic level of the reset signal.

5. The flip-flop of claim 4, wherein the ground connecting circuit comprises:

an NMOS transistor including a gate configured to receive the reset signal, a source connected to the ground node, and a drain connected to the middle node.

6. A flip-flop comprising:

an input switching circuit configured to output an intermediate signal based on an input signal and at least one of a phase of a clock signal or a phase of an inverted clock signal, the phase of the inverted clock signal being opposite to the phase of the clock signal;

a latch circuit configured to generate an output signal based on the intermediate signal according to the at least one of the phase of the clock signal or the phase of the inverted clock signal; and

a blocking circuit configured to block application of a driving voltage to at least one first transistor included in the input switching circuit and at least one second transistor included in the latch circuit in response to receiving a reset signal representing a reset operation of the flip-flop.

7. The flip-flop of claim 6, wherein the blocking circuit comprises:

a PMOS transistor including a gate configured to receive the reset signal, a source connected to a driving voltage node, and a drain connected to the input switching circuit and the latch circuit.

8. The flip-flop of claim 6 or claim 7, wherein the input switching circuit comprises:

a tri-state inverter configured to output the input signal inverted based on the clock signal and the inverted clock signal as the intermediate signal.

9. The flip-flop of any one of claims 6 to 8, wherein the input switching circuit comprises:

a ground connecting circuit connected between a ground node and a middle node, the middle node being connected to the input switching circuit and the latch circuit, and the ground connecting circuit being configured to selectively connect the middle node to the ground node according to a logic level of the reset signal.

10. A master-slave flip-flop comprising:

a master latch including,

a master input switching circuit configured to,

output a master intermediate signal to a master middle node based on a master input signal and at least one of a phase of a clock signal or a phase of an inverted clock signal, the phase of the inverted clock signal being opposite to the phase of the clock signal, and

block charging of the master middle node in response to receiving a reset signal having a logic level, and

a master latch circuit connected to the master middle node, the master latch circuit being configured to output a slave input signal based on the master intermediate signal; and

a slave latch configured to output an output signal synchronized with the at least one of the clock signal or the inverted clock signal based on the slave input signal provided from the master latch.

11. The master-slave flip-flop of claim 10, wherein the master input switching circuit comprises:

a master switching circuit configured to output the master intermediate signal based on the master input signal and the at least one of the phase of the clock signal or the phase of the inverted clock signal; and

a first blocking circuit configured to selectively block application of a driving voltage to the master switching circuit according to the logic level of the reset signal.

12. The master-slave flip-flop of claim 11, wherein the first blocking circuit comprises:

a PMOS transistor including a gate configured to receive the reset signal, a source connected to a driving voltage node, and a drain connected to the master switching circuit.

13. The master-slave flip-flop of claim 11 or claim 12, wherein the master switching circuit comprises:

a tri-state inverter configured to output the master input signal inverted based on the clock signal and the inverted clock signal as the master intermediate signal.

14. The master-slave flip-flop of claim 10, wherein the slave latch comprises:

a slave input switching circuit configured to output a slave intermediate signal to a slave middle node based on the slave input signal and the at least one of the phase of the clock signal or the phase of the inverted clock signal; and

a slave latch circuit connected to the slave middle node, the slave latch circuit being configured to output the output signal based on the slave intermediate signal.

15. The master-slave flip-flop of claim 14, wherein the slave input switching circuit comprises:

a slave switching circuit configured to output the slave intermediate signal based on the slave input signal and the at least one of the phase of the clock signal or the phase of the inverted clock signal; and

a second blocking circuit configured to selectively block application of a driving voltage to the slave switching circuit according to the logic level of the reset signal.

16. The master-slave flip-flop of any one of claims 10 to 15, wherein the master latch comprises:

a ground connecting circuit connected between a ground node and the master middle node, the master middle node being connected to the master input switching circuit and the master latch circuit, and the ground connecting circuit being configured to selectively connect the master middle node to the ground node according to the logic level of the reset signal.

17. The master-slave flip-flop of claim 16, wherein the ground connecting circuit comprises:

an NMOS transistor including a gate configured to receive the reset signal, a source connected to the ground node, and a drain connected to the master middle node.

18. The master-slave flip-flop of claim 10, wherein the master latch circuit comprises:

a third blocking circuit configured to block application of a driving voltage to at least one circuit element of the master latch circuit in response to receiving the reset signal representing a reset operation of the master-slave flip-flop.

19. The master-slave flip-flop of claim 18, wherein the third blocking circuit comprises:

a PMOS transistor including a gate configured to receive the reset signal, a source connected to a driving voltage node, and a drain connected to at least one transistor of the master latch circuit.