

15 FEB 2005

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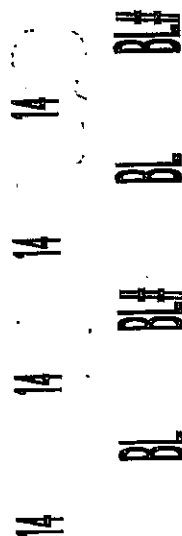
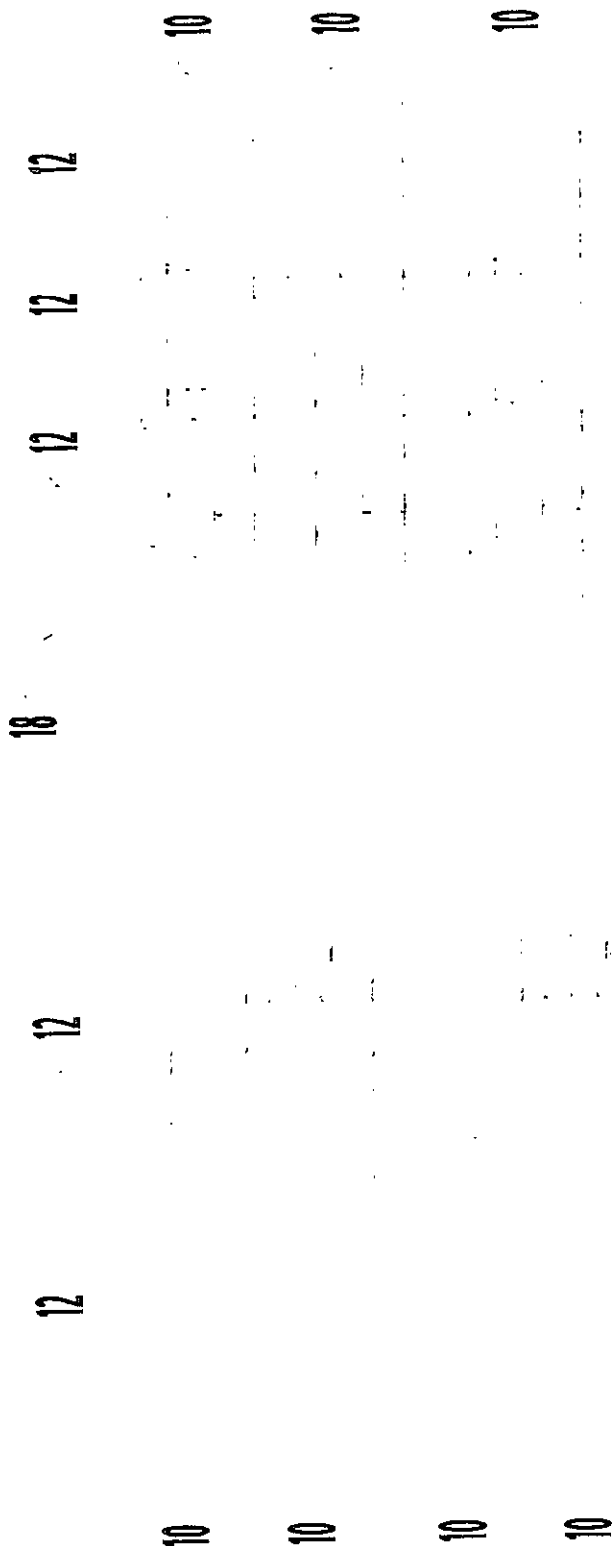


Fig. 2 (Prior Art)

Fig. 1 (Prior Art)

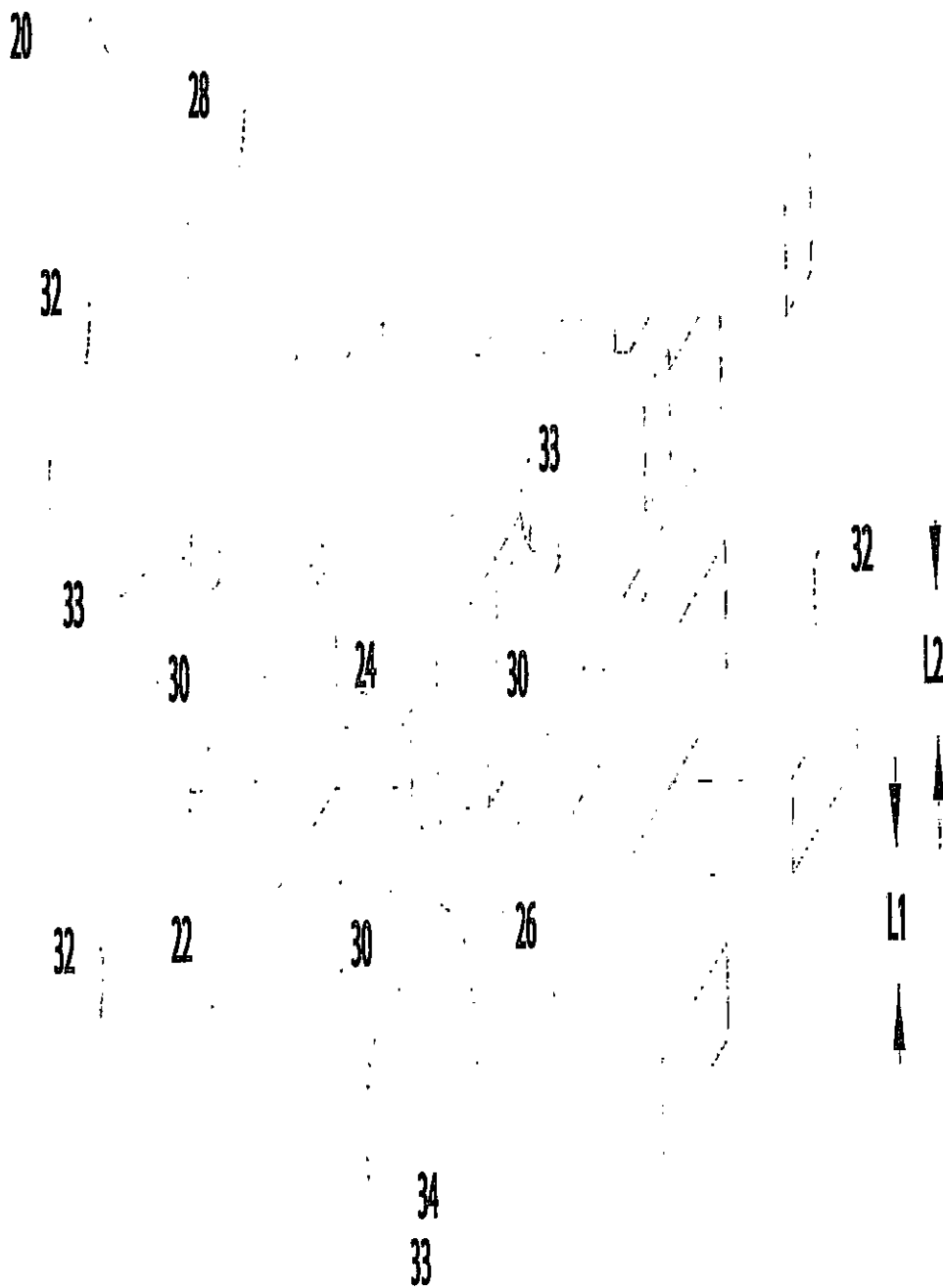


Fig.3

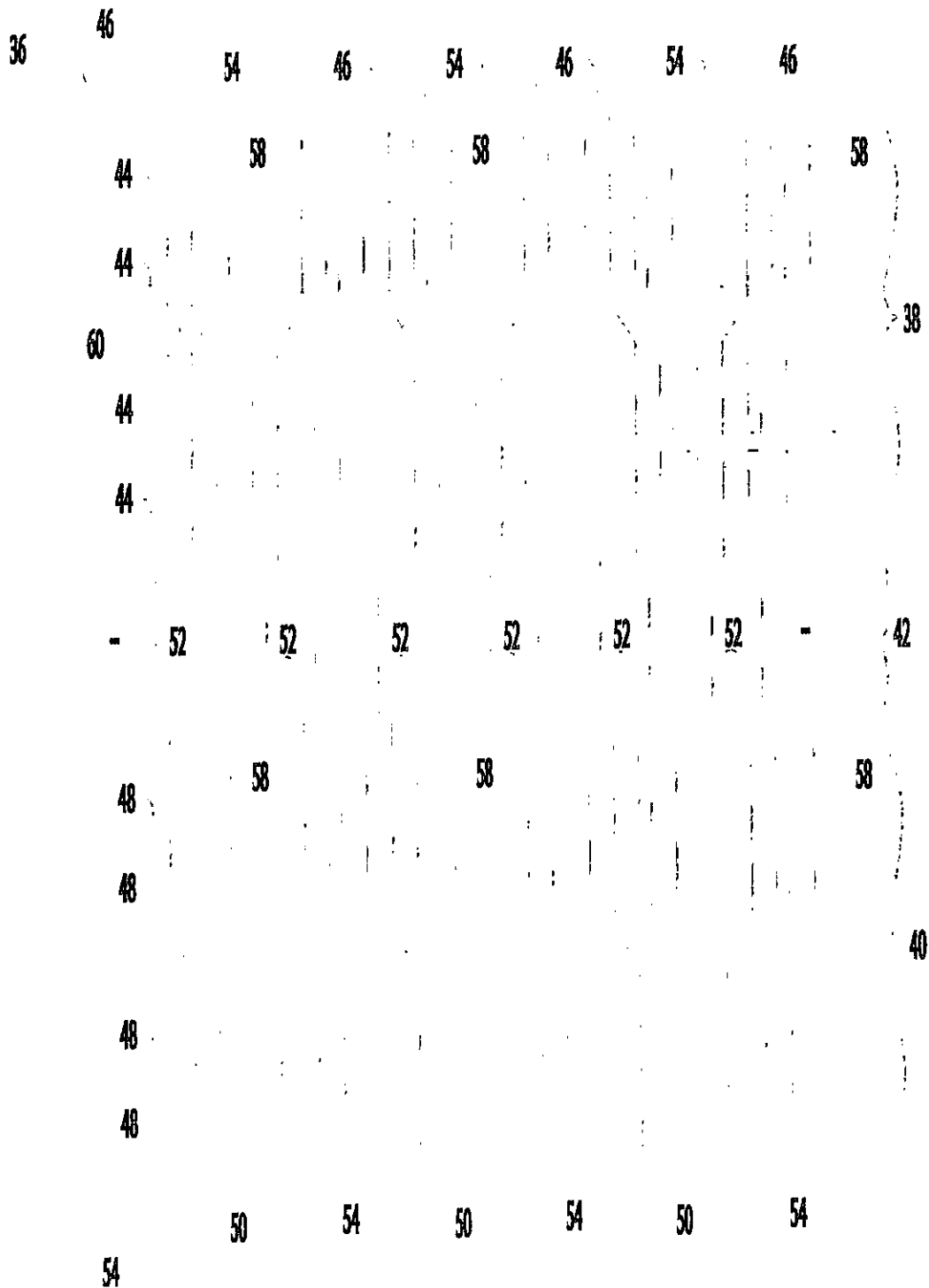


Fig.4

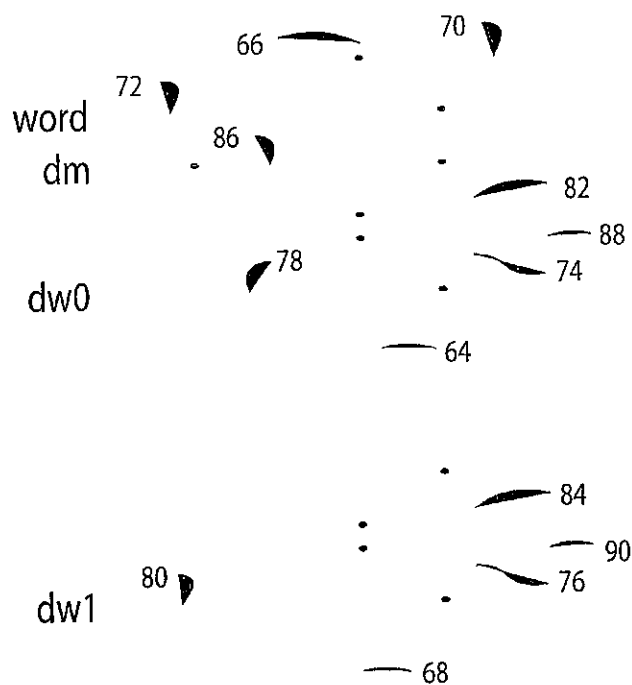


Fig.5

clock
equalize
trim
dm
dw1
word
bit line
voltages

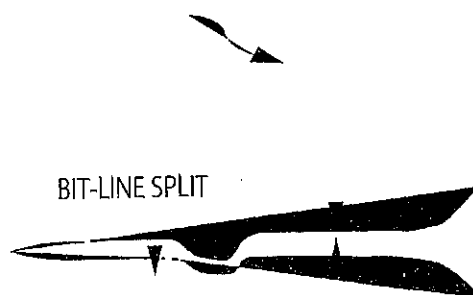


Fig.6