package 164 is mounted over PCB 168. Conductive layer ~~148~~146a is electrically connected through base leads 140a-140b to contact pads 170 formed over PCB 168. Bumps 158 are electrically connected to contact pads 172 formed over PCB 168.

FIG. 6 shows another embodiment of semiconductor package 174, similar to FIGs. 4a-4j, with a plurality of vias formed through semiconductor die 124 while in wafer form, see FIGs. 3a-3c, using laser drilling, mechanical drilling, or deep reactive ion etching (DRIE). The vias are filled with Al, Cu, Sn, Ni, Au, Ag, titanium (Ti), tungsten (W), poly-silicon, or other suitable electrically conductive material using electrolytic plating, electroless plating process, or other suitable metal deposition process to form z-direction vertical conductive through silicon vias (TSV) 175. Encapsulant 150 is planarized with a grinder down to back surface 128 of semiconductor die 124 to expose conductive TSV 175.

A semiconductor die 176 has active surface 178 containing analog or digital circuits implemented as active devices, passive devices, conductive layers, and dielectric layers formed within the die and electrically interconnected according to the electrical design and function of the die. For example, the circuit may include one or more transistors, diodes, and other circuit elements formed within active surface 178 to implement analog circuits or digital circuits, such as DSP, ASIC, memory, or other signal processing circuit. Semiconductor die 176 may also contain IPDs, such as inductors, capacitors, and resistors, for RF signal processing. In one embodiment, semiconductor die 176 is a flipchip type semiconductor die. Contact pads 180 are formed on active surface 178 and electrically connected to the circuits on the active surface. A plurality of bumps 184 is formed over contact

Claims

What is claimed:

1. A semiconductor device, comprising:

a base substrate including a conductive base material and first and second opposing surfaces;

a first conductive layer formed over the first surface of the base substrate and including a first contact pad, a second contact pad, and a conductive trace extending from the first contact pad to the second contact pad;

a second conductive layer including an etch-resistant material formed over the second surface of the base substrate, wherein portions of the base substrate form ~~are electrically~~ isolated ~~to form~~ base leads from the conductive base material disposed between the first conductive layer and second conductive layer including a first base lead extending from the second contact pad of the first conductive layer to a third contact pad of the second conductive layer;

a first semiconductor die ~~disposed over the first conductive layer~~ mounted to the first conductive layer including a first conductive bump of the first semiconductor die bonded to the first contact pad of the first conductive layer, wherein the second contact pad is located outside a footprint of the first semiconductor die;

an encapsulant deposited over the first semiconductor die and first conductive layer; and

a second semiconductor die ~~disposed over the first conductive layer between the base leads~~ mounted to the first conductive layer opposite the first semiconductor die and between the base leads including a second conductive bump of the

second semiconductor die bonded to the first contact pad of the first conductive layer directly opposite the first conductive bump.

~~2. The semiconductor device of claim 1, wherein the first semiconductor die and second semiconductor die are electrically coupled to opposite sides of a portion of the first conductive layer.~~

~~3~~2. The semiconductor device of claim 1, wherein a height of the base leads is greater than a thickness of the second semiconductor die.

~~4. The semiconductor device of claim 1, wherein the first conductive layer and second conductive layer include an etch-~~

~~resistant material.~~

~~5~~3. The semiconductor device of claim 1, further including a third semiconductor die disposed over a top surface of the first semiconductor die, wherein the top surface of the semiconductor die is coplanar with a top surface of the encapsulant.

~~6~~4. The semiconductor device of claim ~~1~~3, further including a plurality of conductive vias formed through the first semiconductor die, wherein the third semiconductor die is electrically connected to the conductive vias.

~~7~~5. A semiconductor device, comprising:

a base substrate;

a first conductive layer formed ~~over~~ directly on a first surface of the base substrate and including a first contact pad, a second contact pad, and a conductive trace extending from the first contact pad to the second contact pad;

a second conductive layer formed over a second surface of the base substrate opposite the first surface including a third contact pad of the second conductive layer directly opposite the second contact pad of the first conductive layer, wherein portions of the base substrate ~~are electrically isolated to~~ form conductive base leads between the first conductive layer and second conductive layer; ~~and~~

a first semiconductor die disposed over the first conductive layer and within a vertical extent of the base substrate, wherein a first conductive bump of the first

semiconductor die is bonded to the first contact pad of the first conductive layer; and

a second semiconductor die mounted to the first conductive layer and including a second conductive bump of the second semiconductor die bonded to the first contact pad of the first conductive layer directly opposite the first conductive bump of the first semiconductor die.

~~8~~6. The semiconductor device of claim ~~7~~5, further including an encapsulant deposited ~~over~~ in contact with the second ~~the first~~ semiconductor die and first conductive layer.

~~9. The semiconductor device of claim 7, further including a second semiconductor die disposed over the first conductive layer between the base leads.~~

~~10. The semiconductor device of claim 9, wherein the first semiconductor die and second semiconductor die are electrically coupled to opposite sides of a portion of the first conductive layer.~~

~~11~~7. The semiconductor device of claim ~~9~~5, wherein a height of the conductive base leads is greater than a thickness of the ~~second~~ first semiconductor die.

~~12~~8. The semiconductor device of claim ~~7~~6, further including a third semiconductor die disposed over the ~~first~~ second semiconductor die outside the encapsulant.

~~13~~9. The semiconductor device of claim ~~7~~8, further including a plurality of conductive vias formed through the ~~first~~ second semiconductor die and electrically connected to the third semiconductor die.

1~~4~~0. A semiconductor device, comprising:

a plurality of ~~electrically~~ isolated conductive base leads formed ~~from~~ as portions of a common base substrate;

a first conductive layer formed over a first surface of the conductive base leads, the first conductive layer including a first contact pad;

~~a second conductive layer formed over a second surface of the base leads opposite the first surface; and~~

a first semiconductor die ~~disposed over the first conductive layer~~ including a first conductive bump bonded to the first contact pad; and

a second semiconductor die including a second conductive bump bonded to the first contact pad directly opposite the first conductive bump.

151. The semiconductor device of claim 140, further including an encapsulant deposited over the first semiconductor die.

~~16. The semiconductor device of claim 14, further including a second semiconductor die disposed over the first conductive layer between the base leads.~~

~~17. The semiconductor device of claim 16, wherein the first semiconductor die and second semiconductor die are electrically coupled to opposite sides of a portion of the first conductive layer.~~

1~~8~~2. The semiconductor device of claim 1~~6~~0, wherein a height of the conductive base leads is greater than a thickness of the second semiconductor die and the second semiconductor die is located completely within the height of the conductive base leads.

1~~9~~3. The semiconductor device of claim 1~~4~~0, ~~wherein the~~ further including a second ~~first~~ conductive layer comprising ~~and second conductive layer include~~ an etch-resistant material formed as a plurality of second contact pads over the conductive base leads opposite the first conductive layer.

~~20~~14. A semiconductor device, comprising:

a plurality of ~~electrically~~ isolated conductive base leads formed as portions of ~~from~~ a common base substrate; ~~and~~

~~a first etch resistant conductive layer formed over a first surface of the base leads~~

a first conductive layer formed directly on a first surface of the conductive base leads;

a first semiconductor die mounted to the first conductive layer opposite the conductive base leads;

a chip carrier substrate, wherein the first semiconductor die is mounted to the chip carrier substrate by the conductive base leads; and

a second semiconductor die mounted to the chip carrier substrate between the conductive base leads and including a conductive bump of the second semiconductor die extending from a first contact pad of the chip carrier substrate to a second contact pad of the second semiconductor die.

~~21. The semiconductor device of claim 20, further including a second etch resistant conductive layer formed over a second surface of the base leads opposite the first surface.~~

~~22. The semiconductor device of claim 20, further including a first semiconductor die disposed over the first etch-resistant conductive layer.~~

~~23. The semiconductor device of claim 22, further including a second semiconductor die disposed over the first etch-resistant conductive layer between the base leads.~~

~~24. The semiconductor device of claim 23, wherein the first semiconductor die and second semiconductor die are electrically coupled to opposite sides of a portion of the first etch-resistant conductive layer.~~

~~2~~15. The semiconductor device of claim ~~23~~14, wherein a height of the conductive base leads is greater than a thickness of the second semiconductor die.

16. The semiconductor device of claim 14, further including an adhesive layer between the second semiconductor die and first conductive layer.

17. The semiconductor device of claim 14, further including an encapsulant deposited over the first semiconductor die and first surface of the conductive base leads.

18. The semiconductor device of claim 14, further including a bump formed between the first conductive layer and first semiconductor die.

19. The semiconductor device of claim 14, further including a second conductive layer comprising an etch-resistant material formed over the conductive base leads opposite the first conductive layer.

20. The semiconductor device of claim 19, wherein the second conductive layer contacts a third contact pad of the chip carrier substrate.

21. The semiconductor device of claim 1, wherein the first base lead includes a footprint of the first base lead coextensive with a footprint of the second contact pad and a footprint of the third contact pad.

22. The semiconductor device of claim 1, further including a chip carrier substrate, wherein a fourth contact pad of the chip carrier substrate contacts the third contact pad.

23. The semiconductor device of claim 1, wherein a first width of the conductive trace is less than a second width of the first contact pad and less than a third width of the second contact pad.

24. The semiconductor device of claim 5, wherein the second conductive layer includes an etch-resistant material.

25. The semiconductor device of claim 5, wherein the third contact pad includes a footprint of the third contact pad coextensive with a footprint of one of the conductive base leads.