implemented for non-cascode configured amplifiers. It will also be understood that in some embodiments, one or more features of the present disclosure can also be implemented utilizing other types of transistors, including bipolar-junction transistors (BJTs).

[0053] For example, Figure 4B shows amplifier circuit 100 having a similar architecture as the amplifier circuit 100 of Figure 4A, but where a cascode amplifier 102 includes first and second BJTs Q1, Q2. More particularly, the first transistor Q1 can be implemented as a common emitter stage where an input signal (RF_in) is provided to a base of Q1, and an amplified signal is output through a collector of Q1, with an emitter of Q1 being coupled to ground. The second transistor Q2 can be implemented as a common base stage where the amplified signal from Q1 is provided to an emitter of Q2, and a further amplified signal is output through a collector of Q2, with a base of Q2 being provided with a base voltage VB.

[0054] In the example of Figure 4B, the amplifier circuit 100 can further include a bias circuit 110 configured to provide, for example, a bias signal to the base of Q1. Accordingly, such a bias circuit can be coupled to the input path that routes the input signal RF_in. In the example of Figure 4B, the amplifier 102 is shown to be provided with a supply voltage VCC to the collector of the second transistor Q2.

[0055] Figure 5 shows an amplifier circuit 100 that can be a more specific example of the amplifier circuit of Figure 4A. In the example of Figure 5, an amplifier 102 is shown to include a cascode arrangement of first and second transistors Q1, Q2, similar to the example of Figure 4A. An input signal (RF_in) is shown to be provided to a gate of Q1 through a DC-block capacitance C2, and an amplified signal is shown to be provided as an output (RF_out) through a drain of Q2 and a DC-block capacitance C3.

[0056] In the example of Figure 5, an inter-transistor switch SW3 is shown to be provided between Q1 and Q2. More particularly, a drain of Q1 is shown to be coupled to a source of Q2 through the inter-transistor switch SW3. Examples related to operation of such a switch are described herein in greater detail.

[0057] In the example of Figure 5, a bias circuit is generally indicated as 110, and is shown to include a current mirror where a reference current IREF can be replicated through a mirror arrangement of a transistor M1 on the IREF side

configured for a protection mode upon detection of a high power condition at the input of the amplifier 102.

[0066] Referring to the normal operating mode of Figure 6A, an RF signal is shown to be provided to Q1 as an input; Q1 is shown to provide a partially amplified signal to Q2; and Q2 is shown to provide an amplified signal as an output of the amplifier 102. In Figure 6A, a path taken by the input signal (RF_in) to become the output signal (RF_out) is depicted as 122. To support such an amplification operation, the bias circuit 110 is shown to provide a bias signal to Q1, as depicted by arrow 120.

[0067] More particularly, it is noted that in the normal operating mode of Figure 6A, each of the switches SW1 and SW2 of the bias circuit 110 can be closed to allow operation of the current mirror involving the transistors M1 and M2. Each of the switches SW4 and SW5 can be opened to allow the resulting bias signal to be delivered to Q1 through the bias resistance R2. With respect to the signal path 122 of Figure 6A, the shunt switch SW6 can be opened to allow the input signal to be delivered to Q1, and the inter-transistor switch SW3 can be closed to allow the partially amplified signal to be delivered to Q2 from Q1.

[0068] Referring to the protection mode of Figure 6B, an RF signal present at the input path can include, for example, a high power signal being transmitted from a nearby device. Accordingly, such an RF signal is shown to be shunted to ground through the shunt path, as indicated by arrow 126. Further, operation of the bias circuit 110 can be disabled, such that a bias signal is not delivered to Q1.

[0069] More particularly, it is noted that in the protection mode of Figure 6B, each of the switches SW1 and SW2 of the bias circuit 110 can be opened to disable operation of the current mirror involving the transistors M1 and M2. Each of the switches SW4 and SW5 can be closed to allow shunting of any current to ground through the switch SW5. For example, arrow 124 depicts a shunt path that can allow a current from Q1 to be shunted to ground through the bypass switch SW4. With respect to the input signal path, the shunt switch SW6 can be closed to allow the RF signal (having high power) to be shunted to ground through the shunt switch S6. Since there is no inline switch along the input path to Q1, Q1 can be subjected to at least some of the RF signal; and at least some of the current associated with such RF signal at Q1 can be further shunted to

ground through the foregoing bypass switch SW4 and the shunt switch SW5. Since the inter-transistor switch SW3 is now open, Q2 can be substantially isolated from Q1 (and thereby the RF signal present at Q1). The open state of Q2 also disables the amplifier current associated with the supply voltage (VDD).

[0070] Referring to Figures 6A and 6B, the foregoing normal operating mode and the protection mode can be controlled by the switch control logic circuit 108 providing appropriate switch control signals. For example, a given switch control signal can be a low signal or a low bit 0 to open the corresponding switch, or a high signal or a high bit 1 to close the corresponding switch. Table 1 lists combinations of switch states corresponding to the respective modes of Figures 6A and 6B.

Table 1

Mode	SW1	SW2	SW3	SW4	SW5	SW6
Normal	Closed	Closed	Closed	Open	Open	Open
Protection	Open	Open	Open	Closed	Closed	Closed

[0071] As described herein, a comparator such as the Schmitt trigger of Figure 5 can be configured so that the protection mode is triggered for the amplifier circuit 100 when the detected peak voltage VDET exceeds a first threshold voltage Vlh (e.g., when VDET > Vlh), and the amplifier circuit 100 reverts back to the normal operating mode when VDET falls below a second threshold voltage Vhl (e.g., when VDET < Vhl). In some embodiments, the first threshold voltage Vlh can be greater than the second threshold voltage Vhl so as to, for example, prevent a chattering effect where the amplifier circuit 100 is too sensitive to transitions between the normal operating mode and the protection mode.

[0072] More particularly, suppose that the first and second threshold values are approximately the same, such that Vlh ≈ Vhl. In such a configuration, the amplifier circuit 100 can transition from normal mode to protection mode once the detected peak voltage VDET exceed Vlh (≈ Vhl). After such a transition, there may be fluctuations in VDET about the common value of Vlh and Vhl. In

WHAT IS CLAIMED IS:

1. An amplifier circuit comprising:

an input node and an output node;

an amplifier implemented between the input node and the output node, wherein the amplifier includes a cascode arrangement of a first transistor and a second transistor, the first transistor having an input coupled to the input node, the second transistor coupled to the first transistor and having an output coupled to the output node;

a bias circuit configured to provide a bias signal to the amplifier;

a protection circuit configured to generate a detected voltage representative of a peak of a radio-frequency signal present at the input node, the protection circuit further configured to enable a protection mode when the detected voltage is greater than a first threshold value and to disable the protection mode when the detected voltage is less than a second threshold value that is less than the first threshold value; and

an assembly switches configured to implement the enablement and disablement of the protection mode,

wherein the assembly of switches includes a shunt switch configured to allow switchable shunting of the radio frequency signal from the input node to ground.

2. The amplifier circuit of claim 1 wherein the input node is configured to be coupled to an antenna.

3. The amplifier circuit of claim 2 wherein the amplifier is a low-noise amplifier configured to support a receive operation.

4. The amplifier circuit of claim 1 wherein each of the first and second transistors is a field-effect transistor having a gate, a drain and a source.

5. The amplifier circuit of claim 4 wherein the first transistor is implemented as a common source device, and the second transistor is implemented as a common gate device, such that the gate of the first transistor is coupled to the input node, the drain of the first transistor is coupled to the source of the second transistor, and the drain of the second transistor is coupled to the output node.

6. The amplifier circuit of claim 5 wherein the source of the first transistor is coupled to ground, and the gate of the second transistor is coupled to a node having a gate potential.

7. The amplifier circuit of claim 1 wherein the shunt switch is configured to be open when the protection circuit disables the protection mode, and to be closed when the protection circuit enables the protection mode.

8. The amplifier circuit of claim 1 wherein the assembly of switches includes an inter-transistor switch configured to provide a switchable coupling of the first and second transistors.

9. The amplifier circuit of claim 8 wherein the inter-transistor switch is configured to be closed when the protection circuit disables the protection mode to allow a partially amplified signal from the first transistor to be provided as an input for the second transistor, and to be open when the protection circuit enables the protection mode to disconnect the second transistor from the first transistor.

10. The amplifier circuit of claim 1 wherein the bias circuit is configured to provide the bias signal to the input of the first transistor through a bias resistance, the bias circuit including a current mirror, such that the bias signal is representative of an output of the current mirror.

11. The amplifier circuit of claim 10 wherein the assembly of switches includes one or more switches implemented in the current mirror, the one or more

switches of the current mirror configured to enable operation of the current mirror when the protection circuit disables the protection mode, and to disable operation of the current mirror when the protection circuit enables the protection mode.

12. The amplifier circuit of claim 10 wherein the assembly of switches includes a bias shunt switch implemented between ground and a node between the current mirror and the bias resistance, the bias shunt switch configured to be open when the protection circuit disables the protection mode, and to be closed when the protection circuit enables the protection mode.

13. The amplifier circuit of claim 10 wherein the assembly of switches includes a bypass switch implemented to be electrically parallel with the bias resistance, the bypass switch configured to be open when the protection circuit disables the protection mode, and to be closed when the protection circuit enables the protection mode.

14. The amplifier circuit of claim 1 wherein the protection circuit includes a detector coupled to the input node to allow sampling of the radio-frequency signal, the detector configured to generate the detected voltage based on the peak of the sampled radio-frequency signal.

15. The amplifier circuit of claim 14 wherein the detector includes a diode configured to limit a current associated with the sampled radio-frequency signal in one direction, and a resistance-capacitance circuit configured to generate the detected voltage, the resistance-capacitance circuit including a parallel arrangement of a resistance and a capacitance between an output of the diode and ground.

16. The amplifier circuit of claim 14 wherein the detector includes a comparator configured to generate an enable output to enable the protection mode when the detected voltage is greater than the first threshold value, and to generate a disable output to disable the protection mode when the detected voltage is less than the second threshold value.

17. The amplifier circuit of claim 16 wherein the comparator includes a Schmitt trigger.

18. The amplifier circuit of claim 16 wherein the protection circuit further includes a control logic circuit configured to generate a first set of control signals to enable the protection mode based on the enable output of the comparator, and to generate a second set of control signals to disable the protection mode based on the disable output of the comparator.

19. The amplifier circuit of claim 18 wherein each of the first and second sets of control signals includes switch control signals.

20. The amplifier circuit of claim 1 further including an electrostatic discharge circuit coupled to the input node and configured to provide a discharge path to ground when a voltage at the input node is greater than a discharge threshold value.

21. The amplifier circuit of claim 20 wherein the electrostatic discharge circuit includes a plurality of diodes each configured as multi-stack device having a reduced size to meet lower electrostatic discharge protection requirement, to thereby provide a reduced parasitic capacitance.

22. A die comprising:

a semiconductor substrate; and

an amplifier circuit implemented on the semiconductor substrate, the amplifier circuit including an input node and an output node, and an amplifier implemented between the input node and the output node wherein the amplifier includes a cascode arrangement of a first transistor and a second transistor, the first transistor having an input coupled to the input node, the second transistor coupled to the first transistor and having an output coupled to the output node, the amplifier circuit further including a bias circuit configured to provide a bias signal to the amplifier, the amplifier circuit further including a protection circuit configured to generate a detected voltage representative of a peak of a radio-frequency signal present at the

input node, the protection circuit further configured to enable a protection mode when the detected voltage is greater than a first threshold value and to disable the protection mode when the detected voltage is less than a second threshold value that is less than the first threshold value, the amplifier circuit further including an assembly switches configured to implement the enablement and disablement of the protection mode, wherein the assembly of switches includes a shunt switch configured to allow switchable shunting of the radio frequency signal from the input node to ground.

23. A packaged module comprising:

a packaging substrate configured to receive a plurality of components; and

an amplifier circuit implemented on the packaging substrate, the amplifier circuit including an input node and an output node, and an amplifier implemented between the input node and the output node, wherein the amplifier includes a cascode arrangement of a first transistor and a second transistor, the first transistor having an input coupled to the input node, the second transistor coupled to the first transistor and having an output coupled to the output node, the amplifier circuit further including a bias circuit configured to provide a bias signal to the amplifier, the amplifier circuit further including a protection circuit configured to generate a detected voltage representative of a peak of a radio-frequency signal present at the input node, the protection circuit further configured to enable a protection mode when the detected voltage is greater than a first threshold value and to disable the protection mode when the detected voltage is less than a second threshold value that is less than the first threshold value, the amplifier circuit further including an assembly switches configured to implement the enablement and disablement of the protection mode, wherein the assembly of switches includes a shunt switch configured to allow switchable shunting of the radio frequency signal from the input node to ground.

24. The packaged module of claim 23 wherein substantially all of the amplifier circuit is implemented on a semiconductor die that is mounted on the packaging substrate.

25. The packaged module of claim 23 wherein the amplifier circuit is configured to support a receive operation.

26. The packaged module of claim 25 wherein the packaged module is a receive module.

27. The packaged module of claim 26 wherein the receive module is a diversity receive module.

28. A wireless device comprising:

an antenna;

a transceiver; and

an amplifier circuit implemented between the antenna and the transceiver, the amplifier circuit including an input node and an output node, and an amplifier implemented between the input node and the output node, wherein the amplifier includes a cascode arrangement of a first transistor and a second transistor, the first transistor having an input coupled to the input node, the second transistor coupled to the first transistor and having an output coupled to the output node, the amplifier circuit further including a bias circuit configured to provide a bias signal to the amplifier, the amplifier circuit further including a protection circuit configured to generate a detected voltage representative of a peak of a radio-frequency signal present at the input node, the protection circuit further configured to enable a protection mode when the detected voltage is greater than a first threshold value and to disable the protection mode when the detected voltage is less than a second threshold value that is less than the first threshold value, the amplifier circuit further including an assembly switches configured to implement the enablement and disablement of the protection mode, wherein the assembly of switches includes a shunt switch configured to allow

switchable shunting of the radio frequency signal from the input node to ground.

29. The wireless device of claim 28 wherein the input node of the amplifier circuit is coupled to the antenna, and the output node of the amplifier circuit is coupled to the transceiver.

30. The wireless device of claim 29 wherein the wireless device is a cellular phone configured to operate in one or more cellular bands.