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(54) IMPROVEMENTS IN OR RELATING TO ELECTRONIC CALCULATORS

(71) We, HEWLETT-PACKARD COMPANY, 1501 Page Mill Road, Palo Alto, California, United States of America, a corporation organized and existing under the laws of the State of California, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention is concerned with improvements in or relating to electronic calculators.

Calculators using delay line memories and serial data processing are well known in the art. Prior art calculators usually had a limited number of data manipulating keys and often a number of key strokes was necessary to achieve a desired manipulation. For example, in prior art calculators the duplication of an entry required either re-entry of the number actuation of a separate repeat key after an enter key. Changing the sign of an entry often required a multistep operation involving subtraction of the entry from zero. Storing a number usually removed it from the stack memory and re-entry or recall of the number was therefore necessary if one wanted to use the stored number immediately.

It is an object of the present invention to provide an improved electronic calculator.

The present invention provides an electronic calculator including a stack memory for storing a stack of data words; shifting means for pushing the words in the stack up and down; digit keys for inputting data into the top word position in the stack; an enter key; and control means connected to the enter key and the shifting means for pushing down the stack and leaving the word in the top of the stack unchanged in response to actuation of the enter key.

Preferably a calculator as set forth in the last preceding paragraph also comprises clearing means connected to the stack memory and the digit keys for clearing the top word of the stack memory in response to the actuation of a digit key subsequent to the actuation of the enter key.

A calculator as set forth in the last preceding paragraph but one may also comprise function keys and function means connected to the stack memory and the function keys for combining the word in the top of the stack with the word in the next memory position, for entering the result of the combination into the top of the stack and for pushing up the rest of the words in the stack in response to the actuation of a function key subsequent to the actuation of the enter key.

A calculator as set forth in the last preceding paragraph but one may also comprise function keys and function means connected to the stack memory and the function keys for combining the word in the top of the stack with the word in the next memory position, for entering the result of the combination into said next memory position and for pushing up the words in the stack in response to the actuation of a function key subsequent to the actuation of the enter key.

A calculator as set forth in the preceding paragraph or the last preceding paragraph but one preferably also comprises logic means connected to the shifting means and the function means for pushing the stack down in response to the actuation of a data key subsequent to the actuation of a function key.

In an electronic calculator as set forth in any one of the last five immediately preceding paragraphs, each word may include information representing the algebraic sign of the word comprising at least one bit; and the calculator preferably further comprises a change sign key; complementing means connected to the stack memory for complementing the sign information in the word in the top of the stack in response to actuation of the change sign key; and control means connected to the complementing means and the digit keys for recomplementing the sign information in the word shifted from the top of the stack to the next memory position in response to the actuation of a data key after the actuation of the change sign key and for complementing the sign information in the

word containing data inputted into the stack memory in response to said actuation of a data key.

Preferably a calculator as set forth in the last preceding paragraph comprises function keys and logic means connected to the function keys and the control means for presetting the control means to respond to the actuation of a data key after the actuation of the change sign key.

An electronic calculator as set forth in any one of the last seven immediately preceding paragraphs may further comprise an auxiliary memory; a store key; and control means connected to the store key, the stack memory and the auxiliary memory for duplicating the word in the top of the stack into the auxiliary memory, leaving the word in the top of the stack unchanged, in response to actuation of the store key.

Preferably a calculator as set forth in the last preceding paragraph comprises clearing means connected to the stack memory and the digit keys for clearing the top of the stack word in response to the actuation of a digit key subsequent to the actuation of the store key.

A calculator as set forth in the last preceding paragraph may comprise function keys and function means connected to the stack memory and the function keys for combining the word in the top of the stack with the word in the next memory position, for entering the result of the combination into the top of the stack and for pushing up the rest of the words in the stack in response to the actuation of a function key subsequent to the actuation of the store key.

A calculator as set forth in the last preceding paragraph but one may comprise function keys and function means connected to the stack memory and the function keys for combining the word in the top of the stack with the word in the next memory position, for entering the result of the combination into said next memory position and for pushing up the words in the stack in response to the actuation of a function key subsequent to the actuation of the enter key.

A calculator as set forth in the last preceding paragraph or the last preceding paragraph but one preferably also comprises logic means connected to the shifting means and the function means for pushing the stack down in response to the actuation of a data key subsequent to the actuation of a function key.

In the present invention, the actuation of the enter key pushes down the stack so that the keyboard register and first memory register contain the same data. Thus, a repeat key is not necessary. If data keys are actuated after the enter key is actuated, the first data key will cause the keyboard register to be cleared before the new data is stored therein.

A change sign (CHS) key is provided to permit changing the sign of the data in the keyboard register without performing a subtract operation. When the CHS key is actuated, the sign digit of the data in the keyboard register is complemented. If the CHS key is actuated after a function is performed and a data key is actuated after CHS, the original sign will be restored to the data in the keyboard register as the stack is pushed down. The sign will then be changed, made negative in this case, on the new data entered from the digit keys. The CHS key may also be actuated after data has been entered from the digit keys to change the sign of that entry. The store key in the present invention causes replication of information in the keyboard register into the auxiliary memory without destroying the information in the keyboard register. If a digit key is actuated after a store operation, the keyboard register will be cleared before the digit is entered into it.

There now follows a detailed description which is to be read with reference to the accompanying drawings of an electronic calculator according to the invention; it is to be clearly understood that this calculator has been selected for description to illustrate the invention by way of example and not by way of limitation.

In the accompanying drawings:—

Figure 1 shows a basic logic circuit of a calculator according to the present invention;

Figure 2 shows the keyboard encoder logic circuit thereof;

Figure 3 shows the keyboard interlock logic circuit thereof;

Figure 4 shows the control flip flops therefor; and

Figure 5 shows the timing logic circuit.

Figure 1 shows a block diagram of the logic circuitry of a calculator according to the present invention. A shift register type stack memory 61 having four storage registers or locations is used for primary information storage. The four storage registers are designated KB, M1, M2, and M3, where KB is the top stack register into which key-board information is entered. The information in the register KB is also the information that is usually displayed to a calculator user. Since the stored data is constantly being circulated around a loop connecting the output 162 of the memory 61 with the input 163, four word times are defined to correspond to the presence of the words in the registers KB, M1, M2 and M3 at a given point in the data loop. The memory positions shown in Figure 1 correspond to a word time W1; for each subsequent word time the memory positions are shifted to the right, and the right-most location becomes the left-most one. When no operations are being performed on the calculator, the normal data path is from the output

162 through an AND gate 62 and a line 160 to the input 163. A second input to the AND gate 62 is OR-tied to AND gates 63 and 64 which are alternatively high during each cycle time in the absence of any operations initiated from the keyboard. Two other storage registers M4 and M5 are provided to facilitate data manipulation. The register M5 is one word long and is used to delay the stack information for shifting the stack down. The register M4 is also one word long and is used for auxiliary data storage. In the following paragraphs the basic calculator operations will be described using signals from the circuits shown in Figures 2, 3, 4 and 5 which will subsequently be described.

A first digit from the keyboard is entered in the following manner. An input F7 to an AND gate 67 determines whether the data in the register KB may be cleared for a new entry or whether the stack must be first pushed down. If the data may be cleared, the input F7 will be low; if not the input F7 would be high and the stack would be pushed down with the entry of a first digit from the keyboard. An input F5 to an AND gate 69 tells whether a data entry is a first digit or not. If the entry is a first digit, the input F5 will be high and the data in the register KB will be cleared because the gate 69 will cause the AND gate 62 to close during W1 and thus prevent the data in the register KB from continuing on the line 160. The digit information coming from the keyboard on the keylines is placed on the line 160 through an AND gate 74. An AND gate 73 enables the gate 74 at the appropriate time in response to digit position timing signals from the timing logic circuit shown in Figure 5. Successive digits are similarly entered via the gates 73 and 74 since the first digit has already been entered, the inputs F5 and F7 will be low, allowing the memory information to circulate normally around the loop.

Once data has been entered into the register KB, the stack can be pushed down in response to an enter signal ENT', to permit further data entries. The signal ENT' opens an AND gate 89 via an OR gate 77 and an AND gate 189 during W1, W2 and W3 to allow KB, M1 and M2 to pass through the one-word length delay memory register M5. Also during W1, KB passes through the gate 62 which is held open by a signal from the AND gate 64. During W2, W3 and W4, the gate 62 is closed by the AND gate 63, thus prohibiting M1, M2 and M3 from getting through. The result of this operation is to duplicate the contents of the register KB into the register M1 and move the contents of the registers M1 and M2 to the registers M2 and M3 respectively. The contents of the register M3 are lost in the process of pushing down the stack.

In this embodiment each memory word is 16 digit positions long, with the first digit position giving the algebraic sign of the numerical information contained in the remaining 15 digit positions. The first digit position of a memory register normally contains a zero, representing a positive sign, and that digit is complemented if the numerical information is to have a negative sign. A signal F8 indicates that a change sign, signal CHS', has been received from the keyboard and that the sign digit has been complemented. The complementing is effected by an inverter 82 when an AND gate 78 is opened in response to the CHS' signal and the change sign digit position signal d_s and W1 in an AND gate 98. When the complementing is being effected, the normal data path is closed by the gate 62 in response to the AND gates 64, 72 and 80 and an inverter 79. The sign digit may be changed at any time during numerical digit entry, as well as before and after, and may also be changed back and forth between positive and negative.

The results of any arithmetic or information handling operation are put in the register KB and a signal CHS' will change the sign of those results as described above. If the next signal is a digit the signals F5 and F7 will be high, indicating that the stack must be pushed down to make way for a first digit. The signal F8 will also be high because of the signal CHS' and the first digit of KB will pass through the inverter 82 to the memory M5 via an AND gate 81, the rest of KB as well as M1 and M2 passing through the AND gate 89 to the register M5, which effects the push down of the stack by delaying the data in each memory position by one word-time to make room for new information in the register KB. During the time KB is passing through the register M5, the gate 62 is closed to break the normal data path. The result of this operation is to change the sign of the result stored in the register KB back to its original value before pushing down the stack and to make the sign of the new information negative. In this process the gate 81 responds to the signals F7, F8, W1 and the sign digit position signal through the AND gate 68. Likewise, the gate 89 responds to the signals F7, F8 and the complement of the sign digit position signal through OR gates 167, 76 and 77 and AND gates 168, 67 and 189.

Information can be stored in the auxiliary memory M4 that has its own data loop 260. When a store signal STO' is received by an AND gate 86, an AND gate 85 is opened during W1 to allow KB information to enter the register M5. At the same time an AND gate 87 is closed, thus clearing the previously stored information. The normal data loop is not disturbed during this operation. The stored information can be recalled by a recall signal RCL' which opens an AND gate 75 during W1 and closes the gate 62, thus put-

ting the information in the KB position. During the same time the gate 89 is opened to pass KB, M1 and M2 through the register M5 in order to push down the stack. To accomplish that operation the gate 89 responds to the recall signal RCL' through the gate 76 and the signal F7 through the gate 67 as well as the gate 189; and the gate responds to the recall signal RCL' through an inverter 179 and gates 71 and 64.

The contents of the register KB and M1 will be added together in an ADDER 90 in response to an add signal, ADD', from the key-board. In order to make the register M1 available simultaneously with the register KB, a one word time early tap 164 is provided on the memory 61. During W1, the gate 62 is closed and an AND gate 92 is opened to pass KB into the ADDER 90. At the same time an AND gate 94 is opened by an AND gate 96 to pass M1 into the ADDER 90, where the contents of the registers KB and M1 are combined and put on the line 160. During W2 and W3 the gate 92 is closed, but the gate 94 is left open, pushing up the contents of the register M3 and M2 to the registers M2 and M1 respectively. During W4 the gate 94 is closed and the gate 62 is reopened, leaving the contents of the register M3 unchanged so that the registers M3 and M2 then contain the same data. Alternatively, one could connect the ADDER to the output 162 and to the register M5, which would put the result of the addition in the register M1, and then on the next cycle the stack could be pushed up.

These operations are performed in response to various signals generated in response to the actuation of keys on the keyboard, the encoding logic circuitry of which is shown in Figure 2. The keyboard 8 is a collection of momentary SPST switches connected to a voltage source V+ and each key actuation gives a logically high signal on the key output line. Each digit key is connected to an OR gate 10 as well as to decoding circuitry comprising OR gates 22, 23, 24 and 25 which encode the numbers in BCD (Binary Coded Decimal). The function keys are all connected to an OR gate 12. Gates 10 and 12 are in turn connected to an OR gate 13 which provides a keydown signal.

Figure 3 illustrates the keyboard interlock logic circuit which includes four flip flops 14, 15, 16 and 17 that are connected as an interlock to give a keydown signal KDN during just one calculator cycle comprising 4 word times. The interlock operation can be simply illustrated by first assuming that the Q output of each flip flop is low when an input keydown signal occurs. The flip flops 14 and 15 are connected as a master and slave so that during W4 the flip flop 14 is set, making Q14 high, and during W1 that signal is transferred to the flip flop 15. Since Q15 and $\overline{Q17}$ are both high they cause an AND gate 26 to be high, giving the KDN signal starting with the first W1 after a key is actuated. The flip flops 16 and 17 are also a master-slave pair so that during W4 the flip flop 16 is set, and the Q16 signal is transferred to the flip flop 17 during W1, making $\overline{Q17}$ low and thus terminating the signal KDN. When the key is released, the keydown signal is removed and the interlock is reset via AND gates 214 and 215. No matter how long a key is depressed, the signal KDN will remain on for only four word times, starting with W1.

The signal KDN is used to produce several synchronous signals indicating that a certain key or one of a class of keys has been actuated. In Figure 2 the signal KDN is AND'ed with the output of the gate 10 in an AND gate 11 to produce a signal DIG' which indicates that a digit key has been actuated. The signal DIG' is used to signal the circuitry in Figure 1 to enter a digit into the register KB. The signal KDN is also AND'ed with each of the function keys "add" (ADD), "enter" (ENT), "recall" (RCL), "store" (STO) and "change sign" (CHS) in AND gates 118, 18, 19, 20 and 21 respectively to produce signals ADD', ENT', RCL', STO' and CHS' also used in connection with the circuits in Figure 1 and Figure 4.

Several control flip flops are shown in Figure 4. Stack control flip flops 206 and 207 are arranged as a master-slave stack control flip flop. As will be recalled from the discussion of Figure 1, the stack must be pushed down when a data entry occurs after a recall or an add operation, so the outputs RCL' and ADD' are connected to the set input of the flip flop 206. After the RCL or ADD key is released, the signal F6 is transferred to the flip flop 207 to make the signal F7 high. Similarly the outputs DIG', STO' and ENT' are connected to the reset input of the flip flop 206 through an OR gate 153 since they do not call for lowering the stack. After the STO, ENT or a digit key is released, the signal $\overline{F7}$ is therefore high. Flip flops 204 and 205 are connected as a master-slave pair to indicate a first digit entry. The outputs ADD', RCL', STO' and ENT' all set the flip flop 204 to make the signal F5 high after the respective key is released. The input DIG' resets the flip flop 204 and causes the signal F5 to be high after the digit key is released. A flip flop 208 is the change sign flip flop which is set to make the signal F8 high whenever the input CHS' occurs and reset whenever the outputs RC', STO', ADD' or ENT' occur.

Figure 5 shows the timing logic circuit that produces the word time signals and the

digit position signals. A master clock 31 provides all of the basic timing signals for the circuitry in Figures 1 and 3. The clock signal is divided down by a string of dividers 132, 133, 134, 135 and 136. Each clock pulse corresponds to a digit and the last two divider outputs are decoded in a decoder 137 to produce the word time signals. An OR gate 32 is used to decode the first digit position d_s which corresponds to the sign digit. Flip flops 33, 34, 35 and 36 provide a digit position counter which keeps track of how many digits have been entered in the register KB. The counter indexes one digit for each signal DIG′ and is reset by signals ADD′, ENT′, RCL′ or STO′. AND gates 37, 38, 39 and 40 connected to an AND gate 41 test for coincidence between the timing signal from the clock and divider chain and the position count from the digit position counter. The DIGIT POSITION signal tells the circuitry of Figure 1 when to insert a digit code from the key lines onto the line 160.

Although the structure and operation of the calculator have been described in terms of flip flops and gates, it will be appreciated by one skilled in the art that the calculator could also be implemented using other types of circuit elements such as read only memories. Thus the logical equations embodied herein in gates and flip flops would be realized in connections between sense and readout lines of a read only memory. It will also be appreciated that other arithmetic operations besides add could be used in the calculator—add was simply shown as illustrative of the interaction between arithmetic functions and data handling functions.

WHAT WE CLAIM IS:—

1. An electronic calculator including a stack memory for storing a stack of data words; shifting means for pushing the words in the stack up and down; digit keys for inputting data into the top word position in the stack; an enter key; and control means connected to the enter key and the shifting means for pushing down the stack and leaving the word in the top of the stack unchanged in response to actuation of the enter key.

2. An electronic calculator according to claim 1 and comprising clearing means connected to the stack memory and the digit keys for clearing the top word of the stack memory in response to the actuation of a digit key subsequent to the actuation of the enter key.

3. An electronic calculator according to claim 2 and comprising function keys and function means connected to the stack memory and the function keys for combining the word in the top of the stack with the word in the next memory position, for entering the result of the combination into the top of the stack and for pushing up the rest of the words in the stack in response to the actuation of a function key subsequent to the actuation of the enter key.

4. An electronic calculator according to claim 2 and comprising function keys and function means connected to the stack memory and the function keys for combining the word in the top of the stack with the word in the next memory position, for entering the result of the combination into said next memory position and for pushing up the words in the stack in response to the actuation of a function key subsequent to the actuation of the enter key.

5. An electronic calculator according to any one of claims 3 and 4 and comprising logic means connected to the shifting means and the function means for pushing the stack down in response to the actuation of a data key subsequent to the actuation of a function key.

6. An electronic calculator according to any one of the preceding claims wherein each word includes information representing the algebraic sign of the word comprising at least one bit; and the calculator further comprises a change sign key; complementing means connected to the stack memory for complementing the sign information in the word in the top of the stack in response to actuation of the change sign key; and control means connected to the complementing means and the digit keys for recomplementing the sign information in the word shifted from the top of the stack to the next memory position in response to the actuation of a data key after the actuation of the change key and for complementing the sign information in the word containing data inputted into the stack memory in response to said actuation of a data key.

7. An electronic calculator according to claim 6 and comprising function keys and logic means connected to the function keys and the control means for presetting the control means to respond to the actuation of a data key after the actuation of the change sign key.

8. An electronic calculator according to any one of the preceding claims wherein the calculator further comprises an auxiliary memory; a store key; and control means connected to the store key, the stack memory and the auxiliary memory for duplicating the word in the top of the stack into the auxiliary memory, leaving the word in the top of the stack unchanged, in response to actuation of the store key.

9. An electronic calculator according to claim 8 and comprising clearing means connected to the stack memory and the digit keys for clearing the top word of the stack memory in response to the actuation of a digit key subsequent to the actuation of the store key.

10. An electronic calculator according to

digit position signals. A master clock 31 provides all of the basic timing signals for the circuitry in Figures 1 and 3. The clock signal is divided down by a string of dividers 132, 133, 134, 135 and 136. Each clock pulse corresponds to a digit and the last two divider outputs are decoded in a decoder 137 to produce the word time signals. An OR gate 32 is used to decode the first digit position d_s which corresponds to the sign digit. Flip flops 33, 34, 35 and 36 provide a digit position counter which keeps track of how many digits have been entered in the register KB. The counter indexes one digit for each signal DIG′ and is reset by signals ADD′, ENT′, RCL′ or STO′. AND gates 37, 38, 39 and 40 connected to an AND gate 41 test for coincidence between the timing signal from the clock and divider chain and the position count from the digit position counter. The DIGIT POSITION signal tells the circuitry of Figure 1 when to insert a digit code from the key lines onto the line 160.

Although the structure and operation of the calculator have been described in terms of flip flops and gates, it will be appreciated by one skilled in the art that the calculator could also be implemented using other types of circuit elements such as read only memories. Thus the logical equations embodied herein in gates and flip flops would be realized in connections between sense and readout lines of a read only memory. It will also be appreciated that other arithmetic operations besides add could be used in the calculator—add was simply shown as illustrative of the interaction between arithmetic functions and data handling functions.

WHAT WE CLAIM IS:—

1. An electronic calculator including a stack memory for storing a stack of data words; shifting means for pushing the words in the stack up and down; digit keys for inputting data into the top word position in the stack; an enter key; and control means connected to the enter key and the shifting means for pushing down the stack and leaving the word in the top of the stack unchanged in response to actuation of the enter key.

2. An electronic calculator according to claim 1 and comprising clearing means connected to the stack memory and the digit keys for clearing the top word of the stack memory in response to the actuation of a digit key subsequent to the actuation of the enter key.

3. An electronic calculator according to claim 2 and comprising function keys and function means connected to the stack memory and the function keys for combining the word in the top of the stack with the word in the next memory position, for entering the result of the combination into the top of the stack and for pushing up the rest of the words in the stack in response to the actuation of a function key subsequent to the actuation of the enter key.

4. An electronic calculator according to claim 2 and comprising function keys and function means connected to the stack memory and the function keys for combining the word in the top of the stack with the word in the next memory position, for entering the result of the combination into said next memory position and for pushing up the words in the stack in response to the actuation of a function key subsequent to the actuation of the enter key.

5. An electronic calculator according to any one of claims 3 and 4 and comprising logic means connected to the shifting means and the function means for pushing the stack down in response to the actuation of a data key subsequent to the actuation of a function key.

6. An electronic calculator according to any one of the preceding claims wherein each word includes information representing the algebraic sign of the word comprising at least one bit; and the calculator further comprises a change sign key; complementing means connected to the stack memory for complementing the sign information in the word in the top of the stack in response to actuation of the change sign key; and control means connected to the complementing means and the digit keys for recomplementing the sign information in the word shifted from the top of the stack to the next memory position in response to the actuation of a data key after the actuation of the change key and for complementing the sign information in the word containing data inputted into the stack memory in response to said actuation of a data key.

7. An electronic calculator according to claim 6 and comprising function keys and logic means connected to the function keys and the control means for presetting the control means to respond to the actuation of a data key after the actuation of the change sign key.

8. An electronic calculator according to any one of the preceding claims wherein the calculator further comprises an auxiliary memory; a store key; and control means connected to the store key, the stack memory and the auxiliary memory for duplicating the word in the top of the stack into the auxiliary memory, leaving the word in the top of the stack unchanged, in response to actuation of the store key.

9. An electronic calculator according to claim 8 and comprising clearing means connected to the stack memory and the digit keys for clearing the top word of the stack memory in response to the actuation of a digit key subsequent to the actuation of the store key.

10. An electronic calculator according to

claim 9 and comprising function keys and function means connected to the stack memory and the function keys for combining the word in the top of the stack with the word in the next memory position, for entering the result of the combination into the top of the stack and for pushing up the rest of the words in the stack in response to the actuation of a function key subsequent to the actuation of the store key.

11. An electronic calculator according to claim 10 and comprising function keys and function means connected to the stack memory and the function keys for combining the word in the top of the stack with the word in the next memory position, for entering the result of the combination into said next memory position and for pushing up the words in the stack in response to the actuation of a function key subsequent to the actuation of the enter key.

12. An electronic calculator according to any one of claims 10 and 11 and comprising logic means connected to the shifting means and the function means for pushing the stack down in response to the actuation of a data key subsequent to the actuation of a function key.

13. An electronic calculator substantially as hereinbefore described with reference to the accompanying drawings.

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