RTMP copy

FORMATION OF A METAL VIA USING A RAISED METAL PLUG STRUCTURE

BACKGROUND OF THE INVENTION

(1) FIELD OF THE INVENTION

This invention relates to the fabrication processes use to create semiconductor devices, and more specifically to methods used to create metal via structures, used to interconnect overlying and underlying metallization levels.

(2) BACKGROUND OF THE INVENTION

The semiconductor industry is continually striving to increase the performance of semiconductor devices, while still maintaining, or decreasing, the manufacturing cost of these same semiconductor devices. These objectives have been successfully addressed by the ability of the semiconductor fabrication community to successfully create silicon devices with specific sub-micron features. The advent of micro-miniaturization, or the use of sub-micron features, has largely been accomplished by advances in several semiconductor fabrication disciplines, specifically photolithograhy and anisotropic dry etching. The development of more sophisticated exposure cameras, as well as the use of more

sensitive photoresist materials, have resulted in sub-micron images in photoresist layers being routinely obtained. In addition similar advances in dry etching, or reactive ion etching, (RIE), have allowed the sub-micron images in photoresist layers, to be successfully transferred to underlying materials, used for the construction of silicon devices. The use of sub-micron features results in decreases in parasitic capacitances, as well as resistance decreases, both providing performance benefits. In addition the smaller features allow a greater number of smaller silicon chips to be obtained from a specific size starting wafer, thus reducing the manufacturing cost for individual chips.

The use of semiconductor chips, fabricated with sub-micron features, does however create specific areas of concern, not encountered with semiconductor chips, fabricated with less aggressive designs. For example, metal filled via holes, used to interconnect metallization levels, are more difficult to form when using sub-micron designs. Via holes, with sub micron diameters, are also difficult to fill with conventional metallization deposition techniques, such as sputtering or evaporation. The high aspect ratio of the via hole, that is the depth of the via, divided by the diameter of the via opening, requires a low pressure chemical vapor deposition, (LPCVD) process for adequate via hole filling. Since it is difficult to deposit aluminum based metallizations, using LPCVD, the semiconductor

industry has used LPCVD tungsten to fill these high aspect ratio via holes. However even with the use of LPCVD tungsten, several shortcomings still exist. For example since the LPCVD fill of a via hole proceeds by tungsten depositing on the sides of the via hole, a seam or imperfection can exist in the center of the tungsten filled via, at the point of convergence of the depositing layers. This seam, when subjected to RIE etch back processes, used to remove unwanted tungsten from areas of the silicon device, other than the via hole, can evolve into a larger seam or defect, making it difficult for subsequent overlying metallizations to successfully cover. Thus overlying metallizations, thin in areas overlying the enlarged seam, may experience higher current densities than desired, and possibly resulting in electromigration failure.

This invention will describe a process for creating metal vias, or studs, using a chemically vapor deposited tungsten layer, to fill a narrow contact hole, or via hole opening, in a dielectric layer. However, to avoid expanding the existing seam in the tungsten fill, a photolithographic and reactive ion etching procedure, is used to remove unwanted tungsten from areas outside the contact or via hole vicinity. These process steps, unlike a blanket etchback, will not allow the narrow seam in the tungsten fill to evolve into a more deleterious fault, in areas where the via is directly over the contact hole. In addition this

approach results in a raised, or extended, tungsten plug structure, that is the top surface of the tungsten plug is higher then the top surface of the dielectric layer, that the contact hole was formed in. A first level interconnect metallization structure, is formed from patterning a metal layer, overlying the extended tungsten plug, and when subjected to subsequent insulator deposition and planarization processes, allow successful contact between overlying second level, and underlying first level metal interconnect structures, without the creation of a via hole. Prior art, such as Cote, et al, in U.S. Pat. No.5,312,512, suggest filling holes in a dielectric layer with a metal, followed by a chemical mechanical polishing removal procedure. The concept described in this invention, now disclosed, is to create a raised, or extended metal pattern, using a masked, etchback procedure, with the raised, or extended metal structure to be used to allow contact to subsequent overlying interconnect metallization structures, without via hole formation procedures.

SUMMARY OF THE INVENTION

It is an object of this invention to fill narrow diameter, contact or via holes, with a chemically vapor deposited metallization process.

It is another object of this invention to use photolithographic, and dry etching procedures, to remove the

unwanted metal, and to create a metal plug. For regions where the via overlies the contact hole, the seams or defects in the metal plug, are not subjected to the dry etching procedure, thus resulting in a raised, or extended metal plug structure, where the top surface of the metal plug structure is higher then the top surface of the insulator material, in which the contact hole was etched.

It is yet another object of this invention to create a first level interconnect metallization structure, overlying the raised metal plug structure.

It is still another object of this invention to use a composite dielectric layer, with a insulator layer such as a spin-on-glass layer, used as part of the composite dielectric layer, to fill the spaces between the first level interconnect metallization structures, and between raised metal plug structures..

It is still yet another object of this invention to planarize the composite dielectric layer, followed by formation of an overlying second level interconnect metallization structure, contacting the underlying first level interconnect metallization structure, without the use of a etched via hole.

In accordance with the present invention a method is described for creating a raised or extended, metal filled contact or via structure, formed by chemical vapor deposition and

patterning, using photolithographic and dry etching procedures. A contact hole is formed in an insulator layer, exposing active device regions in an underlying semiconductor substrate. A chemically vapor deposited layer of tungsten is used to completely fill the contact hole. Patterning of the tungsten layer is performed using photolithographic, and dry etching procedures, removing tungsten from unwanted regions, creating a tungsten plug, in the contact hole, with the tungsten plug extending higher than the top surface of the insulator, by an amount that can different or, be equal, to the thickness of the chemically vapor deposited tungsten. A metal layer is deposited and patterned, using photolithographic and dry etching procedures, to create a first level interconnect metallization structure, directly overlying the raised tungsten plug structure. After photoresist removal a composite dielectric layer is used to fill the spaces between first level interconnect metallization structures, and between raised tungsten plug structures. A chemical mechanical polishing procedure is next used for planarization purposes, exposing the top surface of the first level interconnect metallization structure. Another metal layer, is deposited and patterned, using photolithographic and dry etching procedures, creating a second level interconnect metallization structure, contacting the underlying first level interconnect metallization structure.

BRIEF DESCRIPTION OF THE DRAWINGS

The object and other advantages of this invention are best described in the preferred embodiment with reference to the attached drawings that include:

Fig. 1, which schematically shows a silicon device structure, prior to tungsten filling of the contact hole.

Figs. 2 - 3, which schematically show the creation of a raised tungsten plug structure.

Figs. 4 - 6, which schematically show the formation of a first level interconnect metallization structure, directly overlying the raised tungsten plug structure.

Figs. 7 - 8, which schematically show the stages of processing used to fill the spaces between first level interconnect metallization structures, and between raised tungsten plug structures, using a composite insulator layer.

Fig. 9, which schematically shows the formation of an second level interconnect metallization structure, overlying a first level interconnect metallization structure.

Figs. 10 - 12, which schematically shows use of the raised tungsten plug structure, used for upper levels of interconnect metallization structures.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The method of creating raised tungsten plug structures, and the use of this structure in allowing the elimination of a subsequent via hole formation, needed for contact between levels of interconnect metallization structures, will now be covered in detail. This invention can be used in the fabrication of metal oxide semiconductor field effect transistors, (MOSFET), devices, that are currently being manufactured in industry, therefore only specific areas, unique to understanding this invention, will be covered in detail.

Fig. 1, schematically shows a typical, N channel, (NFET), device, that this invention can be applied to. A substrate, 1, composed of single crystalline silicon, with a <100> crystallographic orientation, is used. Thick field oxide regions, (FOX), 2, are created, for isolation purposes. The FOX regions are produced by first patterning a silicon nitride - silicon dioxide, composite insulator, using conventional photolithographic and reactive ion etching, (RIE), procedures. After photoresist removal the composite insulator pattern is used as an oxidation mask to allow between about 4000 to 6000 Angstroms of silicon dioxide to be thermally grown in non-masked regions. After removal of the oxidation masking composite, using hot phosphoric acid for the silicon nitride layer, and a buffered hydrofluoric acid solution for the underlying silicon dioxide layer, a thin silicon oxide

layer, 3, is grown at a temperature between about 800 to 1000°C, to a thickness between about 50 to 300 Angstroms, in an oxygen - steam ambient, to serve as the gate insulator of the MOSFET device. A polysilicon layer is next deposited using LPCVD processing, at a temperature between about 500 to 700°C, to a thickness between about 1500 to 4000 Angstroms. The polysilicon can be grown using insitu doping techniques, by adding either arsine or phosphine to a silane ambient. The polysilicon layer can also be deposited intrinsically, and then doped via ion implantation of either arsenic or phosphorous, at an energy between about 50 to 100 Kev., at a dose between about 1E15 to 1E16 atoms/cm^2. Standard photolithographic and RIE processing, using Cl_2 as an etchant, are used to create polysilicon gate structures, 4, shown schematically in Fig. 1.

After photoresist removal using plasma oxygen ashing and careful wet cleans, an N type, lightly doped source and drain region, 5, is formed in semiconductor substrate, 1, via ion implantation of phosphorous, at an energy between about 30 to 60 Kev., at a dose between about 1E12 to 5E13 atoms/cm^2. A silicon oxide layer is next deposited using either LPCVD or plasma enhanced chemical vapor deposition, (PECVD), processing, at a temperature between about 500 to 800°C, to a thickness between about 1500 to 4000 Angstroms, using tetraethylorthosilicate as a source. An anisotropic, RIE procedure, using CHF_3 as an etchant, is used to

form insulator sidewall spacer, 6, shown schematically in Fig. 1. Another ion implantation procedure, using arsenic at an energy between about 50 to 100 Kev., at a dose between about 1E14 to 5E15 atoms/cm^2, is used to create heavily doped, N type, source and drain regions, 7, in semiconductor substrate, 1. Another silicon oxide layer, 8, is deposited using either LPCVD or PECVD processing, at a temperature between about 500 to 800°C, to a thickness between about 5000 to 10000 Angstroms. Silicon oxide layer, 8, is subjected to a chemical mechanical polishing procedure, used to create a planar topography. Photolithographic and RIE procedures, again using CHF_3 as an etchant, are next used to open contact hole, 9, exposing the top surface of source and drain region, 7. This is shown schematically in Fig. 1.

After photoresist removal, using plasma oxygen ashing and careful wet cleans, an LPCVD deposition of tungsten, 10a, is performed, at a temperature between about 400 to 600°C, to a thickness between about 8000 to 14000 Angstroms, completely filling contact hole, 9. Tungsten layer, 10a, shown in Fig. 2, is deposited using tungsten hexafluoride as a source. The filling of contact hole, 9, proceeds by tungsten deposition on the sides of contact hole, 9, and therefore a seam, 11, forms at the point of convergence of the depositing layers. If seam, 11, was subjected to a blanket, dry etching procedure, used to create a tungsten plug by removal of unwanted tungsten from regions outside

contact hole, 9, seam, 11, would evolve into a larger seam or void, presenting coverage problems for subsequent overlying metallization layers. Therefore a via mask, in the form of photoresist pattern, 12, is created, and used as a mask for an anisotropic RIE procedure using SF_6 as an etchant, creating tungsten plug, 10b, in contact hole, 9, as well as tungsten shape, 10c, to be used for subsequent via structure formation. This can be seen in Fig. 3, after photoresist removal using plasma oxygen ashing and careful wet cleans. Also shown in Fig. 3, is tungsten plug, 10b, raised or extended beyond the top surface of insulator layer, 8, by the amount of the tungsten layer thickness of between about 8000 to 14000 Angstroms. This raised or extended portion of the tungsten plug, will be part of a subsequent first level interconnect metallization structure, that will allow contact to be made to overlying interconnect metallization structures, without having to open via holes in interlevel insulator layers.

A layer of aluminum, 12a, containing between about 0.5 to 1.0 % copper, and between about 0.5 to 1.0 % silicon, shown in Fig. 4, is next deposited, using r.f. sputtering, to a thickness between about 4000 to 10000 Angstroms. Photoresist shapes, 13, shown in Fig. 5, are used as mask for anisotropic, RIE processing, using Cl_2 and BCl_3 as an etchant, and used to create first level interconnect metallization structure, 12b, overlying the raised or extended, tungsten stud, 10b. This is shown schematically in Fig. 6. First level interconnect metallization shapes, 12c, and

12d, also shown in Fig. 6, can be used for subsequent via structure formation. The width of first level interconnect metallization structure, 12b, was chosen, and shown in Fig. 6, to be identical to the width of tungsten plug, 10b. However this invention, of protecting seam, 11, from subsequent dry etching procedures, as well as allowing contact between interconnect metallization structures to occur without the use of etched via holes, can still be applicable with the width of first level interconnect metallization structure, 12b, being either smaller or larger then the width of tungsten plug, 10b. Photoresist shapes, 13, are again removed using plasma oxygen ashing and careful wet cleans.

Figs. 7, describes the process steps used to fill the spaces between first level interconnect metallization structures, 12b, 12c, and 12d, as well as the spaces between tungsten plug structures, 10b and 10c, with a first composite insulator layer. A first interlevel dielectric layer, 14, of silicon oxide, is deposited using PECVD processing, at a temperature between about 300 to 500°C, to a thickness between about 4000 to 8000 Angstroms. The first interlevel dielectric layer, 14, will be used to passivate and protect the first level interconnect metallization structures and tungsten plugs, form subsequent processes and materials. However first interlevel dielectric layer, 14, does not adequately fill the spaces between these metal structures, and can not produce a desired planar topography, needed for overlying

metallization structures, therefore a layer of spin on glass, 15, (SOG), is applied. The porous SOG layer, 15, is applied using conventional techniques, to a thickness between about 3000 to 7000 Angstroms, and results in a more adequate fill, and planarizing layer then the less porous, underlying first interlevel dielectric layer, 14. A bake out at a temperature between about 100 to 200°C, followed by a curing procedure, at a temperature between about 250 to 450°C, are used to remove volatile components from the SOG layer, 15. Finally a second interlevel dielectric layer, 16, is deposited again using PECVD processing, at a temperature between about 300 to 500°C, to a thickness between about 6000 to 12000 Angstroms. This layer is used to completely fill the spaces between metal structures, as well as encapsulating most of the SOG layer, 15, reducing the level of outgassing from SOG layer, 15, during subsequent processing.

A chemical mechanical polishing procedure, using NH_4OH or KOH stabilized slurry and polishing pad, is next employed to a point in which the top surface of a first level interconnect metallization structure, 12b, is exposed. This is shown schematically in Fig. 8. The chemical mechanical polishing step also provides a planar topography for subsequent overlying metallization structures. The ability to expose the top surface of first level interconnect metallization structure, 12b, allows an overlying metallization structure to contact first level

interconnect metallization structure, 12b, without the difficulty of opening a via hole, in an insulator, to underlying structure, 12b. In addition, microloading effects, sometimes occurring with dry etching of via holes, is also avoided using this technique of exposing underlying metallization structures. The raised, or extended, tungsten plug structure, aided in the creation of the first level interconnect metallization structure, 12b, allowing for the elimination of the via hole opening process.

A barrier layer of titanium nitride, 40, is next deposited using r.f sputtering, to a thickness between about 500 to 1000 Angstroms, followed by an insitu, r.f. sputter deposition of an aluminum layer, containing between about 0.5 to 1.0 % copper, and between about 0.5 to 1.0 % silicon, to a thickness between about 4000 to 10000 Angstroms. Conventional photolithographic and anisotropic, RIE processing, is used to create the second level interconnect, aluminum metallization structure, 17b, and 17c, shown in Fig. 9. Photoresist removal is accomplished again via plasma oxygen ashing and careful wet cleans. The second level interconnect metallization structure, 17b, directly contacts underlying first level interconnect metallization structure, 12b, without the use of a via structure. The width of the second level interconnect metallization structure, 17b, is identical to the width of the first level interconnect metallization structure, 12b.

A second composite dielectric layer, 18, identical to the composite dielectric layer shown in Fig. 6, in materials, processing conditions and thicknesses is again used to fill spaces between second level interconnect metallization structures, 17b and 17c. A chemical mechanical polishing procedure, again using NH_4OH or KOH stabilized slurry and polishing pad, is used to planarize second composite dielectric layer, 18, however not exposing the top surface of second level interconnect metallization structures, 17b and 17c. A photolithographic and RIE procedure, using CHF_3 as an etchant, is used to open via hole, 19, in second composite dielectric layer, 18, exposing the top surface of second level interconnect metallization structures, 17b, and 17c. Photoresist removal is accomplished using plasma oxygen ashing and careful wet cleans. This is shown schematically in Fig. 10.

A tungsten layer is next deposited using LPCVD processing, at a temperature between about 400 to 600°C, to a thickness between about 8000 to 14000 Angstroms, using tungsten hexafluoride as a source. Photolithographic and anisotropic, RIE procedures, using SF_6 as an etchant, are employed to create tungsten plug, 20, shown in Fig. 11. Also shown in Fig. 11, is seam 21, formed during the deposition of the tungsten layer, but not enlarged due to the masking provided during the tungsten etchback procedure. Tungsten plug, 20, again as was the case for underlying tungsten plug, 12b, is raised or extended, allowing

contact between subsequent upper level interconnect metallization structures to occur, without the use of via hole processing. Photoresist removal of the shape used as a mask to define tungsten plug, 20, is accomplished via plasma oxygen ashing, and careful wet cleans.

Fig. 12, shows the result of depositing another aluminum based metallization layer, and via use of standard photolithographic and anisotropic, RIE procedures, creating a third level interconnect metallization structure, 22, overlying the raised tungsten plug structure, 20, and identical in width to raised tungsten plug structure, 20. Photoresist removal is again performed using plasma oxygen ashing and careful wet cleans. This is shown schematically in Fig. 12. A third composite insulator layer, 23, again identical to the first and second composite insulator layers, in materials, processing conditions, and thicknesses, is used to fill the spaces between the third level interconnect metallization structures, 22, as well as filling the spaces between raised tungsten plug structures, 20. Chemical mechanical polishing procedures, using NH_4OH or KOH stabilized silica slurry, is used to planarize third composite insulator layer, 23, to a point in which the top surface of the third level interconnect metallization structure, 22, is exposed. This is shown schematically in Fig. 12. Finally another deposition of a barrier layer of titanium nitride, 41, at a thickness of between about 500 to 1000 Angstroms, followed by the deposition of a

aluminum based metallization layer, to a thickness between about 4000 to 10000 Angstroms, and containing between 0.5 to 1.0 % copper, and between about 0.5 to 1.0 % silicon, is performed using r.f. sputtering procedures. Creation of a fourth interconnect metallization structure, 24, is next accomplished via standard photolithographic and RIE processing, again without the use of via hole processing. Photoresist is again removed via plasma oxygen ashing, followed by careful wet cleans.

This process for creating raised tungsten plug structures, allowing contact between levels of interconnect metallization structures to occur without via hole formation, although shown as an application for N channel, (NFET), devices, can also be applied to P channel, (PFET), devices, complimentary, (CMOS), devices, as well as to BiCMOS devices.

While this invention has been particularly shown and described with reference to, the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of this invention.

What is claimed is:



1. A method for fabricating a MOSFET device structure, on a semiconductor substrate, using a raised metal plug structure, to provide contact between an underlying active device region, in said semiconductor substrate, and a overlying interconnect metallization structure, with raised portion of said raised metal plug structure, and overlying interconnect metallization structure, enabling contact to upper level interconnect metallization structures to be accomplished without via hole processing, comprising the steps of:

providing said active device regions, in said semiconductor substrate;

deposition of an insulator layer on said semiconductor substrate, including deposition on said active device regions;

opening a contact hole in said insulator layer, to expose top surface of said active device regions;

deposition of a metal fill layer on top surface of said insulator layer, completely filling said contact hole;

photolithographic processing to create a first photoresist shape on said metal fill layer, larger in width then said contact hole, and directly overlying said contact hole;



anisotropic etching to create a raised metal plug structure, in said contact hole, and on said insulator layer, with raised metal plug structure extending above the top surface of said insulator layer by an amount equal in thickness to the thickness of said metal fill layer;

removal of said first photoresist shape;

deposition of a first metal interconnect layer, on said raised metal plug structure, and on said insulator layer, not covered by said raised metal plug;

photolithographic processing to create a second photoresist shape, on said first metal interconnect layer, directly overlying said raised metal plug structure;

anisotropic etching of said first metal interconnect layer, to form a first level interconnect metallization structure, directly overlying said raised metal plug structure;

removal of said second photoresist shape;

deposition of a first interlevel dielectric layer on said first level interconnect metallization structure, on exposed sidewalls of underlying said raised metal plug structures and on said insulator layer, not covered by said raised metal plug structure;

* C L M S *

application of a spin on glass layer, on said underlying first interlevel dielectric layer, partiall filling the spaces between said first level interconnec metallization structures, and between said raised meta plug structures;

bake out of said spin on glass layer;

curing of said spin on glass layer;

deposition of a second interlevel dielectric layer, on said spin on glass layer, completely filling spaces between said first level interconnect metallization structures, and between said raised metal plug structures;

chemical mechanical polishing to expose top surface of said first level interconnect metallization structure, and planarizing top surface of said first interlevel dielectric layer, top surface of said spin on glass layer, and top surface of said second interlevel dielectric layer;

deposition of a second metal interconnect layer on exposed top surface of said first level interconnect metallization structure, on top surface of said first interlevel dielectric layer, on top surface of said spin on glass layer, and on top surface of said second interlevel dielectric layer; and



patterning of said second metal interconnect layer, to form second level interconnect metallization structure, contacting underlying, said first level interconnect metallization structure.

2. The method of claim 1, wherein said contact hole is created, in said insulator layer, via anisotropic RIE processing, using CHF_3 as an etchant, with said contact hole having an opening between about 0.5 to 2.0 uM, in width.

3. The method of claim 1, wherein said metal fill layer is tungsten, deposited using LPCVD processing, at a temperature between about 400 to 600°C, to a thickness between about 8000 to 14000 Angstroms, using tungsten hexafluoride as a source.

4. The method of claim 1, wherein said raised metal plug structure is formed using anisotropic RIE processing, using SF_6 as an etchant, with said raised metal plug having a width between about 0.5 to 2.0 uM, and extending between about 8000 to 14000 Angstroms, above the top surface of said insulator layer.

* C L M S *

5. The method of claim 1, wherein said first metal interconnect layer is aluminum, containing between about 0.5 to 1.0 % copper, and between about 0.5 to 1.0 % silicon, deposited using r.f. sputtering, to a thickness between about 4000 to 10000 Angstroms.

6. The method of claim 1, wherein said first level interconnect metallization structure is formed using anisotropic RIE processing, using Cl_2 and BCl_3 as an etchant, with said first level interconnect metallization structure having a width between about 0.5 to 2.0 uM.

7. The method of claim 1, wherein said first interlevel dielectric layer is silicon oxide, deposited using PECVD processing, at a temperature between about 300 to 500°C, to a thickness between about 4000 to 8000 Angstroms.

8. The method of claim 1, wherein said spin on glass layer is applied to a thickness between about 3000 to 7000 Angstroms.

9. The method of claim 1, wherein said spin on glass layer is baked at a temperature between about 100 to 200°C, and cured at a temperature between about 250 to 450°C.



10. The method of claim 1, wherein said second interlevel dielectric layer is silicon oxide, deposited using PECVD processing, at a temperature between about 300 to 500°C, to a thickness between about 6000 to 12000 Angstroms.

11. The method of claim 1, wherein chemical mechanical polishing, used to expose top surface of said first level interconnect metallization structure, is performed using NH_4OH or KOH stabilized silica slurry and polishing pad.

12. The method of claim 1, wherein said second metal interconnect layer is aluminum, containing between about 0.5 to % copper, and between about 0.5 to 1.0 % silicon, deposited using r.f. sputtering, to a thickness between about 4000 to 10000 Angstroms.

13. The method of claim 1, wherein said second level interconnect metallization structure is formed using anisotropic RIE processing, using SF_6 as an etchant.



14. A method for fabricating a MOSFET device structure, on a semiconductor substrate, using a raised tungsten plug structure, to provide contact between an underlying active device region, in said semiconductor structure, and an overlying, first aluminum based, interconnect structure, with raised portion of said raised tungsten plug structure, and said overlying, first aluminum based, interconnect structure, enabling contact to upper levels of interconnect metallization structures, to be accomplished without the use of via hole processing, comprising the steps of:

providing said active device regions, in said semiconductor substrate;

deposition of an insulator layer on said semiconductor substrate, including deposition on said active device regions;

opening a contact hole in said insulator layer, to expose top surface of said active device regions;

deposition of a tungsten fill layer on top surface of said insulator layer, and completely filling said contact hole;

forming a first photoresist shape on underlying said tungsten fill layer, directly overlying said contact hole, with said first photoresist shape having a width, larger then the width of said contact hole;

* C L M S *

anisotropic etching of said tungsten fill layer to create a raised tungsten plug structure, in said contact hole and on said insulator layer, with said raised tungsten plug structure extending above the top surface of said insulator layer by an amount equal to the thickness of said tungsten fill layer;

removal of said first photoresist shape;

deposition of a first aluminum based, interconnect layer, on said raised tungsten plug structure, and on said insulator layer, not covered by said raised tungsten plug structure;

forming a second photoresist shape on underlying, said first aluminum, interconnect layer, directly overlying said raised tungsten plug structure;

anisotropic etching of said first aluminum based, interconnect layer, to create a first aluminum based, interconnect structure, directly overlying said raised tungsten plug structure;

removal of said second photoresist shape;

deposition of a first silicon oxide, interlevel layer, on said first aluminum based, interconnect structure, on exposed sidewalls of underlying, raised tungsten structure, and on said insulator layer, not covered by said raised tungsten plug structure;



application of a spin on glass layer, on said first silicon oxide, interlevel layer, partially filling the spaces between said first aluminum based, interconnect structures, and between said raised tungsten plug structures;

bake out of said spin on glass layer;

curing of said spin on glass layer;

deposition of a second silicon oxide, interlevel layer, on said spin on glass layer, completely filling the spaces between said first aluminum based, interconnect structures, and between said raised tungsten plug structures;

chemical mechanical polishing to expose top surface of said first aluminum based, interconnect structure, and planarizing top surface of said first silicon oxide, interlevel layer, top surface of said spin on glass layer, and top surface of said second silicon oxide, interlevel layer;

deposition of a second aluminum based, interconnect layer, on exposed top surface of said first aluminum based, interconnect structure, on top surface of said first silicon oxide, interlevel layer, on top surface of said spin on glass layer, and on top surface of said second silicon oxide, interlevel layer; and



patterning of said second aluminum based, interconnect layer, to form second aluminum based, interconnect structure, directly contacting underlying, said first aluminum based, interconnect structure.

15. The method of claim 14, wherein said contact hole is opened in said insulator layer using anisotropic RIE processing, using CHF_3 as an etchant, with said contact hole having an opening with a width between about 0.5 to 2.0 uM.

16. The method of claim 14, wherein said tungsten fill layer is deposited using LPCVD processing, at a temperature between about 400 to 600°C, to a thickness between about 8000 to 14000 Angstroms, using tungsten hexafluoride as a source.

17. The method of claim 14, wherein said raised tungsten plug structure is formed using anisotropic RIE processing, using SF_6 as an etchant, with said raised tungsten plug structure having a width between about 0.5 to 2.0 uM, and extending between about 8000 to 14000 Angstroms, above the top surface of said insulator layer.



18. The method of claim 14, wherein said first aluminum based, interconnect layer, is aluminum containing between about 0.5 to 1.0 % copper, and between about 0.5 to 1.0 % silicon, deposited using r.f. sputtering, to a thickness between about 4000 to 10000 Angstroms.

19. The method of claim 14, wherein said first aluminum based, interconnect structure is formed using anisotropic RIE processing, using Cl_2 and BCl_3 as an etchant, with said first aluminum based, interconnect structure having a width between about 0.5 to 2.0 uM.

20. The method of claim 14, wherein said first silicon oxide, interlevel layer, is deposited using PECVD processing, at a temperature between about 300 to 500°C, to a thickness between about 4000 to 8000 Angstroms.

21. The method of claim 14, wherein said spin on glass layer is applied to a thickness between about 3000 to 7000 Angstroms.

22. The method of claim 14, wherein said spin on glass layer is baked at a temperature between about 100 to 200°C, and cured at a temperature between about 250 to 450°C.



23. The method of claim 14, wherein said second silicon oxide, interlevel layer, is deposited using PECVD processing, at a temperature between about 300 to 500°C, to a thickness between about 6000 to 12000 Angstroms.

24. The method of claim 14, wherein chemical mechanical polishing, used to expose top surface of said first aluminum based, interconnect structure, is performed using NH_4OH or KOH stabilized silica slurry and polishing pad.

25. The method of claim 14, wherein said second aluminum based, interconnect layer, is aluminum, containing between about 0.5 to 1.0 % copper, and between about 0.5 to 1.0 % silicon, deposited using r.f. sputtering, to a thickness between about 4000 to 10000 Angstroms.

26. The method of claim 14, wherein said second aluminum based, interconnect structure, is formed using anisotropic RIE processing, using Cl_2 and BCl_3 as an etchant.



27. A MOSFET device structure, on a semiconductor substrate, comprising:

field oxide regions on the surface of said semiconductor substrate;

a device region between said field oxide regions;

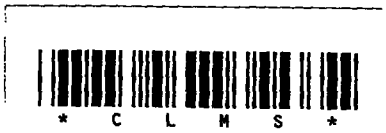
a polysilicon gate structure on said semiconductor substrate, in center of said device region;

source and drain regions in surface of said semiconductor substrate, between said polysilicon gate structure and said field oxide region;

an insulator layer located on said source and drain regions, on said polysilicon gate structure, and on said field oxide regions;

a contact hole, in said insulator layer, to said source and drain regions, filled with a metal plug structure, with said metal plug structure extended above top surface of said insulator layer;

a first interconnect metallization structure, directly overlying said metal plug structure;



a composite insulator layer filling spaces between said first interconnect metallization structures, and between said metal plug structures, with said composite insulator layer having a planar topography, planarized to a point in which top surface of said composite insulator layer, and top surface of first interconnect metallization layer, are equal; and

a second interconnect metallization structure, directly contacting top surface of underlying said first metallization structure.

28. The MOSFET device structure of claim 27, wherein said contact hole is created with a width between about 0.5 to 2.0 uM.

29. The MOSFET device structure of claim 27, wherein said metal plug structure, is composed of tungsten, with a width between about 0.5 to 2.0 uM, and extending above top surface of said insulator layer by between about 8000 to 14000 Angstroms.

30. The MOSFET device structure of claim 27, wherein said first interconnect metallization structure, is composed of aluminum, containing between about 0.5 to 1.0 % copper, and between about 0.5 to 1.0 % silicon, formed to a thickness between about 4000 to 10000 Angstroms, and to a width between about 0.5 to 2.0 uM.

31. The MOSFET device structure of claim 27, wherein said composite insulator layer is composed of: an underlying, first silicon oxide layer, at a thickness between about 4000 to 8000 Angstroms; a spin on glass layer, at a thickness between about 3000 to 7000 Angstroms; and an overlying silicon oxide layer, at a thickness between about 6000 to 12000 Angstroms.

* C L M S *

FORMATION OF A METAL VIA USING A RAISED METAL PLUG STRUCTURE

ABSTRACT

A process has been developed which allows contact between levels of interconnect metallization structures, to occur without the use of via holes, etched in interlevel insulator layers. The process features creation of a raised tungsten plug structure, used to provide contact between underlying active device regions and an overlying interconnect metallization structure. The tungsten plug structure is formed by photolithographic masking and dry etching procedures, thus avoiding increasing the size of a tungsten seam, in the center of the plug structure. In addition the tungsten definition process, also results in a raised plug structure, allowing subsequent contact of interconnect metallization levels to proceed without the use of etched via holes in interlevel insulator layers.

(FIGURE 1 IS SUGGESTED FOR PUBLICATION)

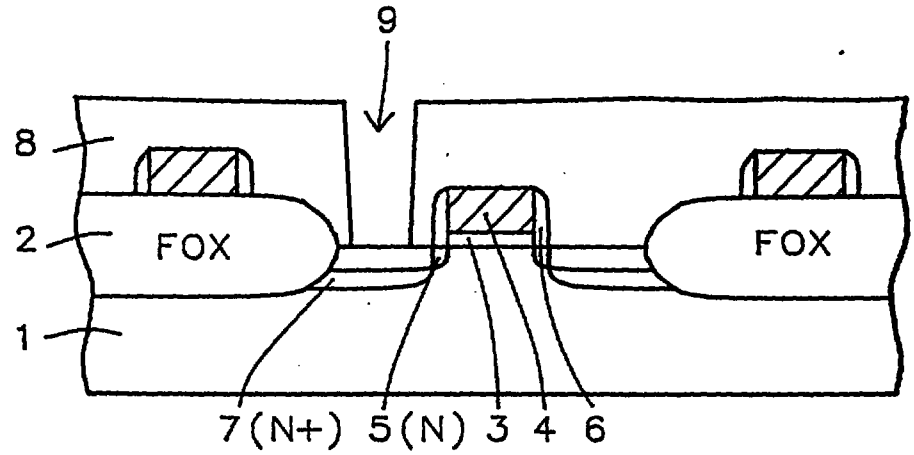


FIG. 1

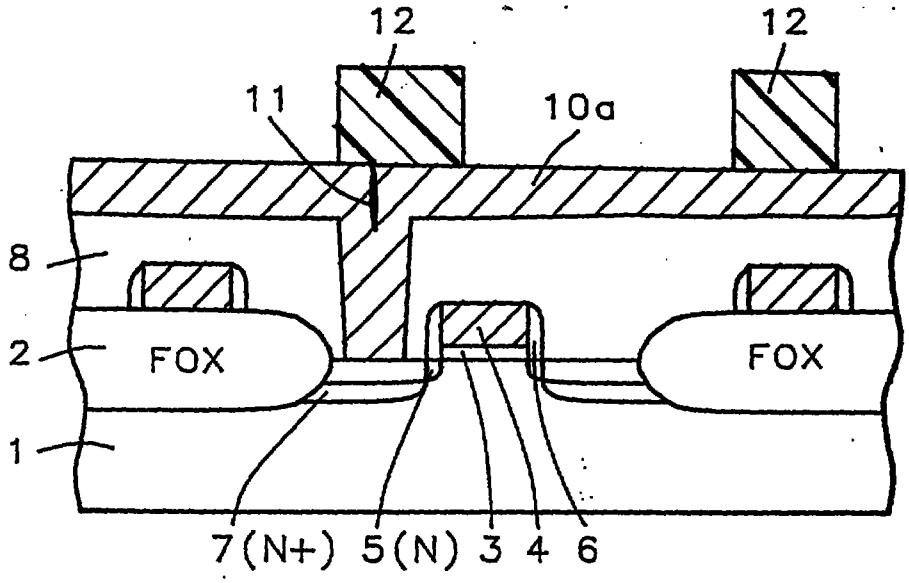


FIG. 2

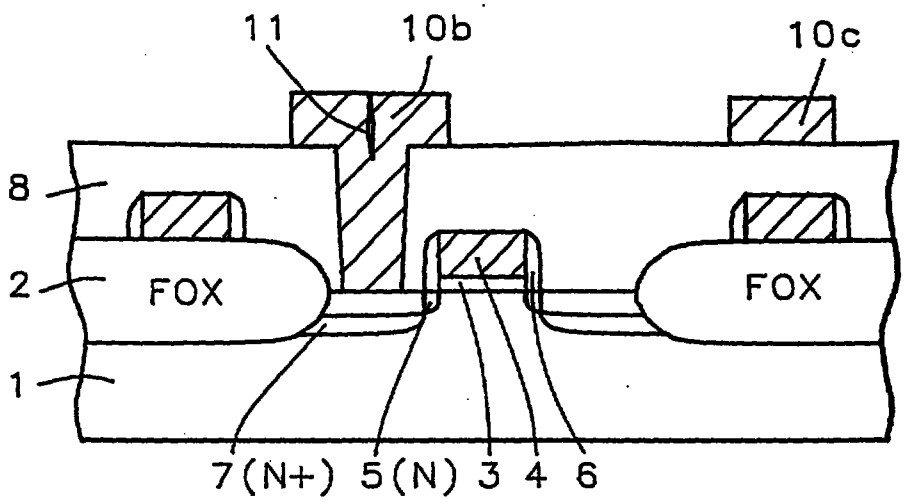

11
10b
10c
8
2
FOX
FOX
1
7(N+)
5(N)
3
4
6

FIG. 3

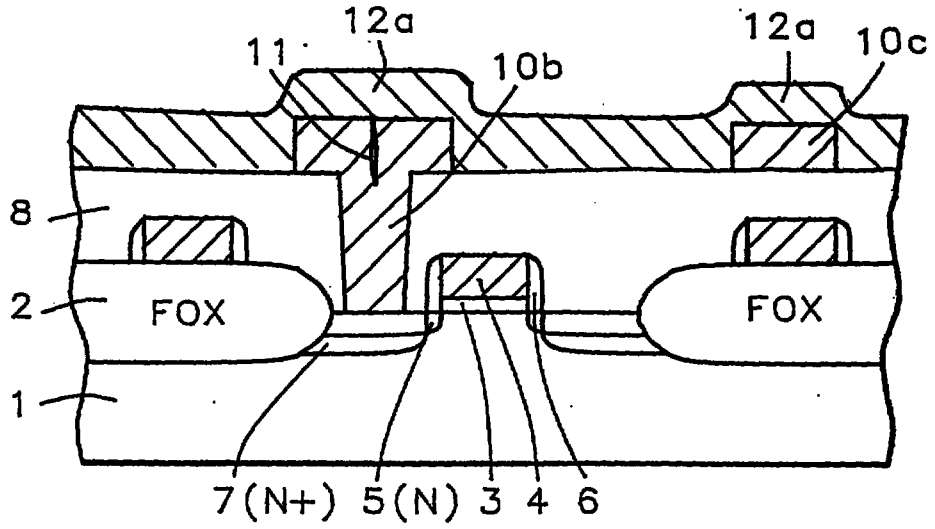

12a
11
10b
12a
10c
8
2
FOX
FOX
1
7(N+)
5(N)
3
4
6

FIG. 4

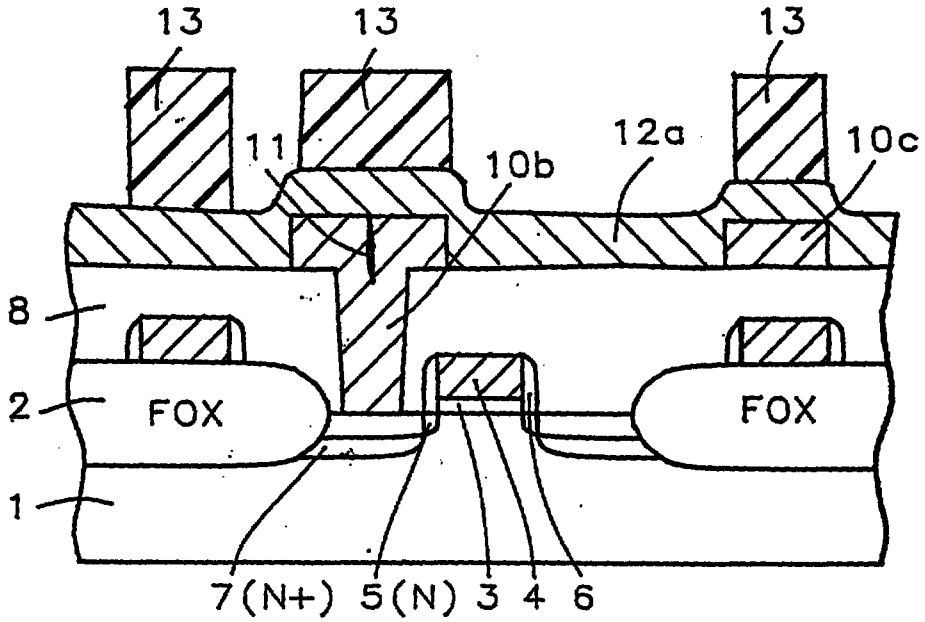

13
13
13
11
10b
12a
10c
8
2
FOX
FOX
1
7(N+)
5(N)
3
4
6

FIG. 5

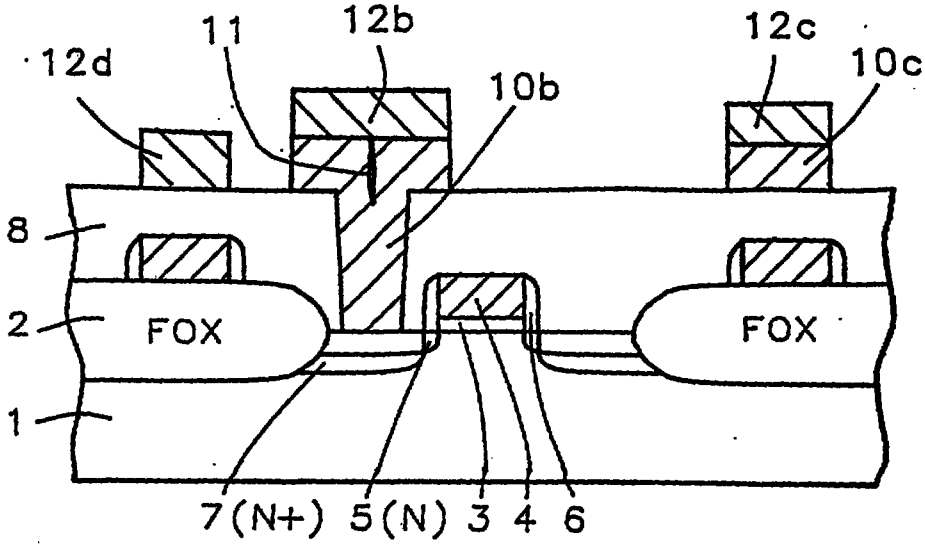

11
12b
12c
12d
10b
10c
8
2
FOX
FOX
1
7(N+)
5(N)
3
4
6

FIG. 6

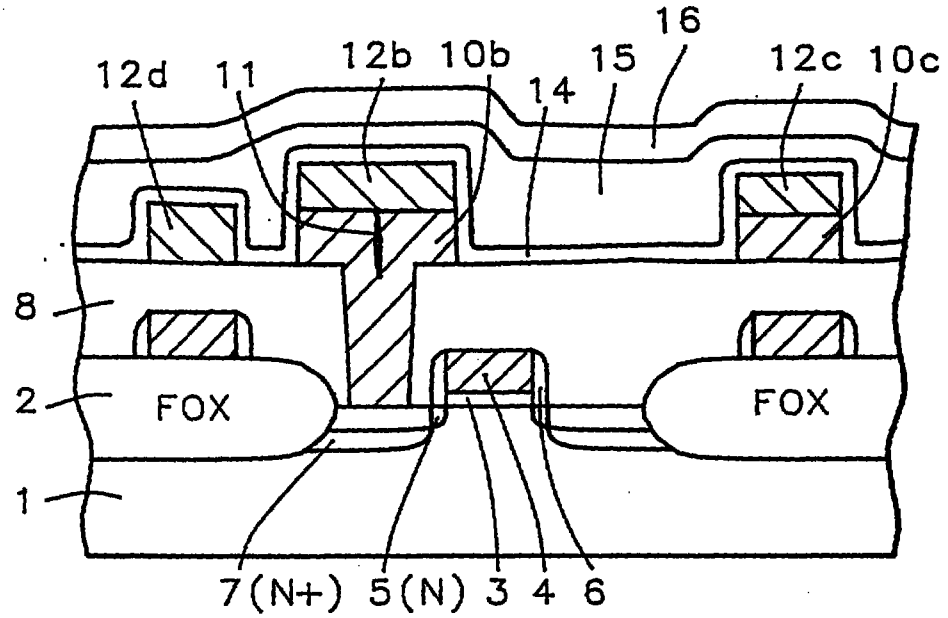

16
12d
11
12b
10b
15
12c
10c
14
8
2
FOX
FOX
1
7(N+)
5(N)
3
4
6

FIG. 7

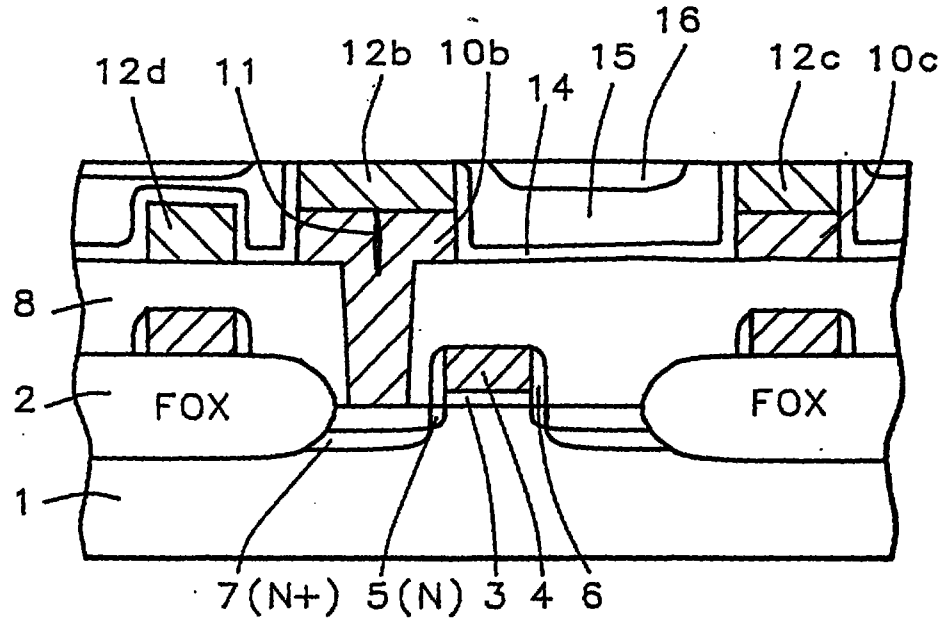

16
12d
11
12b
10b
15
12c
10c
14
8
2
FOX
FOX
1
7(N+)
5(N)
3
4
6

FIG. 8

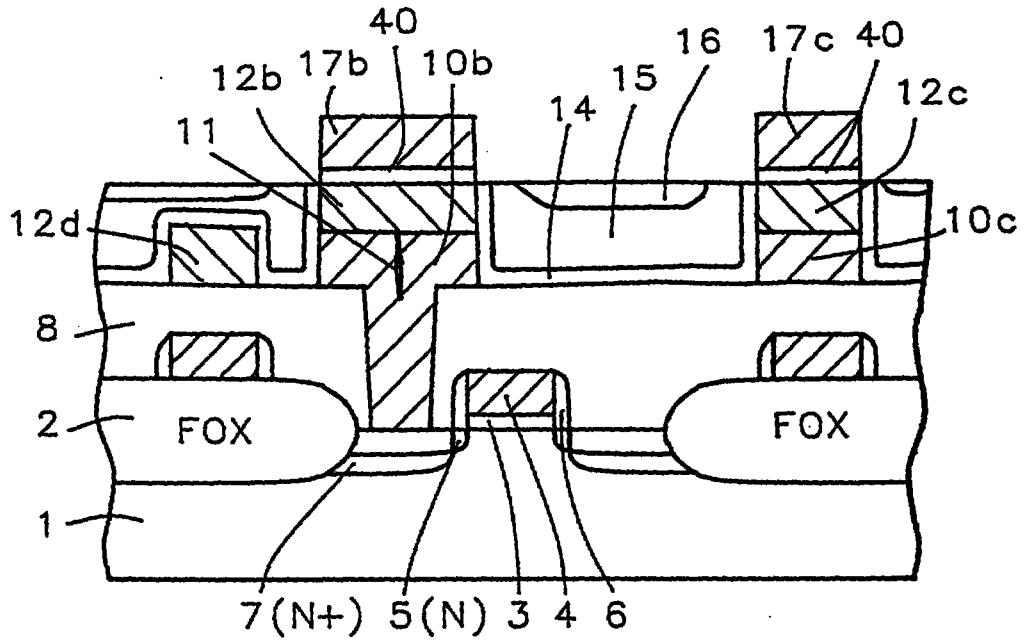

40
12b
17b
10b
16
17c
40
15
14
12c
11
12d
10c
8
2
FOX
FOX
1
7(N+)
5(N)
3
4
6

FIG. 9

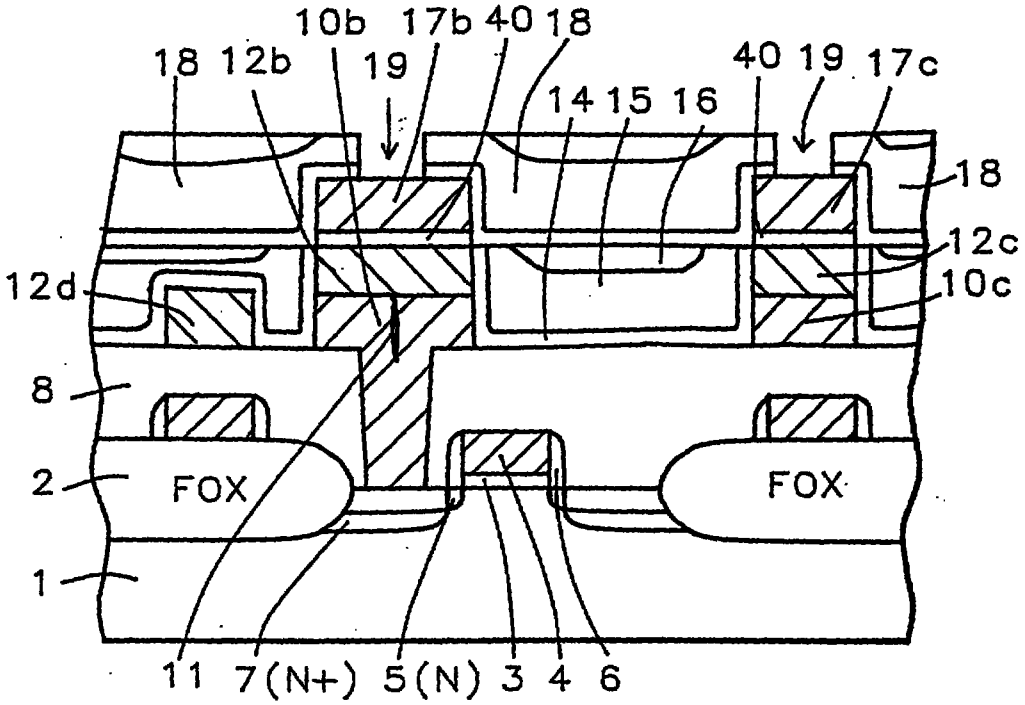

10b
17b
40
18
18
12b
19
40
19
17c
14
15
16
18
12c
12d
10c
8
2
FOX
FOX
1
11
7(N+)
5(N)
3
4
6

FIG. 10

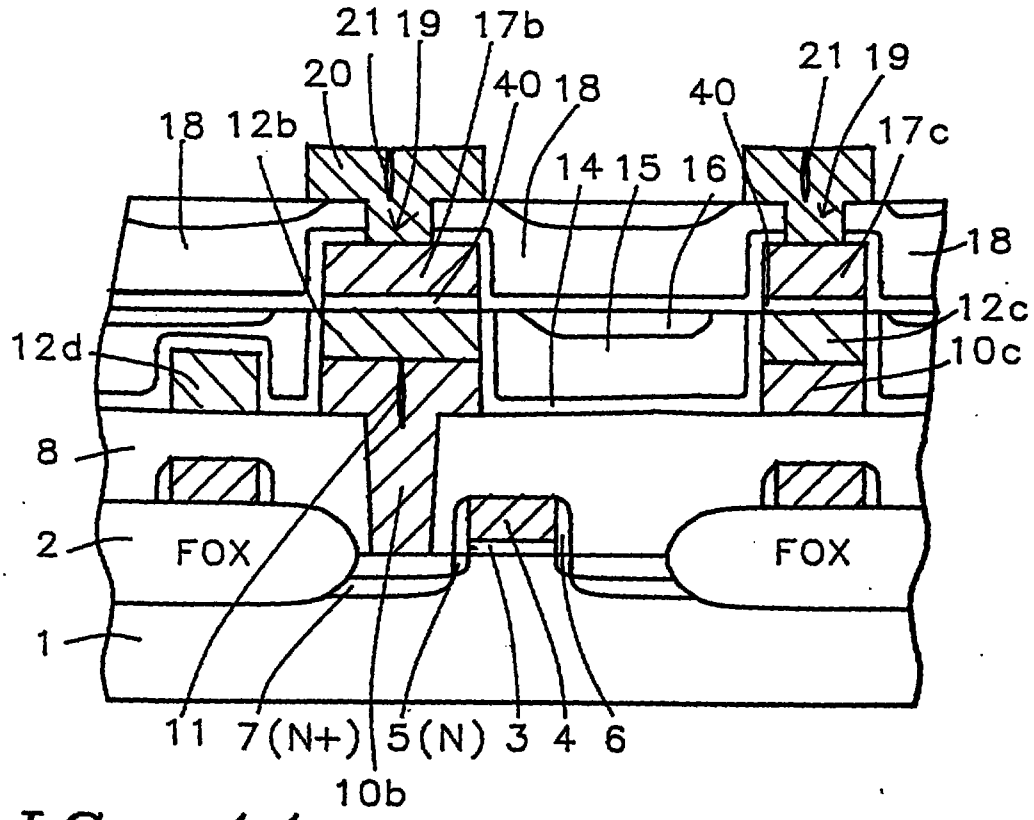

21 19 17b
20
40 18
40
21 19
18 12b
14 15 16
17c
18
12c
12d
10c
8
2
FOX
FOX
1
11 7(N+) 5(N) 3 4 6
10b

FIG. 11

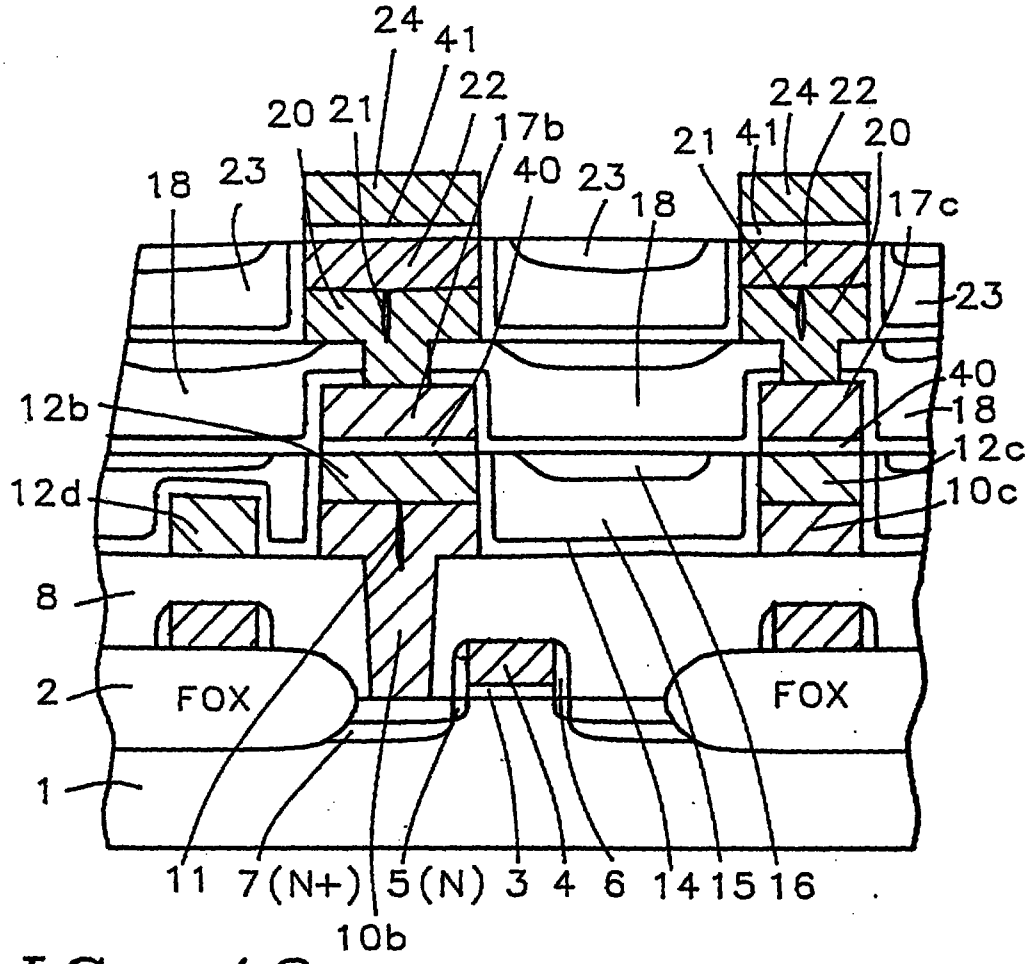

24
41
22
20
21
17b
40
23
18
24
22
21
41
20
17c
23
40
18
12c
10c
12b
12d
8
2
1
FOX
FOX
11
7(N+)
10b
5(N)
3
4
6
14
15
16

FIG. 12