CLAIMS:

1. A method for assembling components onto a product substrate, the method comprising:

selectively picking one or more elements from a source wafer by a vacuum superstrate attached to said one or more elements;

placing said selectively picked one or more elements onto said product substrate, wherein said placing is performed with sub-25 nm placement precision; and

securely attaching said selectively picked one or more elements onto said product substrate using direct bonding by holding onto said one or more elements using said vacuum superstrate until said attachment occurs.

2. The method as recited in claim 1, wherein a distribution of said selectively picked one or more elements is arbitrary.

3. The method as recited in claim 1, wherein said one or more elements are selectively picked from said source wafer using a pick-and-place method, wherein said pick-and-place is highly parallel.

4. The method as recited in claim 1, wherein said one or more elements vary in size from sub-10 micrometers on a side to over 1 millimeter on a side.

5. The method as recited in claim 1, wherein assembling of said one or more elements further achieves sub-10 nm placement precision.

6. The method as recited in claim 1, wherein said placement precision is achieved using a moiré metrology scheme.

7. The method as recited in claim 1, wherein temperature control techniques are used for distortion control of said picked one or more elements.

8. The method as recited in claim 1, wherein said method is used for constructing Application Specific Integrated Circuits (ASICs).

9. The method as recited in claim 1 further comprising:

implementing a subsequent vacuum deposition process to further secure said attached one or more elements.

10. The method as recited in claim 1, wherein, once said product substrate has been fully populated with elements, one or more of a material deposition and a coating is performed, followed by a planarization.

11. The method as recited in claim 10, wherein said planarization utilizes one or more of the following: an inkjet-based planarization and a chemical mechanical polishing.

12. The method as recited in claim 1, wherein said one or more elements are selectively picked from said source wafer using vacuum-based pickup, wherein valves are used to activate vacuum holes on said vacuum superstrate to enable said vacuum-based pickup.

13. The method as recited in claim 12, wherein said activation of said vacuum holes is performed in an addressable manner.

14. A method for assembling components onto a product substrate, the method comprising:

selectively picking one or more elements with a distribution from a source wafer by a vacuum superstrate attached to said one or more elements;

placing said selectively picked one or more elements onto said product substrate, wherein said placing is performed with sub-25 nm placement precision, wherein said sub-25 nm placement precision is enabled by in-liquid fine alignment, and

securely attaching said selectively picked one or more elements onto said product substrate by holding onto said one or more elements using said vacuum superstrate until attachment occurs.

15. The method as recited in claim 14, wherein a distribution of said selectively picked one or more elements is arbitrary.

16. The method as recited in claim 14, wherein said one or more elements are selectively picked from said source wafer using a pick-and-place method, wherein said pick-and-place is highly parallel.

17. The method as recited in claim 14, wherein said one or more elements vary in size from sub-10 micrometers on a side to over 1 millimeter on a side.

18. The method as recited in claim 14, wherein assembling of said one or more elements further achieves sub-10 nm placement precision.

19. The method as recited in claim 14, wherein said placement precision is achieved using a moiré metrology scheme.

20. The method as recited in claim 14, wherein temperature control techniques are used for distortion control of said picked one or more elements.

21. The method as recited in claim 14, wherein said method is used for constructing Application Specific Integrated Circuits (ASICs).

22. The method as recited in claim 14 further comprising:

implementing a subsequent vacuum deposition process to further secure said attached one or more elements.

23. The method as recited in claim 14, wherein, once said product substrate has been fully populated with elements, one or more of a material deposition and a coating is performed, followed by a planarization.

24. The method as recited in claim 23, wherein said planarization utilizes one or more of the following: an inkjet-based planarization and a chemical mechanical polishing.

25. The method as recited in claim 14, wherein said one or more elements are selectively picked from said source wafer using vacuum-based pickup, wherein valves are used to activate vacuum holes on said vacuum superstrate to enable said vacuum-based pickup.