

PATENT SPECIFICATION

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(54) CURRENT DIVIDING CIRCUITS

(71) We, RCA CORPORATION, a corporation organized under the laws of the State of Delaware, United States of America, of 30 Rockefeller Plaza, City and State of New York, 10020, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to current dividing circuits and is useful particularly to such circuits for phase shifting in the chrominance channel of a color television receiver. The circuit configurations are particularly adapted to integrated circuit techniques.

In a color television receiver it is desirable to have a control which serves to vary the phase of the chrominance signals with respect to the color oscillator signal or vice versa, prior to the application of such signals to the demodulators. Such a control serves to produce a change in the hue or tint of the display according to the preference of the viewer.

The prior art discloses many circuits for providing tint control. Such circuits utilize variable capacitors, inductors, and resistors, or combinations thereof, for providing a phase change over a given range.

In the integrated circuit environment, variable components are difficult to fabricate, and in general, difficult to utilize, except in certain "off-board" configurations. However, a prime concern of the integrated circuit art is to provide a function with a minimum of terminals associated with the integrated circuit chip for interfacing with the external environment.

Another desirable feature to be incorporated with a tint or phase control network is to provide the desired amount of phase shift upon application to the circuit of a specified d.c. voltage. In this manner, such a circuit can be easily adapted for remote control activation without the need to provide mechanically variable components.

Due to the limits of the phase angle control

as affecting tint and, therefore, the picture quality, reliable centering of the tint range is desired without dependence upon the exact magnitude of the supply potential or temperature drifts. Furthermore, a desirable feature of the tint control arrangement is to provide a range of suitable phase variation without an accompanying change in amplitude of the signal components as applied to the demodulators.

According to the present invention, a current dividing circuit adaptable for such tint control comprises first and second semiconductor devices each having at least first and second electrodes, the second electrodes of said devices being coupled to a common circuit junction, bias current means coupled to said junction for providing forward bias direct current components to each of said devices, said bias current means including means for establishing a substantially constant quiescent value of bias current through the emitter-collector path of a third semiconductor device in the form of a first transistor having its collector electrode direct current coupled to said junction, signal input means coupled to said junction for supplying signal currents to said devices, means coupled to said first electrode of said first device for by-passing signal currents to a point of reference potential, variable impedance means coupled to said first electrode of said first device for supplying a variable control current to said first device so as to vary proportioning of signal currents traversing said first and second devices between said first and second electrodes thereof, and output signal utilization means coupled to said first electrode of said second device for deriving output signals determined by said input signals and said control current. An embodiment of the invention and its use for tint control in a color television receiver will now be described by way of Example with reference to the accompanying drawings in which:

FIGURE 1 is a schematic diagram in block form of a color television receiver employing

[Price 25p]

Price 75p

an integrated circuit arrangement including a phase shift current dividing circuit according to this invention.

FIGURE 2 comprising sub Figures 2A and 2B is a detailed schematic diagram of the integrated circuit chip shown in FIGURE 1. "FIGURE 2" is used to denote both sub Figures.

Referring to FIGURE 1, there is shown a schematic diagram in block form of a color television receiver utilizing a color processing integrated circuit chip employing a d.c. tint control according to this invention.

A television antenna 10 is adapted to receive radio frequency signal transmissions in the television band and couple such signals to the input terminals of a front end circuit 11. The circuit 11 conventionally selects and processes the RF signals to provide an intermediate frequency signal. The intermediate frequency signals are demodulated by the video detector and amplifier circuitry 12 to provide a video signal containing information pertinent to the final display content, including synchronization and other information.

The video signal is applied to a luminance amplifier channel 13 having an output for driving a color kinescope display device 14. Video signals from the luminance channel 13 are applied to synchronization, deflection and automatic gain control circuitry 15 to assure the formation of a stable raster by the kinescope 14, in providing synchronized vertical and horizontal waveshapes to the deflection coil 16 associated with the kinescope 14. The circuitry 15 may further provide suitable operating potentials for the kinescope 14, which may be a three gun shadow mask device.

The video signal is also applied to a chrominance channel having a chrominance amplifier stage 17 for processing and amplifying the higher frequency components of the composite signal, containing the chrominance sidebands transmitted with the composite signal during a color transmission. An output from the chrominance amplifier 17 is coupled to an input of a burst separator amplifier 18. The function of the burst separator amplifier 18 is to respond to a gate pulse, generated by the deflection circuits 15 and in synchronism with the horizontal retrace interval, to provide an amplified version of the oscillatory burst signal transmitted along with the composite signal during a color transmission. The output of the burst separator 18 is coupled to an input of an oscillator 19. The oscillator 19 is synchronized to the burst, as received, in order to provide an output signal useful for reliable demodulation of the chrominance subcarrier components transmitted with the composite signal and representative of the color content of the scene.

Generally speaking, the output of the locked

oscillator 19, and the output of the chrominance amplifier 17 are applied to suitable demodulator circuits in the receiver where they are synchronously demodulated to provide color difference signals or color signals representative of the colors transmitted by the station. The output of the chrominance amplifier 17 is applied to the color processing integrated circuit (IC) chip 20 and it is coupled to an output of circuitry located thereon and indicated in block diagram form as color demodulators 21. The output signal of the burst locked oscillator 19 is also applied to the color processing integrated circuit chip 20, indicated by the dotted line, by coupling the output terminal of the oscillator 19 to an input of the circuit referenced as tint control 22.

The function of the tint control circuit 22 is to change the phase of the burst locked oscillator 19 signal, to provide the viewer with means for adjusting the relative hue of the picture. Alternatively, phase control may be provided by changing the phase of the chrominance signals and the disclosed embodiments may be utilized in this manner as well.

Hue or tint control is pertinent to the reproduction of flesh tones as well as other colors generated on the viewing screen of the kinescope 14. The output of the tint control 22 is coupled to suitable demodulator driver amplifiers 23 for application to suitable inputs of the color demodulator 21. The function of the color demodulators 21, as indicated briefly above, is to demodulate the chrominance subcarrier frequency components, transmitted with the composite signal, with respect to suitable phases of the color oscillator signal, to provide at an output thereof the color difference signals which are conventionally the B-Y, R-Y, and G-Y signals. The color difference signals are applied to output driver amplifiers 24 for subsequent application to suitable amplifier or isolating stages 29 and thence for application to electrodes, such as the grid electrodes of the kinescope 14.

The above noted functions are those which are ordinarily supplied by many conventional television receivers utilizing discrete components, as well as those receivers which may utilize integrated circuit components. The invention concerns itself with techniques applicable to the color processing integrated circuit chip 20 for providing a convenient means of tint control for the oscillator reference signal prior to demodulation; while further describing suitable biasing and driving techniques for amplifier configurations necessary for proper operation of balanced demodulator circuits utilized on the integrated circuit chip 20.

The typical problems which are of concern to the integrated circuit designer concern temperature stability, power supply dependence and the conservation of terminals. The solu-

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tions to such techniques as utilized to circumvent certain problems will be more clearly described if reference is made to FIGURE 2, which is a detailed schematic diagram of the color processing integrated circuit chip 20, shown in FIGURE 1. The dotted line 20 in FIGURE 2 indicates the boundary of the integrated circuit chip with the components inside of the dotted line being part of the monolithic integrated chip and those outside of the dotted line being off the body of the integrated chip. The small circles on the dotted line 20 represent the terminals of the integrated chip.

The output from the oscillator 19, shown in FIGURE 1, is applied to the base electrode of transistor 30 which forms part of a differential amplifier with the transistor 31. The differential amplifier configuration includes a constant current source transistor 33 having a collector electrode coupled to the emitter electrodes of transistors 30 and 31. The emitter electrode of transistor 33 is returned to the point of reference potential.

A bias arrangement for the constant current source transistor 33 is provided by the series resistors 44, 45, 46, and 47 coupled between the base electrode of transistor 33 and the source of operating potential or supply bus 34. A diode 55 coupled between the base electrode of transistor 33 and ground serves to determine the current bias of transistor 33 and the overall temperature stability.

Transistor 31 of the differential amplifier has its collector electrode returned to the positive supply bus 34 via a resistor 36 which is shunted by a capacitor 37. This R-C network provides a reference phase angle for the tint control circuit to be described subsequently.

The collector electrode of transistor 30 is coupled to the emitter electrode of a transistor 38 which provides a collector load to transistor 30. The collector of transistor 38 is coupled to the emitter electrode of a transistor 40 via a resistor 41. Transistor 40 is arranged in an emitter follower configuration and has its collector electrode coupled to the positive supply bus 34.

The base electrode of transistor 40 is coupled to the junction of the collector electrode of transistor 31 and resistor 36 for supplying operating bias to transistor 40. Transistor 40 serves to transform the signal source as evidenced by the voltage across the R-C network into a low impedance voltage source for coupling to the collector electrode of transistor 38.

The emitter electrode of transistor 40 is further coupled to the collector electrode of a biasing transistor 42, having its emitter electrode coupled to the base electrode of transistor 38 for supplying an operating bias thereto and returned to ground through resistor 43. Biasing for the base electrode of transis-

tor 42 is obtained through the common divider used for biasing the constant current source transistor 33, by means of resistors 44 and 45 forming part of the above noted divider. Transistor 42 serves to prevent transistor 40 from undesirably operating as a detector for low level signals.

The emitter electrode of transistor 38 is coupled to the emitter electrode of a transistor 50 having its base and collector electrodes connected together and, therefore, operated in a diode configuration. The diode formed by utilizing the transistor in this manner matches the base to emitter diodes of the transistors utilized on the integrated circuit chip and serves to aid in temperature tracking and biasing stabilization.

The common terminal formed by coupling the base electrode to the collector electrode of transistor 50 is coupled to an external potentiometer 51 having a terminal thereof coupled to a source of operating potential designated as $+V_s$, and relatively of the same magnitude as that potential applied to the bus 34. The potentiometer 51 is bypassed for chrominance signal frequencies by capacitor 54.

The function of resistor 51 is to determine the amount of current flowing through the collector to base connected transistor 50 which in turn determines the amount of current flowing through transistor 38. This control serves to provide phase shifts by operating on the vector currents or complex currents developed by the differential amplifier circuit using transistors 30 and 31 in conjunction with the biasing arrangement. This particular operation will be described in greater detail subsequently.

Transistor 38 provides at its collector electrode a signal which is representative of the oscillator reference signal as phase shifted according to the setting of potentiometer 51. The collector electrode of transistor 38 is coupled to the base electrode of a transistor 57 arranged in an emitter follower configuration and used to drive a limiting differential amplifier including transistor 58 and 59. The emitter electrode of transistor 57 is direct coupled to the base electrode of transistor 58 and coupled to the base electrode of transistor 59 via a resistor 60.

Transistor 58 drives transistor 59 via the emitter connection and the output collector electrode of transistor 59 is connected to the $+V_s$ supply via external resistor 65. Transistor 59 in conjunction with the magnitude of resistor 65 and the drive applied to its emitter electrode thus provides a large and constant amplitude voltage swing between the $+V_s$ supply and the collector to emitter saturation voltage of transistor 59 for varying magnitude input signals. The differential amplifier including transistors 58 and 59 therefore serves to limit the signal to pro-

vide a constant amplitude signal at the output for a wide range of different amplitude input signals.

5 Biasing for the limiting differential amplifier comprising transistors 58 and 59 is provided by a constant current source transistor 61 arranged in a common collector configuration and having its collector electrode coupled to the junction between the emitter electrodes of transistors 58 and 59. The emitter electrode of transistor 61 is referenced to ground through a resistor 62 while the base electrode is biased from the above mentioned voltage divider by coupling the base electrode thereof to the junction between resistors 46 and 47.

10 The collector electrode of transistor 59 is also coupled to an external network used for producing the proper phased reference signals for the driver stages prior to demodulation of the chrominance subcarrier signals. The external circuit is the series combination of inductor 66 and resistor 67 shunted by the series capacitors 68 and 69 to obtain the adequate reference signals, each of which is approximately 90° out of phase with one another.

20 These reference signals are applied to the demodulators according to phase to enable the generation of the appropriate color difference signals. As in any demodulator, the axis of demodulation is dependent upon the phase of the reference signal supplied to cause synchronous demodulation. By changing the phase of the reference signals with respect to each other, one can demodulate on a different axis as the I or Q axis and so on.

30 The external network is suitably tapped between capacitors 68 and 69 and at the junction between inductor 66 and resistor 67 to provide two desired signals of a given phase and amplitude. The junction between inductor 66 and resistor 67 is coupled to the base electrode of a transistor 71 via the external coupling capacitor 70. Transistor 71 forms part of a d.c. biasing and a.c. driving circuit for the balanced transistor demodulators which will be described subsequently.

40 Transistor 71 is arranged in an amplifier configuration having its emitter electrode returned to the point of reference potential through resistor 72 which is bypassed for chrominance subcarrier frequencies by external capacitor 73. The collector electrode of transistor 71 is returned to the +V_e supply bus 34 via resistor 75. The collector of transistor 71 is also direct coupled to the base electrode of a transistor 76 arranged in a common collector configuration. The emitter electrode of transistor 76 is coupled to the base electrodes of transistors 71 and 77, respectively via resistors 78 and 79. The resistors 78 and 79 are selected to be approximately of the same magnitude.

50 The emitter electrode of transistor 76 is further returned to the point of reference

potential through a resistor 80 which together with resistors 78 and 79 determines the d.c. split at the respective emitter electrodes of transistors 71 and 77. Transistor 77 is arranged in a common collector configuration having its collector electrode direct coupled to the +V_e supply bus 34 and its emitter electrode returned to ground through a resistor 81.

70 The other phased signal of the reference oscillator taken from the junction between capacitors 68 and 69 is applied to an identical amplifier used for driving another balanced demodulator circuit. The amplifier comprises the amplifier transistor 82, the emitter follower drive and biasing transistor 83 and the common collector stage 84 having its base electrode coupled to the emitter electrode of transistor 83.

80 The output terminals of both the above mentioned demodulator driver circuits correspond respectively to the emitter electrodes of transistors 71 and 77 for the aforementioned stage and to the emitter electrodes of transistors 82 and 84 for the latter mentioned stage. The emitter of transistor 71 is bypassed for signal by the .05 microfarads capacitor 73 and the output signal with respect to the a.c. ground reference at the emitter of transistor 71 is developed across the emitter of transistor 77.

90 The integrated circuit chip utilizes two doubly balanced demodulators 95 and 100 for developing the R-Y and B-Y color difference signals from the chrominance subcarrier components and the suitable phased reference oscillator signals.

100 Chrominance signals from chrominance amplifier 17 (FIGURE 1) are applied to the base electrodes of transistors 91 and 93 with respect to the a.c. ground at the base electrodes of transistors 92 and 94. Transistors 91 and 92 form a differential amplifier with transistor 96 biased as a constant current source. Transistors 93 and 94 form a second differential amplifier configuration with transistor 97 biased as a constant current source.

105 The constant current source transistors 96 and 97 are biased from the amplifier supply configuration including transistor 131 arranged in an emitter follower configuration. Transistor 131 has the emitter electrode returned to ground through a resistor 134 and coupled to the base electrode of transistor 133 arranged in a common emitter configuration. Transistor 133 has the collector electrode direct coupled to the base electrode of transistor 131 and directly coupled to the base electrode of an output emitter follower transistor 132. The emitter electrode of transistor 132 supplies biasing current for the constant current transistors 96 and 97 used in the doubly balanced differential amplifiers.

110 The differential amplifiers provide opposite phased chrominance signals at the collector

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electrodes of transistors 91 and 92, 93, and 94 which are applied to the emitter electrodes of switching transistors controlled by the suitably phased reference oscillator signal. For example, the output emitter electrode of transistor 77 is direct coupled to the base electrode of transistor 98 and transistor 99, utilized as switching transistor in the differential demodulator circuit 95.

The emitter electrode of transistor 71 is coupled to the base electrodes of transistors 101 and 102 which in conjunction with transistors 98 and 99 form the switching transistor network for the differential demodulator 95. Chrominance signals as described previously are applied between the base electrodes of transistors 93 and 94 forming the differential amplifier configuration.

In a similar manner, the demodulator 100 receives a suitable oscillator signal by the coupling of the emitter electrode of transistor 84 to the base electrodes of transistors 104 and 107. The a.c. reference is applied to the base electrodes of the switching transistors 105 and 106 by coupling the bypassed emitter electrode of transistor 82 to the base electrodes of transistor 105 and 106.

A load impedance for the doubly balanced demodulator 95 is obtained by the coupling of the resistors 107' and 108 to the collector electrodes of transistors 102 and 98. The load resistance is shunted by a capacitor 109 which determines the frequency response of the demodulator 95.

In operation, the switch transistors 98, 99, 101, and 102 are controlled by the suitable phased reference oscillator signal to determine which of the chrominance signal currents flows into the load impedance of the differential demodulator 95. The chrominance signals are applied between the base electrodes of transistors 93 and 94 for demodulator 95.

The doubly balanced demodulator configuration provides inherent cancellation of the fundamental reference signal and the chrominance signals thus eliminating the need for additional filtering networks at the output terminal of the demodulator. Demodulator 100, as indicated above, is the same type as demodulator 95 and operates in the same manner, but with a different phased reference oscillator signal to provide the appropriate color difference signal.

By utilizing two demodulators on the integrated circuit chip as shown, two color difference signals are provided. The third signal required is obtained by matrixing the two signals produced in suitable proportions.

Matrixing is provided by resistor 110 coupled between the collector electrode of transistor 101 and the collector electrode of transistor 107 and resistor 111 (2.3K ohms) coupled between the collector electrode of transistor 101 and the base electrode of a transistor 112 used as an input stage for a

matrixed color difference signal output amplifier. The proper ratio of signals for matrixing is determined by the magnitude of resistors 110 and 111 and the impedance between the base electrode of transistor 112 and reference potential.

Each of the generated color difference signals is applied to a suitable amplifier before interfacing with the external environment. Each of the amplifiers (three) comprises a Darlington configuration having a first transistor 112, 113, and 114, respectively.

For example, the collector electrode of transistor 102 is coupled to the base electrode of transistor 113 arranged in a Darlington configuration with the transistor 115. The emitter electrode of transistor 115 is coupled to the base electrode of transistor 116 via a resistor 117. Transistor 116 forms part of a power amplifier with transistor 118, having the collector electrode thereof coupled to the emitter electrode of transistor 116.

To provide a stabilized output impedance over a large dynamic range, transistor 118 has the base electrode thereof biased by coupling the collector electrode of transistor 116 of the base electrode of transistor 118 via a Zener diode 119 in series with the resistor 120 (3K ohms). A further resistor 121 is coupled between the base electrode of transistor 118 and ground to complete the biasing circuit for the power amplifier. The output of the power amplifier is obtained between the emitter electrode of transistor 116 and the collector electrode of transistor 118.

As can be seen from the figure, the demodulator 100 has a similar output driver amplifier as does the matrixed color difference network.

Operation of the Tint Control Network

The constant current source transistor 33 supplies a current to the differential amplifier transistors 30 and 31. Each transistor 30 and 31 is biased quiescently so that they conduct current approximately equal to one another, the sum of both being equal to the reference current supplied by the constant current source transistor 33. Transistor 33 is biased by resistors 44, 45, 46, and 47 connected between the +V_e supply bus 34 and the base electrode of transistor 33, and by diode 55 connected between the base electrode and the point of reference potential. The base current is stabilized by the diode 55 for temperature and voltage variations and is equal to the current flowing through the collector to emitter path of transistor 33, which is approximately:

$$\text{Total } I_{de} = \frac{+V_e - V_{be}}{R_{44} + R_{45} + R_{46} + R_{47}}$$

where

V_e=potential at supply bus 34

V_{be}=voltage drop across diode 55 which is

equal to voltage drop from base to emitter of transistor 33.

With the biasing shown, the quiescent d.c. current in each of the differential transistors 30 and 31 is equal to one-half the value of the total current, I_{ao} .

The reference signal E_s from the oscillator is applied to the base electrode of transistor 30. The currents flowing due to signal E_s , through the collector electrodes of transistors 30 and 31 are equal in magnitude but opposite in phase, due to the differential action.

The collector current flowing through transistor 30 is divided into two current paths, one through the diode-connected transistor 50 and the other through transistor 38. The exact current division is a function of the setting of resistor 51, determining how much of the current is contributed via the diode path and how much through the transistor 38. The a.c. signal current is bypassed at the junction of resistor 51 with the collector and base electrodes of the diode connected transistor 50, by means of capacitor 54.

As indicated, the phase shifted output signal is taken from the collector electrode of transistor 38, and is developed as follows. The voltage developed across the R-C network comprising resistor 36 and capacitor 37 is equal to the transconductance (gm) of the transistor 31 multiplied by the input signal E_s as phase shifted 180 degrees, and the complex impedance comprising resistor 36 and capacitor 37. This voltage is represented by a vector having a phase angle determined by the R-C network forming the complex impedance.

The voltage developed across resistor 41 coupled to the collector electrode of transistor 38, due to the input signal E_s , is approximately equal to the input signal E_s multiplied by the transconductance (gm) of transistor 30 times a factor K (less than one), the whole term multiplied by the magnitude of resistor 41. The factor K is adjusted by resistor 51 as determining the current division between transistor 38 and the diode connected transistor 50.

Since the signal developed across the R-C network, as described above, is applied to the base electrode of transistor 40 whose emitter is coupled to transistor 38 via resistor 41, the output voltage is proportional to the vector sum of the voltage at the base or emitter of transistor 40 and the voltage across the resistor 41.

The output signal is then approximately equal to:

$$E_o = E_1 + E_2$$

where

E_o = Voltage between the collector electrode

of transistor 38 and a point of reference potential

E_1 = Voltage across RC network, resistor 36 and capacitor 37

E_2 = Voltage across resistor 41 $\cong E_s$ (gm) KR

Accordingly:

$$E_o = E_s(gm)(KR - |Z_1|e^{\theta})$$

where:

E_s = signal voltage

gm = transconductance of transistors 30, and 31.

K = current division factor between transistor 38 and transistor connected diode 50.

$|Z|$ = absolute magnitude of impedance of resistor 36 in parallel with capacitor 37

e = natural logarithm

θ = phase angle determined by resistor 36 in parallel with capacitor 37.

R = magnitude of resistor 41

Since the factor K is adjustable according to the setting of potentiometer 51, the phase angle of the output signal E_o is adjustable as being determined by the KR term plus the

$-|Z_1|e^{\theta}$ term; and will vary between the angle θ for K=0 and the angle formed by the complex vector when K=1.

The resultant obtained by adding complex vectors in the above described manner changes slightly in amplitude for changes in phase angle. However, the range of oscillator amplitude or input signal may vary greatly for different types of oscillator configurations. For this reason the output taken from the collector electrode of transistor 38 is coupled to the base electrode of an emitter follower transistor 57, for driving the limiter including transistor 58 and transistor 59. Transistors 58 and 59 as previously described form part of the differential limiter amplifier configuration including the constant current source transistor 61.

This circuit with the signals provided will produce a reliable peak-to-peak amplitude signal for application to the phase determining network comprising inductor 66, resistor 67, in parallel with capacitors 68 and 69 as described above.

As indicated above, the potentiometer 51 determines how the collector current of transistor 30 will be divided into two current paths. One path is through the diode connected transistor 50 and the other path through the transistor 38. It should be noted that this current divider operates as an attenuator circuit for the input signal applied to the base electrode of the transistor 30.

That is, the output signal appearing at the

collector of transistor 38 will be a divided or attenuated version of the input signal applied to the base electrode of the transistor 30. This is clearly controlled by the setting of the potentiometer 51. Note that this current dividing function is independent from the operation of the transistor 31 and the phase shifting network made up of resistor 36 and capacitor 37. Thus, in the absence of the transistor 31 and network 36, 37 the output signal appearing at the collector of transistor 38 would be an attenuated or divided non-phase-shifted version of the input signal applied to transistor 30.

Thus, the above described circuit always provides a current dividing or attenuating function which is also used for phase shifting purposes when the transistor 31 and network 36, 37 are included.

20 Operation of the Drive and Biasing Circuits for the Differential Demodulators

The Drive and Biasing Circuits assure that the switching transistors used in the balanced demodulators are maintained at equal bias levels to provide reliably balanced operation.

The drive amplifier used to supply reference oscillator signals at the proper phase to the switching transistors 98, 99, 101, 102, for example, as utilized in demodulator 95, is a symmetrical circuit employing a negative feedback network capable of developing highly predictable DC potentials, by including a branch network with the DC potential essentially determined by the symmetry of the circuit. Negative feedback is obtained via transistor 71 and transistor 76. Transistor 71 includes a collector load resistor 75 and has its base electrode coupled to the emitter electrode of transistor 76 via resistor 78. The base electrode of transistor 76 is further coupled to the collector electrode of transistor 71 providing the negative feedback. The resistors 72, 75, 80 and 81 provide the necessary stabilization against power supply and temperature variations.

In operation, if the collector voltage of transistor 71 decreases due to the increase in collector current, the decrease in voltage is applied to the base electrode of transistor 76 which tends to reverse bias transistor 76, tending to make the emitter electrode of transistor 76 less positive. This action serves to decrease the base current in transistor 71, thus stabilizing the collector voltage variation.

The increase of current through transistor 71 also serves to increase the voltage across the emitter resistor 72 which also functions to stabilize the bias and therefore the collector voltage of transistor 71. This operation thereby stabilizes the circuit operation against DC supply variations or current variations due to temperature changes. It is also noted that the DC voltage at the emitter electrode of transistor 71 and the DC voltage at the

emitter electrode of transistor 77 are maintained relatively constant and track with each other as both voltages are controlled by the follower transistor 76.

Because of the equal magnitudes of resistors 78 and 79, as coupled to the base electrodes of transistor 71 and 77, and as energized by the connection of the emitter electrodes of transistor 76; the DC currents flowing in the transistors 71 and 77 are virtually identical and track with any variations in voltage or temperature due to the action of transistor 76. Therefore, the bias supplied to the switching transistors 98 and 99 and 101 and 102 is held relatively constant and identical for both temperature and voltage variations.

As far as the AC gain of the amplifier is concerned, the emitter of transistor 71 is bypassed for AC signals by capacitor 73. The AC signal when applied to the base electrode of transistor 71 is amplified by the gain of the stage as determined by the transconductance of the transistor and its collector load resistor 75. This effective gain is available at the emitter of transistor 77 due to the coupling of the base electrode of transistor 77 to the emitter electrode of transistor 76 via resistor 79.

In essence, the full AC signal with the aforementioned gain is applied to transistors 98 and 99 via transistor 77. Due to the operation of the circuit the signal applied to transistors 98 and 99 is referenced back to the emitter of transistor 71 which is at AC ground. Thus the operation and application of the signals is in common to the differential mode operation of a typical differential amplifier assembly. When such an amplifier is driven by a single ended signal, it will provide a push-pull output signal by the emitter couplings as utilized, for example, in the above described arrangements of the differential transistor configurations.

As indicated previously, a similar driving circuit obtaining and utilizing the same properties of symmetry is also used in conjunction with demodulator 100 for supplying the proper bias and phased referenced oscillator signal thereto.

WHAT WE CLAIM IS:—

1. A current dividing circuit for electrical signal currents comprising first and second semiconductor devices each having at least first and second electrodes, the second electrodes of said devices being coupled to a common circuit junction, bias current means coupled to said junction for providing forward bias direct current components to each of said devices, said bias current means including means for establishing a substantially constant quiescent value of bias current through the emitter-collector path of a third semiconductor device in the form of a first transistor having its collector electrode direct current



collector of transistor 33 will be a divided or attenuated version of the input signal applied to the base electrode of the transistor 30. This is clearly controlled by the setting of the potentiometer 51. Note that this current dividing function is independent from the operation of the transistor 31 and the phase shifting network made up of resistor 36 and capacitor 37. Thus, in the absence of the transistor 31 and network 36, 37 the output signal appearing at the collector of transistor 38 would be an attenuated or divided non-phase-shifted version of the input signal applied to transistor 30.

Thus, the above described circuit always provides a current dividing or attenuating function which is also used for phase shifting purposes when the transistor 31 and network 36, 37 are included.

Operation of the Drive and Biasing Circuits for the Differential Demodulators

The Drive and Biasing Circuits assure that the switching transistors used in the balanced demodulators are maintained at equal bias levels to provide reliably balanced operation.

The drive amplifier used to supply reference oscillator signals at the proper phase to the switching transistors 98, 99, 101, 102, for example, as utilized in demodulator 95, is a symmetrical circuit employing a negative feedback network capable of developing highly predictable DC potentials, by including a branch network with the DC potential essentially determined by the symmetry of the circuit. Negative feedback is obtained via transistor 71 and transistor 76. Transistor 71 includes a collector load resistor 75 and has its base electrode coupled to the emitter electrode of transistor 76 via resistor 78. The base electrode of transistor 76 is further coupled to the collector electrode of transistor 71 providing the negative feedback. The resistors 72, 75, 80 and 81 provide the necessary stabilization against power supply and temperature variations.

In operation, if the collector voltage of transistor 71 decreases due to the increase in collector current, the decrease in voltage is applied to the base electrode of transistor 76 which tends to reverse bias transistor 76, tending to make the emitter electrode of transistor 76 less positive. This action serves to decrease the base current in transistor 71, thus stabilizing the collector voltage variation.

The increase of current through transistor 71 also serves to increase the voltage across the emitter resistor 72 which also functions to stabilize the bias and therefore the collector voltage of transistor 71. This operation thereby stabilizes the circuit operation against DC supply variations or current variations due to temperature changes. It is also noted that the DC voltage at the emitter electrode of transistor 71 and the DC voltage at the

emitter electrode of transistor 77 are maintained relatively constant and track with each other as both voltages are controlled by the follower transistor 76.

Because of the equal magnitudes of resistors 78 and 79, as coupled to the base electrodes of transistor 71 and 77, and as energized by the connection of the emitter electrodes of transistor 76; the DC currents flowing in the transistors 71 and 77 are virtually identical and track with any variations in voltage or temperature due to the action of transistor 76. Therefore, the bias supplied to the switching transistors 98 and 99 and 101 and 102 is held relatively constant and identical for both temperature and voltage variations.

As far as the AC gain of the amplifier is concerned, the emitter of transistor 71 is bypassed for AC signals by capacitor 73. The AC signal when applied to the base electrode of transistor 71 is amplified by the gain of the stage as determined by the transconductance of the transistor and its collector load resistor 75. This effective gain is available at the emitter of transistor 77 due to the coupling of the base electrode of transistor 77 to the emitter electrode of transistor 76 via resistor 79.

In essence, the full AC signal with the aforementioned gain is applied to transistors 98 and 99 via transistor 77. Due to the operation of the circuit the signal applied to transistors 98 and 99 is referenced back to the emitter of transistor 71 which is at AC ground. Thus the operation and application of the signals is in common to the differential mode operation of a typical differential amplifier assembly. When such an amplifier is driven by a single ended signal, it will provide a push-pull output signal by the emitter couplings as utilized, for example, in the above described arrangements of the differential transistor configurations.

As indicated previously, a similar driving circuit obtaining and utilizing the same properties of symmetry is also used in conjunction with demodulator 100 for supplying the proper bias and phased referenced oscillator signal thereto.

WHAT WE CLAIM IS:—

1. A current dividing circuit for electrical signal currents comprising first and second semiconductor devices each having at least first and second electrodes, the second electrodes of said devices being coupled to a common circuit junction, bias current means coupled to said junction for providing forward bias direct current components to each of said devices, said bias current means including means for establishing a substantially constant quiescent value of bias current through the emitter-collector path of a third semiconductor device in the form of a first transistor having its collector electrode direct current



coupled to said junction, signal input means coupled to said junction for supplying signal currents to said devices, means coupled to said first electrode of said first device for bypassing signal currents to a point of reference potential, variable impedance means coupled to said first electrode of said first device for supplying a variable control current to said first device so as to vary proportioning of signal currents traversing said first and second devices between said first and second electrodes thereof, and output signal utilization means coupled to said first electrode of said second device for deriving output signals determined by said input signals and said control current.

2. A current dividing circuit as claimed in Claim 1, comprising a fourth semiconductor device in the form of a second transistor having base, collector and emitter electrodes, its emitter electrode being directly coupled to said emitter electrode of said third device and to a source of substantially constant current said signal input means being coupled to the base electrode of said third semiconductor device to provide at said collector electrodes of said third and fourth devices replicas of said input signal of different phase with respect to one another, said first and second devices providing first and second controllable current paths for the signal current supplied to said junction, said signal current as divided between said first and second paths being approximately equal to the total current through said third semiconductor device, means coupling the collector electrode of said fourth device to said second current path for applying said replica of said signal of said different phase thereto, and said output signal utilization means being coupled to said second current path and responsive to said current flowing therethrough for providing a signal having a phase determined in accordance with said current division.

3. A current dividing circuit as claimed in Claim 2, in which said third and fourth devices are first and second transistors respectively arranged in a differential amplifier configuration, with second impedance means coupled to the collector electrode of said second transistor to shift the phase of the signal appearing thereat by a predetermined amount.

4. A current dividing circuit as claimed in Claim 3, in which said second semiconductor device includes a third transistor having a base, collector and emitter electrode, said emitter electrode being coupled to the collector electrode of said first transistor, means for biasing said base electrode of said third transistor, means coupling said collector electrode of said third transistor to a point of operating potential, and means for varying the bias between said base and emitter electrodes of said third transistor and therefore

varying said current through said first path.

5. A current dividing circuit as claimed in Claim 3 or 4, in which said first semiconductor device includes a unidirectional current conducting device having a first and a second terminal and poled to conduct current from said first to said second terminal, said second terminal being coupled to the collector electrode of said third device and said variable impedance means includes a variable resistor coupled between said first terminal of said unidirectional conducting device and a point of operating potential for varying the current conducted by that device according to the variation in magnitude of said resistor.

6. A current dividing circuit as claimed in Claim 4, comprising a fourth transistor having a collector electrode coupled to said emitter electrodes of said first and second transistors and an emitter electrode returned to a point of reference potential, means coupled to the base electrode of said fourth transistor for biasing said fourth transistor to conduct current via its collector to emitter path of a magnitude approximately equal to the current flowing through said collector to emitter paths of said first and second transistors, said second impedance means including a phase shifting network coupled to the collector electrode of said second transistor, and means coupling said phase shifting network to the collector electrode of said third transistor for application of a portion of said phase shifted signal thereto, to cause vectorial addition of said phase shifted signal as applied to said collector electrode and that signal present due to said input signal as applied to the base electrode of said first transistor, thereby to provide a changed phase shifted signal at said collector electrode of said third transistor.

7. A current dividing circuit as claimed in Claim 6, in which said means coupled to the base electrode of said fourth transistor includes a unilateral current conducting device coupled between the base electrode of said fourth transistor and a point of reference potential and poled for easy current conduction in the same direction as said base to emitter junction of said fourth transistor, and a resistor coupled between said base electrode of said fourth transistor and a point of operating potential.

8. A current dividing circuit as claimed in Claim 5 or 6, in which said phase shifting impedance means includes a resistor coupled between said collector of said transistor and said point of operating potential, and a capacitor in parallel with said resistor for providing said given phase shift to said signal appearing at said collector electrode of said third transistor.

9. A current dividing circuit as claimed in Claim 5, in which said unidirectional current conducting device is a transistor having a base, collector and emitter electrode, and having its

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base electrode directly connected to its collector electrode, said collector to base connection being said first electrode and said emitter electrode being said second electrode.

- 5 10. A current dividing circuit as claimed in any one of Claims 1—9, in which all of the recited elements except for said variable impedance means are formed as elements of a monolithic integrated circuit on a common
- 10 substrate.

11. A current dividing circuit substantially

as hereinbefore described in conjunction with the drawings.

12. A circuit according to any of claims 1—11 provided in a hue control circuit arrangement in a color television. 15

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