

Description

The present invention relates to a level conversion circuit, and more particularly to a level conversion circuit for converting a CMOS (Complementary Metal Oxide Semiconductor) level signal to an ECL (Emitter-Coupled Logic) level signal.

Recently, so-called Bi-CMOS circuits have become popular in the semiconductor circuit art. The Bi-CMOS circuits have a combined structure of bipolar device circuits and CMOS device circuits formed together on one single chip. Bipolar circuits such as ECL LSIs (Large Scale Integrated Circuits) typically provide fast circuit speeds, reduced delay per unit load, and have historically been the predominant technology applied in ICs (Integrated Circuits). CMOS circuits provide high noise immunity, high input impedance, and low power consumption, and have rapidly gained acceptance in the industry. Thus Bi-CMOS circuits may have features of both the bipolar circuits and the CMOS circuits.

To use ECL device circuits together with CMOS device circuits, the input-output levels of both circuits must be matched and in particular, an interface circuit for converting a CMOS logic level (high level; power source potential, for example, 5.0 volts, low level; ground potential, i.e., 0 volts) to an ECL logic level (high level; for example, - 0.7 volts, low level; for example, - 2.5 volts) is necessary.

US Patent 4,453,095 discloses various ECL MOS buffer circuits for interfacing CMOS circuitry with associated ECL devices. The circuits adapt from one voltage logic swing to another.

For example, figure 1a of this document shows a circuit for converting an ECL input to a CMOS output. The circuit includes a "current mirror buffer" portion of an input buffer which amplifies the signal output from a level shifter in order to provide a signal which fully swings between the power source collector voltage and the power source emitter voltage. A CMOS output is also provided.

Figure 2B of the latter reference shows an ECL MOS output buffer having a differential amplifier circuit and an output bipolar transistor which outputs an ECL logic level signal from its emitter.

US Patent 4,616,146 discloses a circuit for converting a CMOS logic level to an ECL logic level and comprising a pair of push-pull bipolar transistors, e.g., NPN transistors.

The upper NPN transistor has a collector terminal connected to a first potential source and a source terminal of MOS device, e.g., P-channel MOS transistor (referred as PMOS transistor hereafter), an emitter terminal connected to an output terminal and the collector terminal of the lower bipolar transistor, and a base terminal connected to an input terminal and the gate terminals of the

PMOS transistor and an N-channel MOS transistor (referred as NMOS transistor hereafter) which is connected to the PMOS transistor so that they constitute a CMOS structure. The emitter terminal of the lower NPN transistor is connected to a second potential source and the source terminal of the NMOS transistor, and a base terminal connected to the drain terminals of the PMOS transistor and the NMOS transistor. However, this circuit has a low impedance at the input terminal since the input terminal is connected to the base terminal of the upper NPN transistor, and as the output of the circuit switches from low to high, the lower NPN transistor is slow to turn off causing a slow transition to the high output.

EP-A2-0 167 339 shows, in figures 2, 6 and 23, examples of various known ways to control a differential amplifier circuit.

Thus, what is needed is an IC combining CMOS and bipolar technology having a high input impedance, improved switching characteristics, low power consumption, and high noise immunity.

Accordingly, an object of the present invention is to provide an improved level conversion circuit for converting CMOS level signals to ECL level signals.

Another object of the present invention is to provide a level conversion circuit having improved output signal switching characteristics.

Further object of the present invention is to provide a level conversion circuit having a high input impedance.

Still another object of the present invention is to provide a level conversion circuit having low power consumption.

In order to achieve the above objects, the present invention provides a level conversion circuit for converting a CMOS logic level signal to an ECL logic level signal comprising: a level shift circuit connected between a high potential voltage source and a low potential voltage source, which receives as its input a CMOS logic level signal and a CMOS logic level signal of opposite logic level to the first-mentioned CMOS logic level signal, and which supplies control signals as its output; the level shift circuit including first and second MOS transistors of one conductivity type, third and fourth MOS transistors of another conductivity type and a diode, the gate terminals of the first and second MOS transistors respectively being connected to the non-inverse side and the inverse side of input signal receiving means for receiving said input signals of the circuit, the third and fourth MOS transistors having respective gate terminals connected to each other and to the drain terminal of the third MOS transistor and respectively connected between the high potential source and the low potential source through respectively the first and sec-

ond MOS transistors, with the diode being connected between a first intermediate potential source and the drain of the fourth MOS transistor; a differential amplifier circuit comprising a pair of bipolar transistors and connected between a second intermediate potential voltage source and the low potential voltage source said differential amplifier selecting current flow path between the second intermediate potential voltage source and the low potential voltage source under the control of the bipolar transistors whose emitter terminals are mutually connected together and whose conduction is each controlled by a respective one of said control signals which are supplied to the base terminals thereof such that said bipolar transistors are in opposite states of conduction; and an output bipolar transistor the conduction of which is controlled by one of the collector potentials of said bipolar transistors and which outputs an ECL logic level signal from its emitter terminal.

An embodiment of the invention will now be described in more detail, by way of example only and with reference to the accompanying drawings, in which :-

Figure 1 is a schematic circuit diagram of a level conversion circuit according to the present invention; and

Figure 2 is a level diagram showing level conversion operation of the circuit shown in Figure 1.

The present invention will now be described in detail with reference to the accompanying drawings, namely, Figures 1 and 2.

Referring now to Figure 1, an embodiment of the level conversion circuit according to the present invention will be described. Figure 1 is a circuit diagram showing an embodiment of level conversion circuit according to the present invention. The level conversion circuit includes a level shift circuit 10 of which output level shifts between two levels in response to an input CMOS level signal, a differential circuit 12 of which two current paths selectively become conductive in response to the output level of the level shift circuit 10, and a bipolar transistor 14 whose conductivity is controlled by the differential circuit 12 and outputs an ECL level signal corresponding to the input CMOS level signal.

The level shift circuit 10 is provided with a first and a second PMOS transistors 16 and 18, a first and a second NMOS transistors 20 and 22, and a diode 24. The first PMOS transistor 16 has a gate terminal connected to a non-inverse input terminal INa, a source terminal connected to a first potential source 26 which supplies a first potential Vdd of, e.g., 5 volts, and a drain terminal connected to a drain terminal of the first NMOS transistor 20. The second PMOS transistor 18 has a gate terminal

connected to an inverse input terminal INb, a source terminal connected to the Vdd potential source 26, and a drain terminal connected to a drain terminal of the second NMOS transistor 22.

The anode terminal of diode 24 is connected to the drain terminal of the second PMOS transistor 18 and its cathode terminal is connected to a second potential source 28 which supplies a second potential Vcl of, e.g., - 1.5 volts. The respective gate terminals of the first and second NMOS transistors 20 and 22 are connected together and also connected to the drain terminal of the first NMOS transistor 20, and their respective source terminals are connected to a third potential source 30 which supplies a third potential Vee of, e.g., - 3.0 volts.

The differential circuit 12 is provided with a first and a second NPN transistors 32 and 34, a resistor 36 with a resistance R1, and a current source 38. The first NPN transistor 32 has a base terminal connected to the drain terminal of the second PMOS transistor 18, a collector terminal connected to a ground terminal G through the resistor 36, and an emitter terminal connected to the Vee potential source 30 through the current source 38. The second NPN transistor 34 has a base terminal connected to the connection node of the gate terminals of the first and second NMOS transistors 20 and 22 and the drain terminal of the first PMOS transistor 16, a collector terminal connected to the ground terminal G, and an emitter terminal connected to the Vee potential source 30 through the current source 38 together with the emitter terminal of the first NPN transistor 32.

The bipolar transistor 14 is a third NPN transistor and the third NPN transistor 14 has a base terminal connected to the collector terminal of the first NPN transistor 32, a collector terminal connected to the ground terminal G, and the emitter terminal is connected to the output terminal OUT. The output terminal OUT is used to be connected to a fourth potential source 40 which supplies a fourth potential Vb of, e.g., - 2.0 volts through a load circuit 42, i.e., an ECL device circuit. In Figure 1, the load circuit, i.e., an ECL device circuit is shown as a form of resistor with a resistance R2 of about 50 ohms.

The operation of the embodiment of the level conversion circuit according to the present invention will now be described.

CMOS logic signals are applied across the input terminals INa and INb of the level conversion circuit. First, here will be described a case that a high level CMOS logic signal is applied to the input terminals INa and INb. Hereafter, it is assumed that when the high level CMOS logic signal is applied to the input terminals INa and INb, the high level 5.0 volts of CMOS logic signals is applied to the non-inverse input terminal INa, while the low level 0

volts of CMOS logic signals which is the inverse level of the high level of CMOS logic signals is applied to the inverse input terminal INb.

The first PMOS transistor 16 is then rendered non-conductive. In this state, the first NMOS transistor 20 acts as a relatively small resistance, since its gate and drain terminals are connected together. Thus the potential on the drain terminal of the first NMOS transistor 20 coincides with the potential of the Vee potential source 30, i.e., - 3.0 volts. On the other hand, the second PMOS transistor 18 is rendered conductive. Thus, a current flows from the Vdd potential source 26 to the Vcl potential source 28 through the second PMOS transistor 18 and the diode 24. As a result, the anode potential of the diode 24 becomes a potential which is higher than the Vcl potential, i.e., 1.5 volts by the forward voltage of diodes, e.g., 0.7 volts. As a result, the anode potential of the diode 24 becomes to about - 0.8 volts (i.e., - 1.5 volts + 0.7 volts).

The first NPN transistor 32 of the differential circuit 12 is therefore supplied at its base terminal with the potential - 0.8 volts on the anode of the diode 24. Thus, the first NPN transistor 32 is rendered conductive but operates in the unsaturated region. The second NPN transistor 34 of the differential circuit 12 is supplied at its base terminal with the potential 3.0 volts on the drain terminal of the first NMOS transistor 20. Thus the second NPN transistor 34 is rendered non-conductive. As a result, the current I of the current source 38 flows through a current path including the resistor 36 and the first NPN transistor 32, from the ground terminal G to the Vee potential source 30. If the resistance R1 of the resistor 36 is set to 300 ohms and the current I of the current source 38 is set to about 3 mA, the collector potential of the first NPN transistor 32 is then set to about - 0.9 volts (i.e., 300 ohms x 3 mA). The collector potential - 0.9 volts is applied to the base terminal of the third NPN transistor 14. Therefore, the third NPN transistor 14 becomes conductive and passes a current therethrough from the ground terminal G to the load circuit 42 connected to the output terminal OUT. As a result, the emitter potential of third NPN transistor 14, i.e., the level of the output terminal OUT becomes lower than the base potential of the third NPN transistor 14, which is set to the collector potential - 0.9 volts as mentioned above, by the forward base to emitter voltage drop, usually 0.9 volts of the third NPN transistor 14. Thus the potential level of about - 1.8 volts is obtained at the output terminal OUT.

Consequently, when high level CMOS logic signals are applied between the input terminals INa and INb, low level ECL logic signals are obtained on the output terminal OUT.

Next, there will be described another case that a low level CMOS logic signal is applied to the input terminals INa and INb. The first PMOS transistor 16 has then applied to its gate terminal, the low level 0 volts of CMOS logic signals and is rendered conductive. In this state, the first NMOS transistor 20 also is rendered conductive. The first PMOS transistor 16 and the first NMOS transistor 20 are set so that they have respective resistances at a ratio of 5 : 3 to each other in the conductive state. The ratio is set in corresponding to the ratio of the absolute values of the Vdd potential, i.e., 5.0 volts and the Vee potential, i.e., 3.0 volts. According to the resistance ratio, the potential on the connection node between the first PMOS and NMOS transistors 16 and 20, i.e., the potential on their drain terminals, becomes 0 volts.

On the other hand, the second PMOS transistor 18 has applied to its gate terminal with the high level 5.0 volts of CMOS logic signals and is rendered non-conductive. However, the second NMOS transistor 22 is rendered conductive, since its gate has applied to it the potential 0 volts on the drains terminals of the first PMOS and NMOS transistors 16 and 20. Therefore, the drain potential of the second NMOS transistor 22 becomes 3.0 volts.

The first NPN transistor 32 of the differential circuit 12 is therefore supplied at its base terminal with the potential - 3.0 volts on the drain terminal of the second NMOS transistor 22. Thus the first NPN transistor 32 is rendered non-conductive. The second NPN transistor 34 of the differential circuit 12 is supplied at its base terminal with the potential 0 volts on the drain terminals of the first PMOS and NMOS transistors 16 and 20. Thus the second NPN transistor 34 is rendered conductive. The current I of the current source 38 then flows through another current path including the second NPN transistor 34, from the ground terminal G to the Vee potential source 30. In this condition, the base terminal of the third NPN transistor 14 has applied to it the potential 0 volts on the ground terminal G so that the third NPN transistor 14 is rendered non-conductive. As a result, the emitter potential of third NPN transistor 14, i.e., the level of the output terminal OUT becomes lower than the base potential of the third NPN transistor 14, which is set to the collector potential 0 volts as mentioned above, by the forward base to emitter voltage drop 0.9 volts of the third NPN transistor 14. Thus the potential level of about - 0.9 volts is obtained at the output terminal OUT.

Consequently, when low level CMOS logic signals are applied between the input terminals INa and INb, high level ECL logic signals are obtained on the output terminal OUT.

Figure 2 shows the level conversion characteristics of the embodiment. In Figure 2, the solid line

is a simulation graph of the input CMOS logic level signal and the broken line is a simulation graph of the output ECL logic level signal. As seen from Figure 2, the output ECL logic level signal has a delay time Td1 of about 1.2 nsec. (nano second) when the input CMOS logic level signal changes from the high level state to the low level state and a delay time Td2 of about 1.6 nsec. when the input CMOS logic level signal changes from the low level state to the high level state. In the above, the delay times are measured by the periods between the times the respective signals are at 50% of their amplitudes. On the other hand, in the example of conventional level conversion circuits described above, the delay times Td1 and Td2 were 1.7 nsec. and 2.3 nsec., respectively.

From the foregoing detailed description, it can thus be seen that the present invention provides a level conversion circuit to perform the level conversion of the CMOS logic level signals into the ECL logic level signals. The level conversion circuit of the present invention has the features of improved circuit speed, low power consumption and high input impedance.

While there has been illustrated and described what are at present to be preferred embodiment of the present invention, it will be understood by those skilled in the art various changes and modifications may be made.

Therefore, it is intended that this invention not be limited to the particular embodiment disclosed as the best mode contemplated for carrying out this invention, but that the invention will include all embodiments following within the scope the appended claims.

Claims

1. A level conversion circuit for converting a CMOS logic level signal to an ECL logic level signal comprising:

a level shift circuit (10) connected between a high potential voltage source (26) and a low potential voltage source (30), which receives as its input a CMOS logic level signal and a CMOS logic level signal of opposite logic level to the first-mentioned CMOS logic level signal, and which supplies control signals as its output; the level shift circuit (10) including first and second MOS transistors (16, 18) of one conductivity type, third and fourth MOS transistors (20, 22) of another conductivity type and a diode (24), the gate terminals of the first and second MOS transistors (16, 18) respectively being connected to the non-inverse side and the inverse side of input signal receiving means (INa, INb) for receiving said input signals (10), the third and fourth MOS transistors

(20, 22) having respective gate terminals connected to each other and to the drain terminal of the third MOS transistor (20) and respectively connected between the high potential source (26) and the low potential source (30) through respectively the first and second MOS transistors (16, 18), with the diode (24) being connected between a first intermediate potential source (28) and the drain of the fourth MOS transistor (22);

a differential amplifier circuit (12) comprising a pair of bipolar transistors (32, 34) and connected between a second intermediate potential voltage source (G) and the low-potential voltage source (30) said differential amplifier selecting the current flow path between the second intermediate potential voltage source (G) and the low potential voltage source (30) under the control of the bipolar transistors (32, 34) whose emitter terminals are mutually connected together and whose conduction is each controlled by a respective one of said control signals which are supplied to the base terminals thereof such that said bipolar transistors (32,34) are in opposite states of conduction; and

an output bipolar transistor (14) the conduction of which is controlled by one of the collector potentials of said bipolar transistors (32, 34) and which outputs an ECL logic level signal from its emitter terminal.

2. A level conversion circuit as claimed in claim 1,

wherein the second intermediate potential voltage source is ground (G), and

the output bipolar transistor (14) is connected between the ground potential source (G) and an output terminal (OUT).

3. A level conversion circuit as claimed in claim 2, wherein the differential circuit (12) includes a resistor (36) and a current source (38), one of the bipolar transistors (32) of the differential amplifier (12) having its collector connected to the ground potential source (G) through the resistor (36), its emitter connected to the low potential source (30) via said current source (38) and its base connected to the drain terminal of the fourth MOS transistor (22), and the second bipolar transistor (34) of the pair having its collector connected to the ground potential source (G), its emitter connected to the low potential source (30) together with the emitter of the first bipolar transistor (32) via said current source (38) and its base connected to the drain terminal of the third MOS transistor (20), with the output bipolar transistor (14) having its

is a simulation graph of the input CMOS logic level signal and the broken line is a simulation graph of the output ECL logic level signal. As seen from Figure 2, the output ECL logic level signal has a delay time Td1 of about 1.2 nsec. (nano second) when the input CMOS logic level signal changes from the high level state to the low level state and a delay time Td2 of about 1.6 nsec. when the input CMOS logic level signal changes from the low level state to the high level state. In the above, the delay times are measured by the periods between the times the respective signals are at 50% of their amplitudes. On the other hand, in the example of conventional level conversion circuits described above, the delay times Td1 and Td2 were 1.7 nsec. and 2.3 nsec., respectively.

From the foregoing detailed description, it can thus be seen that the present invention provides a level conversion circuit to perform the level conversion of the CMOS logic level signals into the ECL logic level signals. The level conversion circuit of the present invention has the features of improved circuit speed, low power consumption and high input impedance.

While there has been illustrated and described what are at present to be preferred embodiment of the present invention, it will be understood by those skilled in the art various changes and modifications may be made.

Therefore, it is intended that this invention not be limited to the particular embodiment disclosed as the best mode contemplated for carrying out this invention, but that the invention will include all embodiments following within the scope the appended claims.

Claims

1. A level conversion circuit for converting a CMOS logic level signal to an ECL logic level signal comprising:

a level shift circuit (10) connected between a high potential voltage source (26) and a low potential voltage source (30), which receives as its input a CMOS logic level signal and a CMOS logic level signal of opposite logic level to the first-mentioned CMOS logic level signal, and which supplies control signals as its output; the level shift circuit (10) including first and second MOS transistors (16, 18) of one conductivity type, third and fourth MOS transistors (20, 22) of another conductivity type and a diode (24), the gate terminals of the first and second MOS transistors (16, 18) respectively being connected to the non-inverse side and the inverse side of input signal receiving means (INa, INb) for receiving said input signals (10), the third and fourth MOS transistors

(20, 22) having respective gate terminals connected to each other and to the drain terminal of the third MOS transistor (20) and respectively connected between the high potential source (26) and the low potential source (30) through respectively the first and second MOS transistors (16, 18), with the diode (24) being connected between a first intermediate potential source (28) and the drain of the fourth MOS transistor (22);

a differential amplifier circuit (12) comprising a pair of bipolar transistors (32, 34) and connected between a second intermediate potential voltage source (G) and the low-potential voltage source (30) said differential amplifier selecting the current flow path between the second intermediate potential voltage source (G) and the low potential voltage source (30) under the control of the bipolar transistors (32, 34) whose emitter terminals are mutually connected together and whose conduction is each controlled by a respective one of said control signals which are supplied to the base terminals thereof such that said bipolar transistors (32,34) are in opposite states of conduction; and

an output bipolar transistor (14) the conduction of which is controlled by one of the collector potentials of said bipolar transistors (32, 34) and which outputs an ECL logic level signal from its emitter terminal.

2. A level conversion circuit as claimed in claim 1,

wherein the second intermediate potential voltage source is ground (G), and

the output bipolar transistor (14) is connected between the ground potential source (G) and an output terminal (OUT).

3. A level conversion circuit as claimed in claim 2, wherein the differential circuit (12) includes a resistor (36) and a current source (38), one of the bipolar transistors (32) of the differential amplifier (12) having its collector connected to the ground potential source (G) through the resistor (36), its emitter connected to the low potential source (30) via said current source (38) and its base connected to the drain terminal of the fourth MOS transistor (22), and the second bipolar transistor (34) of the pair having its collector connected to the ground potential source (G), its emitter connected to the low potential source (30) together with the emitter of the first bipolar transistor (32) via said current source (38) and its base connected to the drain terminal of the third MOS transistor (20), with the output bipolar transistor (14) having its



collector terminal connected to the ground potential source (G), its emitter terminal connected to the output terminal and its base terminal connected to the collector terminal of the first bipolar transistor (32).

Patentansprüche

1. Pegelumwandlungsschaltung zum Umwandeln eines CMOS-Logikpegel-Signals in ein ECL-Logikpegel-Signal, die aufweist:

- eine zwischen einer Hochpotential-Spannungsquelle (26) und einer Niederpotential-Spannungsquelle (30) angeschlossene Pegelschiebeschaltung (10), die an ihrem Eingang ein CMOS-Logikpegel-Signal und ein zu diesem CMOS-Logikpegel-Signal entgegengesetztes-CMOS-Logikpegel-Signal erhält, und an ihrem Ausgang Steuersignale ausgibt; wobei die Pegelschiebeschaltung (10) einen ersten und zweiten MOS-Transistor (16, 18) eines Leitungstyps, einen dritten und vierten MOS-Transistor (20, 22) eines anderen Leitungstyps, und eine Diode (24) umfaßt, und wobei die Gate-Anschlüsse des ersten und zweiten MOS-Transistors (16, 18) an die nicht-inverse Seite bzw. die inverse Seite des Eingangssignal-Empfangsmittels (INa, INb) angeschlossen sind, um diese Eingangssignale zu erhalten, und die Gate-Anschlüsse des dritten und vierten MOS-Transistors (20, 22) miteinander und mit dem Drain-Anschluß des dritten MOS-Transistors (20) verbunden sind, und der dritte und vierte MOS-Transistor (20, 22) über den ersten und zweiten MOS-Transistor (16, 18) zwischen der Hochpotential-Quelle (26) und der Niederpotential-Quelle (30) angeschlossen sind, und die Diode (24) zwischen einer ersten Zwischenpotential-Quelle (28) und dem Drain-Anschluß des vierten MOS-Transistors (22) angeschlossen ist;
- eine Differentialverstärkerschaltung (12) mit zwei bipolaren Transistoren (32, 34), die zwischen einer zweiten Zwischenpotential-Spannungsquelle (G) und der Niederpotential-Spannungsquelle (30) angeschlossen ist, wobei der Differentialverstärker den Stromweg zwischen der zweiten Zwischenpotential-Spannungsquelle (G) und der Niederpotential-Spannungsquelle (30) aussucht, bei Steuerung durch die bipolaren Transistoren (32, 34), deren Emitteranschlüsse

miteinander verbunden sind, und deren Leitung durch eines der auf ihre Basis-Anschlüsse gegebenen Steuersignale so gesteuert wird, daß die bipolaren Transistoren (32, 34) in entgegengesetzten Leitungszuständen sind; und

- einen bipolaren Ausgangstransistor (14), dessen Leitung durch eines der Kollektorpotentiale der bipolaren Transistoren (32, 34) gesteuert wird, und der an seinem Emitter-Anschluß ein ECL-Logikpegel-Signal ausgibt.

2. Pegelumwandlungsschaltung gemäß Anspruch 1, wobei die zweite Zwischenpotential-Spannungsquelle die Erde (G) ist, und der bipolare Ausgangstransistor (14) zwischen der Erdpotential-Quelle (G) und einer Ausgangsklemme (OUT) angeschlossen ist.

3. Pegelumwandlungsschaltung gemäß Anspruch 2, wobei die Differentialverstärkerschaltung (12) einen Widerstand (36) und eine Stromquelle (38) umfaßt, und bei einem der bipolaren Transistoren (32) des Differentialverstärkers (12) der Kollektor über den Widerstand (36) mit der Erdpotential-Quelle (G) verbunden ist, der Emitter über die Stromquelle (38) mit der Niederpotential-Quelle (30) verbunden ist, und die Basis mit dem Drain-Anschluß des vierten MOS-Transistors (22) verbunden ist, und bei dem zweiten bipolaren Transistor (34) der Kollektor mit der Erdpotential-Quelle (G) verbunden ist, der Emitter, zusammen mit dem Emitter des ersten bipolaren Transistors (32), über die Stromquelle (38) mit der Niederpotential-Quelle (30) verbunden ist, und die Basis mit dem Drain-Anschluß des dritten MOS-Transistors (20) verbunden ist, und wobei bei dem bipolaren Ausgangstransistor (14) der Kollektor-Anschluß mit der Erdpotential-Quelle (G) verbunden ist, der Emitter-Anschluß mit der Ausgangsklemme verbunden ist, und der Basis-Anschluß mit dem Kollektor-Anschluß des ersten bipolaren Transistors (32) verbunden ist.

Revendications

1. Circuit de conversion de niveau pour convertir un signal de niveau logique CMOS en un signal de niveau logique ECL, comprenant:
 - un circuit de décalage de niveau (10) connecté entre une source de tension de potentiel haut (26) et une source de tension de potentiel bas (30), lequel reçoit au niveau de son entrée un signal de niveau logique CMOS et un signal de niveau logique CMOS d'un



niveau logique opposé au signal de niveau logique CMOS mentionné en premier et fournit des signaux de commande au niveau de sa sortie; le circuit de décalage de niveau (10) incluant des premier et second transistors MOS (16, 18) d'un type de conductivité, des troisième et quatrième transistors MOS (20, 22) d'un autre type de conductivité et une diode (24), les bornes de grille des premier et second transistors MOS (16, 18) étant respectivement connectées au côté de non inversion et au côté d'inversion d'un moyen de réception de signal d'entrée (INa, INb) pour recevoir lesdits signaux d'entrée, les troisième et quatrième transistors MOS (20, 22) comportant des bornes de grille respectives connectées l'une à l'autre ainsi qu'à la borne de drain du troisième transistor MOS (20) et respectivement connectées entre la source de potentiel haut (26) et la source de potentiel bas (30) au travers respectivement des premier et second transistors MOS (16, 18), la diode (24) étant connectée entre une première source de potentiel intermédiaire (28) et le drain du quatrième transistor MOS (22);

un circuit amplificateur différentiel (12) comprenant une paire de transistors bipolaires (32, 34) et connecté entre une seconde source de tension de potentiel intermédiaire (G) et la source de tension de potentiel bas (30), ledit amplificateur différentiel sélectionnant la voie de circulation de courant entre la seconde source de tension de potentiel intermédiaire (G) et la source de tension de potentiel bas (30) sous la commande des transistors bipolaires (32, 34) dont des bornes d'émetteur sont mutuellement connectées ensemble et dont une conduction est commandée pour chacun par l'un respectif desdits signaux de commande qui sont appliqués à leurs bornes de base de telle sorte que lesdits transistors bipolaires (32, 34) soient dans des états de conduction opposés; et

un transistor bipolaire de sortie (14) dont la conduction est commandée par l'un des potentiels de collecteur desdits transistors bipolaires (32, 34) et qui émet en sortie un signal de niveau logique ECL depuis sa borne d'émetteur;

2. Circuit de conversion de niveau selon la revendication 1, dans lequel la seconde source de tension de potentiel intermédiaire est reliée à la masse (G); et

le transistor bipolaire de sortie (14) est connecté entre la source de potentiel de masse (G) et une borne de sortie (OUT).

3. Circuit de conversion de niveau selon la revendication 2, dans lequel le circuit différentiel (12) inclut une résistance (36) et une source de courant (38), l'un des transistors bipolaires (32) de l'amplificateur différentiel (12) ayant son collecteur connecté à la source de potentiel de masse (G) au travers de la résistance (36), son émetteur connecté à la source de potentiel bas (30) via ladite source de courant (38) et sa base connectée à la borne de drain du quatrième transistor MOS (22), et le second transistor bipolaire (34) de la paire de transistors ayant son collecteur connecté à la source de potentiel de masse (G), son émetteur connecté à la source de potentiel bas (30) avec l'émetteur du premier transistor bipolaire (32) via ladite source de courant (38) et sa base connectée à la borne de drain du troisième transistor MOS (20), le transistor bipolaire de sortie (14) ayant sa borne de collecteur connectée à la source de potentiel de masse (G), sa borne d'émetteur connectée à la borne de sortie et sa borne de base connectée à la borne de collecteur du premier transistor bipolaire (32).

