

Description

The invention relates to a digital-to-analog converter for converting a digital signal having a word length n into an analog signal, comprising

- a series arrangement of at least a first and a second integrating circuit each having an input and an output and a control signal input, the input of the first integrating circuit being adapted to receive a reference voltage, the output of the first integrating circuit being coupled to the input of the second integrating circuit, the output of the last integrating circuit in the series arrangement being coupled to the output of the digital-to-analog converter, each of the (first and second) integrating circuits comprising a first and a second amplifier stage, respectively, having an inverting and a non-inverting input and an output and a first and a second capacitor, respectively, coupled between the inverting input and the output of the first and the second amplifier stage, respectively, the first and the second integrating circuit being adapted to perform an integration step under the influence of a control signal applied to the control signal input,
- a control unit having an input, and at least a first and a second output coupled to the control signal input of the first and the second integrating circuit, respectively, the input of the control unit being adapted to receive n bits digital signals for conversion, wherein for converting the n bit digital signal, said control unit is adapted to generate in response to the n bit digital signal applied to its input, in this order, a first control signal at its first output, a second control signal at its second output, a third control signal at its first output and a fourth control signal at its second output.

A converter of this type is known from the published Japanese Patent Application (kokai) no. 59-8427 and is intended to convert an n -bit digital signal. The integrating circuits in the known converter are in the form of analog integrators.

The known converter is intended to convert 16-bit digital signals into analog signals and it operates as follows. Under the influence of the first control signal the first integrating circuit performs $M1$ times an integration step so that a first value is derived which is proportional to $2^8 V_{ref}$, in which V_{ref} is a reference value. Subsequently the second integrating circuit is activated $M2$ times by the second control signal so that an analog signal, which is proportional to $MSB \cdot 2^8 V_{ref}$, is produced at the output of the second circuit, in which MSB is equal to the value of the binary number of the eight most significant bits of the 16-bit digital signal.

Subsequently the output of the first integrating circuit is brought to an initial level (reset to zero in this case) under the influence of a reset signal of the control unit. Subsequently the first circuit performs $M3$ integration steps under the influence of the third control signal so that a value proportional to V_{ref} is derived. The second circuit is then activated $M4$ times by the fourth control signal. An analog output signal is now produced which is proportional to $(MSB \cdot 2^8 + LSB) V_{ref}$ in which LSB is equal to the value of the binary number of the eight least significant bits of the 16-bit digital signal. The known converter appears to have a disturbing offset component in the analog output signal.

It is an object of the invention to provide a digital-to-analog converter which does not have (substantially) any disturbing offset component in the analog output signal. The digital-to-analog converter according to the invention is therefore characterized in that the integrators are switched capacitor integrators and in that a first capacitor network comprising at least two capacitors is coupled between the input of the first integrator and the inverting input of the first amplifier stage, a second capacitor network comprising at least two capacitors being coupled between the input of the second integrator and the inverting input of the second amplifier stage, the first capacitor network being adapted to couple during a given time interval a total capacitance of $M1 \cdot C_{ref1}$ and $M3 \cdot C_{ref1}$ to the inverting input of the first amplifier stage under the influence of the first and the third control signal, respectively, the second capacitor network being adapted to couple during a given time interval a total capacitance of $M2 \cdot C_{ref2}$ and $M4 \cdot C_{ref2}$ to the inverting input of the second amplifier stage under the influence of the second and the fourth control signal, respectively, C_{ref1} and C_{ref2} being fixed capacitances, and in that for converting arbitrary digital signals having a word length n it holds that $M2 + M4$ is equal to a constant (k). For converting an n -bit digital signal the constant (k) is preferably chosen to be equal to 2^p in which $p \leq n$.

Thus, the invention can also be used in digital-to-analog converters for converting digital signals having a word length n which may be associated with numerical systems other than the binary system. For example, ternary or quaternary numerical systems are feasible.

The invention is based on the following recognition. The known converter appears to generate an offset at its output which is signal-dependent. This means that the offset for different values of the n -bit digital signal has a different magnitude. It can be calculated that the offset at the output of the converter, in so far as it results from an offset V_o at the output of the first integrating circuit, is equal to

$(MSB + LSB) \cdot V_0$

This means, for example, for a 16-bit digital signal for which it holds that $MSB = 0$ and $LSB = 255$ (decimal), that the offset is equal to $255 V_0$. However, for the 16-bit digital signal which is larger by the value of 1, i.e. $MSB = 1$ and $LSB = 0$, this means that the offset is equal to V_0 .

The measure according to the invention is based on the recognition that the two integrating circuits are controlled in such a way that a signal-independent offset is generated at the output of the converter. This means that an offset voltage is produced at the output of the converter but the magnitude of this offset voltage is independent of the value of the digital signal. For this fixed offset voltage, whose magnitude can of course be determined in a simple manner, a compensation, if required, can be easily realized at a later stage. Since the second integrating circuit according to the invention initially receives the second and then the fourth control signal, whilst firstly a total capacitance of $M2 \cdot C_{ref2}$ and then a total capacitance of $M4 \cdot C_{ref2}$ is coupled to the inverting input of the second amplifier stage, and in which $M2 + M4$ is equal to a constant k , an offset voltage which is proportional to $(M2 + M4) \cdot V_0$, i.e. equal to $k \cdot V_0$, is generated at the output of the converter. The offset voltage thus has a given constant value, irrespective of the signal to be converted.

The digital-to-analog converter may be further characterized in that $M3 = 1$, in that $M4$ is the value corresponding to the binary number formed by the p least significant bits of the n -bit digital signal and in that $M1$ is the value corresponding to the binary number formed by the $n-p$ most significant bits of the n -bit digital signal. In contrast to the control in the known converter in which the first integrating circuit generates a fixed value (namely the aforementioned first and second value) and in which only the second integrating circuit is controlled by control signals derived from the value of the n -bit digital signal, signals which are dependent on the value of the digital signal to be converted in all four integration steps are derived in both the first and the second integrating circuit in the converter according to the invention. Thus, it holds for the first integration step that $M1$ is equal to the previously mentioned value MSB , $M2 = k - M4$ for the second integration step, $M3 = 1$ for the third integration step (which means that after two integration steps in the first integrator an output signal is present at its output which is equal to $(M1 + 1) \cdot V_{ref}$, i.e. $(MSB + 1) \cdot V_{ref}$, which signal is thus also dependent on the value of the n -bit digital signal), and $M4$ is equal to the previously mentioned value LSB for the fourth integration step.

The digital-to-analog converter may be further characterized in that a third switched capacitor integrator comprising a third amplifier stage, a third capacitor coupled between an inverting input and an output of this amplifier stage and a third capacitor network comprising at least two capacitors coupled between an input of the third integrator and the inverting input of the amplifier stage is arranged in series with the second switched capacitor integrator, said third integrator being adapted to perform an integration step under the influence of a control signal at a control signal input of said integrator, the control unit being adapted to generate in response to the n bit digital signal applied to its input a reset signal for bringing the signal at the output of the first integrator to an initial level and for subsequently generating a fifth control signal to be applied to a first output, the control unit being further adapted to generate, in this order, a sixth control signal and an eighth control signal to be applied to a third output which is coupled to the control signal input of the third integrator and being adapted to generate, after the sixth control signal and before the eighth control signal, a seventh control signal to be applied to the second output, the first capacitor network being further adapted to couple during a given time interval a total capacitance of $M5 \cdot C_{ref1}$ to the inverting input of the first amplifier stage under the influence of the fifth control signal, the third capacitor network being adapted to couple during a given time interval a total capacitance of $M6 \cdot C_{ref3}$ and $M8 \cdot C_{ref3}$ to the inverting input of the third amplifier stage under the influence of the sixth and the eighth control signal, respectively, the second capacitor network being adapted to couple during a given time interval a total capacitance of $M7 \cdot C_{ref2}$ to the inverting input of the second amplifier stage under the influence of the seventh control signal, C_{ref3} being a fixed capacitance. If for converting arbitrary n -bit digital signals it holds that $M6 + M8$ is equal to a constant (k'), for example equal to 2^q in which $p + q \leq n$, an offset is produced at the output of the converter, which offset is also more or less constant and more or less independent of the value of the digital signal.

It is of course evident that the converter according to the invention may be further extended by arranging at least a fourth integrator in series with the third integrator.

For converting an n -bit digital signal the digital-to-analog converter may be further characterized in that $M3 = M5 = M7 = 1$, in that $M8$ is the value corresponding to the binary number constituted by the q least significant bits of the n -bit digital signal, $M1$ is the value corresponding to the binary number constituted by the $n-p-q$ most significant bits and $M4$ is the value corresponding to the binary num-

ber constituted by the remaining p bits of the n -bit digital signal. The n -bit digital signal to be converted has now been split up into three parts, namely the $n-p-q$ most significant bits constituting the (decimal) number $M1$ or MSB, the q least significant bits constituting the (decimal) number $M8$ or LSB and the remaining p bits constituting the (decimal) number $M4$ or ISB. The first four integration steps in the first and the second integrator are equal to those in the previously described embodiment, with the difference that $M1$ now corresponds to the $n-p-q$ most significant bits and $M2=k\text{-ISB}$ and $M4=\text{ISB}$. It may be clear that the sixth integration step, which is performed by the third integrator, can be performed at any moment after the fourth integration step, which is performed by the second integrator. It is clear that in the sixth and the eighth integration step performed by the third integrator a total capacitance of $k \cdot C_{ref3}$ is coupled to the inverting input of the third amplifier stage, which capacitance is constant for an arbitrary digital signal.

In the two-stage design of the converter p is preferably equal to $n/2$ if n is even. In the three-stage version it preferably holds that $p = q = n/3$ if n is divisible by 3. In these cases the total capacitance in the capacitor networks is lowest so that the required surface area in the IC for the capacitors is also smallest.

To be able to reset to an initial output level a parallel arrangement of another switching element and the capacitor may be coupled between the inverting input and the output of the first integrating circuit, the other switching element having a control signal input for receiving the reset signal.

The capacitor networks may be constructed in different manners. One possibility is to provide a capacitor network with capacitors having a substantially equal capacitance. Another possibility is for successive capacitors in a capacitor network to have a capacitance which is eachtime a factor of 2 larger. The first-mentioned possibility is more advantageous because the spread in the capacitors may be lower in this case.

The influence of the spread on the output signal of the converter may be further suppressed by constituting the total capacitances $M2 \cdot C_{ref2}$ and $M4 \cdot C_{ref2}$ by parts in the second capacitor network which are complementary with respect to one another. The same applies to the realization of the capacitances $M6 \cdot C_{ref3}$ and $M8 \cdot C_{ref8}$ in the third capacitor network.

The invention will now be described in greater detail, by way of example, with reference to the accompanying drawings in which

Fig. 1 shows a first embodiment of the converter comprising two integrators,

Fig. 2 shows a part of the embodiment of Fig. 1,

but comprising a different capacitor network, Fig. 3 shows an embodiment of the control unit in the converter of Fig. 1,

Fig. 4 shows a second embodiment of a converter comprising two integrators,

Fig. 5 shows an embodiment of the control unit in the converter of Fig. 4, and

Fig. 6 shows an embodiment of a converter comprising three integrators.

Fig. 1 shows a digital-to-analog converter comprising a series arrangement of a first and a second switched capacitor integrator 1 and 2, respectively. To this end, an output 3 of the first integrator 1 is coupled to an input 4 of the second integrator 2. The integrators comprise amplifier stages 5 and 6 having inverting (-) and non-inverting (+) inputs and outputs 7 and 8, capacitors 9 and 10, respectively, coupled between the inverting input and the output and capacitor networks 11 and 12 comprising at least two capacitors and being coupled between the inputs 13 and 4, respectively, of the integrator and the inverting input of the amplifier stage. The non-inverting inputs (+) of the amplifier stages 5 and 6 are coupled to a point of constant potential (ground). Control signal inputs 14 and 15 of the first and the second integrator 1 and 2 are intended to receive control signals which are applied via the leads 16.1 to 16.m and 17.1 to 17.k, respectively, from a control unit 18. The control signal for the first integrator 1 is applied via the inputs 14.1 to 14.m of the capacitor network 11 to switches 25.1 to 25.m for controlling these switches. The control signal for the second integrator 2 is applied via the inputs 15.1 to 15.k of the capacitor network 12 to switches 26.1 to 26.k for controlling these switches. The capacitor network 11 comprises m capacitors 27.1 to 27.m all having a capacitance C_{ref1} . In the one position of the switches 25.1 to 25.m the capacitors 27.1 to 27.m are coupled between the input terminal 13 and ground and in the other position of these switches the capacitors are coupled between the inverting input of the amplifier stage 5 and ground. The same applies to the switches 26.1 to 26.k in the capacitor network 12. All capacitors 26.1 to 26.k have a capacitance C_{ref2} . The capacitor networks 11 and 12 are rather sensitive to parasitic capacitances, see the description with reference to Fig. 14 in Philips Technisch Tijdschrift 41, no. 4, pages 109-129. In practice a different configuration of the switches and the capacitors will therefore preferably be taken, for example, using the circuits as described with reference to Fig. 13 in the said Journal. Their realization, using the circuit described with reference to Fig. 13a of this Journal, is shown in Fig. 2 for the capacitor network 11. For the explanation of the operation of the embodiment of Fig. 1 the less ideal network may suffice, which is

also described in the aforementioned Journal, see Fig. 11b.

First and second reset signals R1 and R2 are applied via the leads 19 and 20 from the control unit 18 to switching elements 21 and 22 arranged parallel to the capacitors 9 and 10 and being formed as a switch. The control unit 18 derives the control signals from the n-bit digital signal which is applied via the inputs 23.0 to 23.n-1 to the control unit 18. The control unit also receives clock pulses from a clock generator 24.

The converter of Fig. 1 operates as follows. In the shown position of the switches 25.1 to 25.m the capacitors 27.1 to 27.m are charged to the voltage Vref. This position of the switches is realized because, for example, a logic low signal is applied to these switches via all leads 16.1 to 16.m. A reset signal R1 is applied via the lead 19 to the switch 21. The capacitor 9 is thereby discharged. Under the influence of a reset signal R2 the capacitor 10 is also discharged. The reset signal R2 may be generated at a different instant, provided that this instant is before the moment when the integrator 2 performs an integration step for the first time. A first control signal is applied via the leads 16.1 to 16.m to the integrator 1. This means that at M1 of the m leads the signal becomes "high" for a short period. As a result M1 of the m switches change over for a short period to the position different from the one shown. M1 of the m capacitors 25 are discharged, whilst the capacitor 9 is charged thereby. A voltage which is equal to

$$M1 \cdot V_{ref} \cdot C_{ref} / C_2 = M1 \cdot \alpha \cdot V_{ref}$$

is produced at the output 7, in which C2 is the capacitance of the capacitor 9.

In the shown position of the switches 26.1 to 26.k the capacitors 28.1 to 28.k are charged to the above-mentioned voltage. The position of the switch 26 is determined by, for example, a logic low signal which is applied to these switches via the leads 17.1 to 17.k. Subsequently a second control signal is applied to the integrator 2 via the leads 17.1 to 17.k. This means that at M2 (= k-M4) of the k leads 17 a "high" signal is applied for a short period to M2 of the k switches 26 which thereby assumes for a short period the position different from the one shown. M2 capacitors 28 are thus discharged and the capacitor 10 is charged. A voltage which is equal to

$$M1 \cdot (k-M4) \cdot \alpha \cdot \beta \cdot V_{ref}$$

is then produced at the output 8, in which β is equal to C_{ref} / C_4 and C4 is the capacitance of the capacitor 10. Subsequently a third control signal is applied via the leads 16 to the integrator 1. This

means that the signal becomes "high" for a short period at M3 (= 1) of the m leads 16. A voltage which is equal to

$$(M1+1) \cdot \alpha \cdot V_{ref}$$

is then produced at the output 7. Finally the fourth control signal is applied to the integrator 2 via the leads 17. This means that the signal becomes "high" for a short period at M4 of the k leads 17. Preferably they are those M4 of the k leads which remained "low" during the second integration step. The remaining M4 capacitors in the capacitor network 12 are now coupled to the inverting input of the amplifier stage 6. The advantage of this measure is that the spread in the capacitances of the capacitors 26 has a minimum influence on the output signal 7. A voltage which is equal to $M4 \cdot (M1+1) \cdot \alpha \cdot \beta \cdot V_{ref} + M1 \cdot (k-M4) \cdot \alpha \cdot \beta \cdot V_{ref}$ is then produced at the output 8 of the second integrator 2. This is equal to

$$(M1 \cdot k + M4) \cdot \alpha \cdot \beta \cdot V_{ref}, \text{ or for } k = 2^p$$

$$(M1 \cdot 2^p + M4) \cdot \alpha \cdot \beta \cdot V_{ref}, \text{ where } p \leq n.$$

For $k = 2^p$ it then holds that m in Fig. 1 is equal to 2^{n-p} . For converting the n-bit digital signal $b_{n-1} \dots b_0$, see Fig. 1, which is applied to the input 23 of the control unit 18, the (decimal) number LSB is to be taken for M4, corresponding to the binary number $b_{p-1} \dots b_0$, that is to say, the binary number constituted by the p least significant bits of the digital signal. For M1 the (decimal) number MSB is to be taken which corresponds to the binary number $b_{n-1} \dots b_p$, that is to say, the binary number constituted by the n-p most significant bits of the digital signal.

It is clear that in the second and the fourth integration step combined a fixed capacitance of $(M2 + M4) \cdot C_{ref} / 2$ is coupled to the inverting input of the amplifier stage 6 for any arbitrary n-bit digital signal which is converted by the converter. This means that the offset at the output 8 due to the offset V_o at the output 7 has the same fixed value in all cases. This can be shown by means of the following calculation.

After the first integration step the output 7 conveys a voltage

$$M1 \cdot \alpha \cdot V_{ref} + V_o$$

After the second integration step the output 8 conveys a voltage

$$(M1 \cdot \alpha \cdot V_{ref} + V_o) \cdot (k-M4) \cdot \beta$$

After the third integration step the output 7 conveys a voltage

$$(M1+1) \cdot \alpha \cdot V_{ref} + V_0.$$

After the fourth integration step this leads to a voltage at the output 8 which is equal to

$$(M1 \cdot k + M4) \cdot \alpha \cdot \beta \cdot V_{ref} + k \cdot \beta \cdot V_0.$$

Since k is constant for an arbitrary n -bit digital signal, the offset voltage at the output 8 is also constant for an arbitrary digital signal to be converted.

For k is even it will be preferred to take $p = n/2$. This has the advantage that the total number of capacitors in the capacitor networks 11 and 12 is then smallest, namely equal to $2 \cdot 2^p$ and that consequently the required IC surface is smallest. One requirement for the capacitors 27 and also for the capacitors 28 is that they should have a capacitance which is identical as much as possible. The conversion by means of a converter of the type as shown in Fig. 1 then yields a reasonably accurate and fast digital-to-analog conversion. In fact, only five clock pulses of the clock pulse generator 24 are required for one conversion, namely a first clock pulse for generating the reset signals and then four clock pulses for generating the four control signals.

The converter of Fig. 1, comprising capacitor networks like the network 11' of Fig. 2 operates in the same manner as described above. In the case of a logic low signal on the lead 16.1 the switches 25.1a and 25.1b are in the position shown. The capacitor 27.1 is then charged to the voltage V_{ref} . If the signal on the lead 16.1 becomes "high", the two switches 25.1a and 25.1b change over to the position other than the one shown. The capacitor 27.1 now discharges via the inverting input of the amplifier stage 5 so that the capacitor 9 is charged. The switches 25.2a and 25.2b to 25.ma and 25.mb operate in the same way.

Fig. 3 shows a possible embodiment of the control unit 18 in the converter of Fig. 1. The control unit comprises a 5-counter 60. Under the influence of the clock pulses cl of the clock generator 24, applied to the input 61 of the counter 60, a subsequent output 62.i of the five outputs 62.1 to 62.5 each time becomes "high", starting with the output 62.1. This output supplies the reset pulses $R1$ and $R2$. At the next clock pulse the output 62.2 becomes "high". This output is coupled to an input of AND-gates 63.1 to 63.m. Another input of these AND-gates 63 is coupled to an associated output of the m outputs 64.1 to 64.m of a circuit 65. This circuit has $n-p$ inputs 66 to which the digital number MSB is applied, i.e. the digital number $b_{n-1} \dots b_p$ constituted by the $n-p$ most significant bits of the n -bit digital signal to be converted. The circuit

65 renders as many outputs 64 "high", namely a total of $M1$ outputs, as is consistent with the (decimal) number corresponding to the afore mentioned $n-p$ -bit digital number. Thus this means that $m = 2^{n-p}$. Since the output 62.2 is "high", the AND-gates 63 are enabled and the signals at the outputs 64 of the circuit 65 are passed. The signal at the output 64.1 is then applied via the AND-gate 63.1 and an OR-gate 67 to the lead 16.1. Similarly, the signals at the outputs 64.i, in which i extends from 2 to 2^{n-p} , are applied via the AND-gates 63.i to the lead 16.1. This realizes the first integration step in the converter of Fig. 1. At the next clock pulse of the generator 24 the output 62.2 becomes low again, the AND-gates 63 are inhibited and the output 62.3 becomes "high". This output is coupled to an input of AND-gates 68.1 to 68.k so that these gates are enabled. Outputs 69.1 to 69.k of a circuit 70 are coupled via inverters 71.1 to 71.k to the other input of the AND-gates 68.1 to 68.k, respectively. The circuit 70 has p inputs 72.1 to 72.p to which the digital number $b_{p-1} \dots b_0$ corresponding to the p least significant bits of the n -bit digital signal to be converted is applied. The circuit operates in the same way as the circuit 65. This means that $M4$ of the $k (= 2^p)$ outputs 69 become "high". The signals at the outputs 69.i, in which i extends from 1 to k , are now applied via the inverters 71.i, the AND-gates 68.i and the OR-gates 73.i to the leads 17.i. Due to the signal inversion in the inverters 71 this means that $k - M4$ of the k leads 17 convey a "high" signal. This leads to the second integration step in the converter of Fig. 1. At the next clock pulse the output 62.3 becomes "low" again, the AND-gates 68 are inhibited and the output 62.4 becomes "high". This output is coupled to the second input of the OR-gate 67 which thus leads to a "high" signal on the lead 16.1: the third integration step in the converter. At the subsequent clock pulse the output 62.4 becomes "low" again and the output 62.5 becomes "high". The output 62.5 is coupled to an input of k AND-gates 74.1 to 74.k. The other inputs of these AND-gates 74.i are coupled to corresponding outputs 69.i of the circuit 70 (i extends from 1 to k). The outputs of the AND-gate 74.i are each coupled to a second input of the associated OR-gate 73.i. The "high" signal at the output 62.5 enables the AND-gates 74 so that the signals present at the outputs 69 can be applied to the leads 17. This means that a "high" signal appears on $M4$ of the k leads 17. Consequently the complementary part of the capacitors in the network 12 is coupled to the inverting input of the amplifier stage 6. This leads to the fourth integration step in the converter of Fig. 1 whereafter the conversion of the n -bit digital signal is completed. At the next clock pulse of the generator 24 a new n -bit digital signal is applied to

the inputs 66 and 72 of the circuits 65 and 70 and the output 62.5 becomes "low" again and the output 62.1 becomes "high". The conversion of a subsequent n-bit digital signal begins.

Fig. 4 shows a second embodiment of a two-stage digital-to-analog converter which, however, shows great resemblance to the converter of Fig. 1. Only the capacitor networks and the control unit are formed differently. They are now denoted by the reference numerals 11', 12' and 18', respectively. The capacitor network 11' comprises r capacitors 37.1 to 37.r. As will be evident hereinafter, $r = n - p$. The capacitor network 12' comprises p capacitors 38.1 to 38.p. The capacitance of one of the capacitors 37.1 to 37.r is always a factor of 2 larger than that of the capacitor having a previous ordinal number. Thus this means that the capacitors 37.1 to 37.r have a capacitance which is equal to $C_1, 2C_1, \dots, 2^{n-p}C_1$. Similarly the capacitors 38.1 to 38.p have capacitances which are equal to $C_3, 2C_3, \dots, 2^pC_3$, respectively. Preferably, the capacitors 37.2 to 37.r and 38.2 to 38.p are formed by means of a parallel circuit of one or more of the unit capacitors C_1 and C_3 , respectively. This has for its object to achieve an optimum ratio between the capacitances. The control unit 18' operates differently because the control of the capacitor networks must now be different. The converter operates as follows.

The leads 16.1 to 16.r convey a logic low signal so that all switches 25.1 to 25.r are in the position shown. The capacitors 37.1 to 37.r are then charged to the voltage V_{ref} . The control unit 18' firstly applies reset signals R1 and R2 via the leads 19 and 20 to the switches 21 and 22 so that the capacitors 9 and 10 are discharged. Subsequently the signal on a number of the leads 16.1 to 16.r becomes "high" and thus a number of the switches 25.1 to 25.r are changed over for a short period in such a way that a total capacitance of $M1.C_1$ is coupled to the inverting input of the amplifier stage 5. In fact this means that the signal on the lead 16.1 corresponds to the bit b_p of the n-bit digital signal, the signal on the lead 16.2 corresponds to the bit b_{p+1} , etc.... and the signal on the lead 16.r corresponds to the bit b_{n-1} of the n-bit digital signal. Subsequently the signal on a number of the leads 17.1 to 17.p becomes "high" and consequently a number of the switches 26.1 to 26.p are switched over for a short period to the position other than the one shown so that a total capacitance of $(2^p - M4).C_3$ is coupled to the inverting input of the amplifier stage 6. In fact this means that, if a bit b_i of the p-bit digital signal $b_{p-1} \dots b_0$ applied to the inputs 23.0 to 23.p-1 of the control unit 18' has a logic value "0", the signal on the associated lead 17.i becomes "high" (i extending from 0 to p-1). Subsequently the signal on the

lead 16.1 becomes "high" for a short period so that the switch 37.1 changes over for a short period. Then the signal becomes "high" for a short period on a number of the leads 17.1 to 17.p, and this in such a way that a total capacitance of $M4.C_3$ is coupled to the inverting input of the amplifier stage 6. In fact this means that if a bit b_i of the aforementioned p-bit digital number is a logic "1", the signal on the associated lead 17.i, i.e. the lead having the same index i as the bit b_i is "high" (with i extending again from 0 to p-1).

Fig. 5 shows an embodiment of the control unit 18' in the converter of Fig. 4. The circuit diagram of the control unit of Fig. 5 shows great resemblance to the control unit of Fig. 3. The only difference with the control unit of Fig. 3. is that the circuits 65 and 70 of this control unit are absent in the control unit of Fig. 5 and that there are only r (= n-p) AND-gates 63, p AND-gates 68, p AND-gates 74, p OR-gates 73 and p inverters 71. This means that the inputs 23.0 to 23.p-1 are now directly coupled to the inverters 71.1 to 71.p and the AND-gates 68.1 to 68.p and that the inputs 23.p to 23.n-1 are now directly coupled to the AND-gates 63.1 to 63.r. Otherwise, the operation of this control unit is identical to that of the control unit of Fig. 3 so that it does not require any further explanation.

Fig. 6 shows a three-stage converter for converting an n-bit digital signal. The integrators 1 and 2 of the converters are identical in structure to the integrators 1 and 2 of the converter of Fig. 1. The structure of integrator 43 is identical to that of the integrators 1 and 2. The capacitor network 57 comprises k' capacitors 53.1 to 53.k' arranged between ground and associated switches 51.1 to 51.k'. All capacitors 53 have the same capacitance C_{ref3} . The switches 51 are switchable under the influence of signals which are generated by the control unit 18' and which are applied via the leads 47.1 to 47.k' to the switches. A reset signal R3 is applied via the lead 49 to the switch 50 which is arranged parallel to the capacitor 54 for discharging this capacitor.

The converter of Fig. 6 operates as follows. The first four integration steps of the converter of Fig. 6 correspond to the four integration steps of the converter of Fig. 1. As already described hereinbefore, the output 8 then conveys a voltage which is equal to

$$(M1.k + M4).a.\beta.V_{ref}.$$

Subsequently a reset signal R1 is generated again. The voltage at the output 7 thus becomes equal to zero. Then a "high" signal, the fifth control signal, is generated on a number of the signal leads 16 and this in such a way that a total capacitance of

M5.Cref1 is coupled for a short period to the inverting input of the amplifier stage 5. This means that the signal on the lead 16.1 becomes "high" (M5 = 1). A voltage which is equal to

$$\alpha \cdot V_{ref}.$$

is then produced at the output 7. After the reset signal R3 has been applied to the switch 50, the capacitor 54 is discharged. Note that this discharge could also have taken place at an earlier moment. For example, it could have coincided in time with the discharge of the capacitors 9 and 10 at the start of the conversion. Subsequently the control unit 18" generates a sixth control signal across the leads 47.1 to 47.k' in such a way that a total capacitance of M6.Cref3 (= k' - M8).Cref3 is coupled to the inverting input of the amplifier stage 55. A voltage which is equal to

$$(k' - M8) \cdot \delta \cdot (M1 \cdot k + M4) \cdot \alpha \cdot \beta \cdot V_{ref},$$

is then produced at the output 56 of the amplifier stage 55, in which $\delta = C_{ref3}/C_6$ and C_6 is the capacitance of the capacitor 54. Here it holds that this last integration step could alternatively have been performed earlier, but after the fourth integration step. Subsequently, under the influence of the seventh control signal applied via the leads 17.1 to 17.k to the capacitor network 12, such a number of switches 26 is switched for a short period to the position other than the one shown that a total capacitance of M7.Cref2 is coupled to the inverting input of the amplifier stage 6. This means that, for example, the signal on the lead 17.1 becomes "high" (M7 = 1). A voltage which is equal to

$$\alpha \cdot \beta \cdot V_{ref} + (M1 \cdot k + M4) \cdot \alpha \cdot \beta \cdot V_{ref}.$$

is then produced at the output 8. Subsequently, under the influence of an eighth control signal applied via the leads 47 to the capacitor network 57, a total capacitance of M8.Cref3 is coupled to the inverting input of the amplifier stage 55. The complementary part of the capacitors 53 in the network 57 is preferably coupled to the inverting input of the amplifier stage 55. A voltage which is equal to

$$(k \cdot k' \cdot M1 + k' \cdot M4 + M8) \cdot \alpha \cdot \beta \cdot \delta \cdot V_{ref}.$$

is then produced at the output 56.

For $k = 2^p$ and $k' = 2^q$ this reduces to $(M1 \cdot 2^{(p+q)} + M4 \cdot 2^q + M8) \cdot \alpha \cdot \beta \cdot \delta \cdot V_{ref}$, in which $p + q \leq n$.

This means that the capacitor network 11 of Fig. 6 has $m (= 2^{n-p-q})$ capacitors 25.

For converting the n-bit digital signal $b_{n-1} \dots b_0$, see Fig. 6, which is applied to the input 23 of the control unit 18" the (decimal) number LSB should thus be taken for M8, which number corresponds to the binary number $b_{q-1} \dots b_0$ constituted by the q least significant bits in the n-bit digital signal. For M1 the (decimal) number MSB should be taken which number corresponds to the binary number $b_{n-1} \dots b_{p+q}$ constituted by the n-p-q most significant bits of the digital signal. For M4 the (decimal) number ISB should be taken, which number corresponds to the binary number $b_{p+q-1} \dots b_q$ constituted by the remaining p bits.

If the offset $k \cdot \beta \cdot V_0$ present after the fourth integration step at the output 8 had been included in the calculation, this offset would have given rise to an offset of $(M8 + k \cdot k') \cdot \beta \cdot \delta \cdot V_0$ at the output 56 after the eighth integration step. Only the term $M8 \cdot \beta \cdot \delta \cdot V_0$ is dependent on the value of the n-bit digital signal. β and δ are both generally smaller than 1 and are, for example, equal to $1/k'$ or 2^{-q} and $1/k$ or 2^{-p} , respectively. Similarly, α is then equal to 2^{n-p-q} . Thus, for the largest possible n-bit digital signal an amplitude is obtained in each stage which is equal to the input signal in the same stage. Thus this means that the term $M8 \cdot \beta \cdot \delta \cdot V_0$ contributes to a small extent to the total offset at the output 56.

For n which is divisible by 3 and $p = q = n/3$ the total number of capacitors in the capacitor networks is smallest, namely $3 \cdot 2^{n/3}$ and the required IC surface is smallest. Moreover, a three-stage converter, at a sufficiently large value for n, will require fewer capacitors than the two-stage converters of Figs. 1 and 4, at an equal value of n for the two types of converters. However, the three-stage converter requires more clock pulses of the clock generator 24 than does the two-stage converter. Thus, the conversion in the three-stage converter takes slightly longer than the conversion in the two-stage converter.

It is of course evident that the control unit 18" in Fig. 6 may have a structure which is analogous to that of the control unit of Fig. 3. For designing a circuit for the control unit 18" it is thus not necessary to use knowledge beyond that of those skilled in the art. In fact the circuit is no more than the logical and obvious extension of the control unit for a two-stage converter to a control unit for a three-stage converter. A further explanation of the control unit 18 can therefore be dispensed with.

It is to be noted that the invention can also be used for those embodiments differing from the points of the embodiments not relating to the invention. For example, it is possible to provide the three-stage converter of Fig. 6 with other capacitor networks, for example, capacitor networks in the form described with reference to Fig. 2 or 4. If the

capacitor networks of Fig. 4 are used, it will be evident that the control will be different and hence the control unit will be formed differently. Such a control unit is then a logical extension of the control unit of Fig. 5 for use in a three-stage converter, for which no special knowledge is required either.

Claims

1. A digital-to-analog converter for converting a digital signal having a word length n into an analog signal, comprising
 - a series arrangement of at least a first and a second integrating circuit each having an input and an output and a control signal input, the input of the first integrating circuit being adapted to receive a reference voltage, the output of the first integrating circuit being coupled to the input of the second integrating circuit, the output of the last integrating circuit in the series arrangement being coupled to the output of the digital-to-analog converter, each of the (first and second) integrating circuits comprising a first and a second amplifier stage, respectively, having an inverting and a non-inverting input and an output and a first and a second capacitor, respectively, coupled between the inverting input and the output of the first and the second amplifier stage, respectively, the first and the second integrating circuit being adapted to perform an integration step under the influence of a control signal applied to the control signal input,
 - a control unit having an input, and at least a first and a second output coupled to the control signal input of the first and the second integrating circuit, respectively, the input of the control unit being adapted to receive n bits digital signals for conversion, wherein for converting the n bit digital signal said control unit is adapted to generate in response to the n bit digital signal applied to its input, in this order, a first control signal at its first output, a second control signal at its second output, a third control signal at its first output and a fourth control signal at its second output, characterized in that the integrators are switched capacitor integrators and in that a first capacitor network comprising at least two capacitors is coupled between the input of the first integrator and the inverting input of the first amplifier stage, a second capacitor network comprising at least two capaci-

tors being coupled between the input of the second integrator and the inverting input of the second amplifier stage, the first capacitor network being adapted to couple during a given time interval a total capacitance of $M1.Cref1$ and $M3.Cref1$ to the inverting input of the first amplifier stage under the influence of the first and the third control signal, respectively, the second capacitor network being adapted to couple during a given time interval a total capacitance of $M2.Cref2$ and $M4.Cref2$ to the inverting input of the second amplifier stage under the influence of the second and the fourth control signal, respectively, $Cref1$ and $Cref2$ being fixed capacitances, and in that for converting arbitrary digital signals having a word length n it holds that $M2 + M4$ is equal to a constant (k).

2. A digital-to-analog converter as claimed in Claim 1 for converting an n -bit digital signal, characterized in that the constant (k) is equal to 2^p , in which $p \leq n$.
3. A digital-to-analog converter as claimed in Claim 2, characterized in that $M3 = 1$, in that $M4$ is the value corresponding to the binary number formed by the p least significant bits of the n -bit digital signal and in that $M1$ is the value corresponding to the binary number formed by the $n-p$ most significant bits of the n -bit digital signal.
4. A digital-to-analog converter as claimed in Claim 1 or 2, characterized in that a third switched capacitor integrator comprising a third amplifier stage, a third capacitor coupled between an inverting input and an output of this amplifier stage and a third capacitor network comprising at least two capacitors coupled between an input of the third integrator and the inverting input of the amplifier stage is arranged in series with the second switched capacitor integrator, said third integrator being adapted to perform an integration step under the influence of a control signal at a control signal input of said integrator, the control unit being adapted to generate in response to the n bit digital signal applied to its input a reset signal for bringing the signal at the output of the first integrator to an initial level and for subsequently generating a fifth control signal to be applied to a first output, the control unit being further adapted to generate, in this order, a sixth control signal and an eighth control signal to be applied to a third output which is



capacitor networks of Fig. 4 are used, it will be evident that the control will be different and hence the control unit will be formed differently. Such a control unit is then a logical extension of the control unit of Fig. 5 for use in a three-stage converter, for which no special knowledge is required either.

Claims

1. A digital-to-analog converter for converting a digital signal having a word length n into an analog signal, comprising
 - a series arrangement of at least a first and a second integrating circuit each having an input and an output and a control signal input, the input of the first integrating circuit being adapted to receive a reference voltage, the output of the first integrating circuit being coupled to the input of the second integrating circuit, the output of the last integrating circuit in the series arrangement being coupled to the output of the digital-to-analog converter, each of the (first and second) integrating circuits comprising a first and a second amplifier stage, respectively, having an inverting and a non-inverting input and an output and a first and a second capacitor, respectively, coupled between the inverting input and the output of the first and the second amplifier stage, respectively, the first and the second integrating circuit being adapted to perform an integration step under the influence of a control signal applied to the control signal input,
 - a control unit having an input, and at least a first and a second output coupled to the control signal input of the first and the second integrating circuit, respectively, the input of the control unit being adapted to receive n bits digital signals for conversion, wherein for converting the n bit digital signal said control unit is adapted to generate in response to the n bit digital signal applied to its input, in this order, a first control signal at its first output, a second control signal at its second output, a third control signal at its first output and a fourth control signal at its second output, characterized in that the integrators are switched capacitor integrators and in that a first capacitor network comprising at least two capacitors is coupled between the input of the first integrator and the inverting input of the first amplifier stage, a second capacitor network comprising at least two capacitors

tors being coupled between the input of the second integrator and the inverting input of the second amplifier stage, the first capacitor network being adapted to couple during a given time interval a total capacitance of $M1.Cref1$ and $M3.Cref1$ to the inverting input of the first amplifier stage under the influence of the first and the third control signal, respectively, the second capacitor network being adapted to couple during a given time interval a total capacitance of $M2.Cref2$ and $M4.Cref2$ to the inverting input of the second amplifier stage under the influence of the second and the fourth control signal, respectively, $Cref1$ and $Cref2$ being fixed capacitances, and in that for converting arbitrary digital signals having a word length n it holds that $M2 + M4$ is equal to a constant (k).

2. A digital-to-analog converter as claimed in Claim 1 for converting an n -bit digital signal, characterized in that the constant (k) is equal to 2^p , in which $p \leq n$.
3. A digital-to-analog converter as claimed in Claim 2, characterized in that $M3 = 1$, in that $M4$ is the value corresponding to the binary number formed by the p least significant bits of the n -bit digital signal and in that $M1$ is the value corresponding to the binary number formed by the $n-p$ most significant bits of the n -bit digital signal.
4. A digital-to-analog converter as claimed in Claim 1 or 2, characterized in that a third switched capacitor integrator comprising a third amplifier stage, a third capacitor coupled between an inverting input and an output of this amplifier stage and a third capacitor network comprising at least two capacitors coupled between an input of the third integrator and the inverting input of the amplifier stage is arranged in series with the second switched capacitor integrator, said third integrator being adapted to perform an integration step under the influence of a control signal at a control signal input of said integrator, the control unit being adapted to generate in response to the n bit digital signal applied to its input a reset signal for bringing the signal at the output of the first integrator to an initial level and for subsequently generating a fifth control signal to be applied to a first output, the control unit being further adapted to generate, in this order, a sixth control signal and an eighth control signal to be applied to a third output which is



- coupled to the control signal input of the third integrator and being adapted to generate, after the sixth control signal and before the eighth control signal, a seventh control signal to be applied to the second output, the first capacitor network being further adapted to couple during a given time interval a total capacitance of $M5.Cref1$ to the inverting input of the first amplifier stage under the influence of the fifth control signal, the third capacitor network being adapted to couple during a given time interval a total capacitance of $M6.Cref3$ and $M8.Cref3$ to the inverting input of the third amplifier stage under the influence of the sixth and the eighth control signal, respectively, the second capacitor network being adapted to couple during a given time interval a total capacitance of $M7.Cref2$ to the inverting input of the second amplifier stage under the influence of the seventh control signal, $Cref3$ being a fixed capacitance.
5. A digital-to-analog converter as claimed in Claim 4, characterized in that for converting arbitrary digital signals having a word length n it holds that $M6 + M8$ is equal to a constant (k').
 6. A digital-to-analog converter as claimed in Claim 5 for converting an n -bit digital signal, characterized in that the constant (k') is equal to 2^q in which $p + q \leq n$.
 7. A digital-to-analog converter as claimed in Claim 6, characterized in that $M3 = M5 = M7 = 1$, in that $M8$ is the value corresponding to the binary number constituted by the q least significant bits of the n -bit digital signal, $M1$ is the value corresponding to the binary number constituted by the $n-p-q$ most significant bits and $M4$ is the value corresponding to the binary number constituted by the remaining p bits of the n -bit digital signal.
 8. A digital-to-analog converter as claimed in Claim 1, 2 or 3, characterized in that n is an even number and in that $p = n/2$.
 9. A digital-to-analog converter as claimed in any one of Claims 4 to 7, characterized in that n is a number which is divisible by 3 and in that $p = q = n/3$.
 10. A digital-to-analog converter as claimed in Claim 4, characterized in that a parallel arrangement of another switching element and the capacitor is coupled between the inverting input and the output of the first integrating circuit and in that the other switching element has a control signal input for receiving the reset signal.
 11. A digital-to-analog converter as claimed in any one of the preceding Claims, characterized in that all capacitors in a capacitor network have a substantially identical capacitance.
 12. A digital-to-analog converter as claimed in any one of Claims 1 to 10, characterized in that, whilst adding an index m (in which m is an integer) to the capacitors in a capacitor network, in which the index 1 is assigned to the capacitor having the lowest capacitance and subsequent indices are assigned to capacitors having a subsequent increasing capacitance, it holds that the capacitance ratio between the capacitor with index l and that with index $l + 1$ is substantially equal to $1/2$ for each value of l , in which $1 \leq l \leq l_m - 1$ and l_m is the highest index value.
 13. A digital-to-analog converter as claimed in Claim 1, characterized in that the total capacitances $M2.Cref2$ and $M4.Cref2$ are constituted by parts in the second capacitor network which are complementary to one another.
 14. A digital-to-analog converter as claimed in Claim 5, characterized in that the total capacitances $M6.Cref3$ and $M8.Cref3$ are constituted by parts in the third capacitor network which are complementary to one another.

Revendications

1. Convertisseur numérique-analogique pour convertir un signal numérique de longueur de mot n en un signal analogique, comportant
 - un montage en série d'au moins un premier et un deuxième circuit intégrateur ayant chacun une entrée et une sortie ainsi qu'une entrée de signal de commande, l'entrée du premier circuit intégrateur étant agencée pour recevoir une tension de référence, la sortie du premier circuit intégrateur étant couplée à l'entrée du deuxième circuit intégrateur, la sortie du dernier circuit intégrateur du montage en série étant couplée à la sortie du convertisseur numérique-analogique, les (premier et deuxième) circuits intégrateurs comportant chacun des premier et deuxième étages amplificateurs ayant une entrée inverseuse et une entrée non inverseuse ainsi qu'une sortie et ayant respectivement des premier et



deuxième condensateurs couplés entre l'entrée inverseuse et la sortie respectivement des premier et deuxième étages amplificateurs, les premier et deuxième circuits intégrateurs étant agencés pour effectuer une étape d'intégration sous l'influence d'un signal de commande appliqué à l'entrée de signal de commande,

- une unité de commande ayant une entrée et au moins des premier et deuxième sorties couplées à l'entrée de signal de commande respectivement des premier et deuxième circuits intégrateurs, l'entrée de l'unité de commande étant agencée pour recevoir des signaux numériques à n bits en vue de leur conversion, unité de commande qui, pour convertir le signal numérique à n bits, est agencée pour engendrer, en réaction au signal numérique à n bits appliqué à son entrée, dans cet ordre, un premier signal de commande sur sa première sortie, un deuxième signal de commande sur sa deuxième sortie, un troisième signal de commande sur sa première sortie et un quatrième signal de commande sur sa deuxième sortie, caractérisé en ce que les intégrateurs sont des intégrateurs à condensateurs commutables et en ce qu'entre l'entrée du premier intégrateur et l'entrée inverseuse du premier étage amplificateur, est couplé un premier circuit de condensateurs comportant au moins deux condensateurs et, entre l'entrée du deuxième intégrateur et l'entrée inverseuse du deuxième étage amplificateur, est couplé un deuxième circuit de condensateurs comportant au moins deux condensateurs, le premier circuit de condensateurs étant agencé pour coupler, pendant un intervalle de temps donné, une capacité totale de $M1.Cref1$ et de $M3.Cref1$ à l'entrée inverseuse du premier étage amplificateur, sous l'influence respectivement des premier et troisième signaux de commande et le deuxième circuit de condensateurs étant agencé pour coupler, pendant un intervalle de temps donné, une capacité totale de $M2.Cref2$ et de $M4.Cref2$ à l'entrée inverseuse du deuxième étage amplificateur, sous l'influence respectivement des deuxième et quatrième signaux de commande, $Cref1$ et $Cref2$ étant des capacités fixes, et en ce que, pour la conversion de signaux numériques arbitraires de longueur de mot n , $M2 + M4$ est égal

à une constante (k).

- 2. Convertisseur numérique-analogique selon la revendication 1, pour convertir un signal numérique à n bits, caractérisé en ce que la constante (k) est égale à 2^p , où $p \leq n$.
- 3. Convertisseur numérique-analogique selon la revendication 2, caractérisé en ce que $M3 = 1$, en ce que $M4$ est la valeur correspondant au nombre binaire formé par les p bits de poids le plus faible du signal numérique à n bits et en ce que $M1$ est la valeur correspondant au nombre binaire formé par les $n-p$ bits de poids le plus fort du signal numérique à n bits.
- 4. Convertisseur numérique-analogique selon la revendication 1 ou 2, caractérisé en ce qu'un troisième intégrateur à condensateurs commutables comportant un troisième étage amplificateur, un troisième condensateur couplé entre une entrée inverseuse et une sortie de cet étage amplificateur et un troisième circuit de condensateurs comportant au moins deux condensateurs couplés entre une entrée du troisième intégrateur et l'entrée inverseuse de l'étage amplificateur est disposé en série avec le deuxième intégrateur à condensateurs commutables, ledit troisième intégrateur étant agencé pour effectuer une étape d'intégration sous l'influence d'un signal de commande sur une entrée de signal de commande dudit intégrateur, l'unité de commande étant agencée pour engendrer, en réaction au signal numérique à n bits appliqué à son entrée, un signal de remise à un niveau initial pour remettre à un niveau initial le signal sur la sortie du premier intégrateur et pour engendrer ensuite un cinquième signal de commande devant être appliqué à une première sortie, l'unité de commande étant encore agencée, d'une part, pour engendrer, dans cet ordre, un sixième signal de commande et un huitième signal de commande devant être appliqués à une troisième sortie couplée à l'entrée de signal de commande du troisième intégrateur et, d'autre part, pour engendrer, après le sixième signal de commande et avant le huitième signal de commande, un septième signal de commande devant être appliqué à la deuxième sortie, le premier circuit de condensateurs étant encore agencé pour coupler, pendant un intervalle de temps donné, une capacité totale de $M5.Cref1$ à l'entrée inverseuse du premier étage amplificateur, sous l'influence du cinquième signal de commande, le troisième circuit de condensateurs étant agencé pour coupler, pendant un intervalle de temps donné, une capacité totale



- de M6.Cref3 et de M8.Cref3 à l'entrée inverseuse du troisième étage amplificateur, sous l'influence respectivement des sixième et huitième signaux de commande, et le deuxième circuit de condensateurs étant agencé pour coupler, pendant un intervalle de temps donné, une capacité totale de M7.Cref2 à l'entrée inverseuse du deuxième étage amplificateur, sous l'influence du septième signal de commande, Cref3 étant une capacité fixe.
5. Convertisseur numérique-analogique selon la revendication 4, caractérisé en ce que, pour la conversion de signaux numériques arbitraires de longueur de mot n , $M6 + M8$ est égal à une constante (k').
6. Convertisseur numérique-analogique selon la revendication 5, pour convertir un signal numérique à n bits, caractérisé en ce que la constante (k') est égale à 2^q , où $p + q \leq n$.
7. Convertisseur numérique-analogique selon la revendication 6, caractérisé en ce que $M3 = M5 = M7 = 1$, en ce que $M8$ est la valeur correspondant au nombre binaire constitué par les q bits de poids le plus faible du signal numérique à n bits, $M1$ est la valeur correspondant au nombre binaire constitué par les $n - p - q$ bits de poids le plus fort et $M4$ est la valeur correspondant au nombre binaire constitué par les p bits restants du signal numérique à n bits.
8. Convertisseur numérique-analogique selon la revendication 1, 2 ou 3, caractérisé en ce que n est un nombre pair et en ce que $p = n/2$.
9. Convertisseur numérique-analogique selon l'une quelconque des revendications 4 à 7, caractérisé en ce que n est un nombre pouvant être divisé par 3 et en ce que $p = q = n/3$.
10. Convertisseur numérique-analogique selon la revendication 4, caractérisé en ce qu'entre l'entrée inverseuse et la sortie du premier circuit intégrateur, est disposé un montage parallèle d'un autre élément commutateur et du condensateur, et en ce que l'autre élément commutateur a une entrée de signal de commande pour recevoir le signal de remise à un niveau initial.
11. Convertisseur numérique-analogique selon l'une quelconque des revendications précédentes, caractérisé en ce que tous les condensateurs contenus dans un circuit de condensateurs ont des capacités sensiblement identiques.
12. Convertisseur numérique-analogique selon l'une quelconque des revendications 1 à 10, caractérisé en ce que, avec l'addition d'un indice m (où m est un entier) aux condensateurs du circuit de condensateurs, l'indice 1 étant attribué au condensateur de capacité la plus faible et des indices suivants étant attribués à des condensateurs de capacités suivantes croissantes, le rapport de capacités entre le condensateur d'indice i et celui d'indice $i + 1$ est sensiblement égal à $1/2$ pour chaque valeur de i , où $1 \leq i \leq i_{m-1}$ et i_m est la valeur d'indice la plus élevée.
13. Convertisseur numérique-analogique selon la revendication 1, caractérisé en ce que les capacités totales M2.Cref2 et M4.Cref2 sont constituées par des parties du deuxième circuit de condensateurs qui sont complémentaires l'une de l'autre.
14. Convertisseur numérique-analogique selon la revendication 5, caractérisé en ce que les capacités totales M6.Cref3 et M8.Cref 3 sont constituées par des parties du troisième circuit de condensateurs qui sont complémentaires l'une de l'autre.

Patentansprüche

1. Digital/Analog-Wandler zum Umsetzen eines Digitalsignals mit einer Wortlänge n in ein analoges Signal, mit
- einer Reihenschaltung aus Wenigstens einer ersten und einer zweiten integrierten Schaltung mit je einem Eingang, je einem Ausgang und je einem Steuereingang, wobei der Eingang der ersten integrierten Schaltung zum Empfangen einer Bezugsspannung dient, der Ausgang der ersten integrierten Schaltung mit dem Eingang der zweiten integrierten Schaltung gekoppelt ist, der Ausgang der letzten integrierten Schaltung in der Reihenschaltung mit dem Ausgang des Digital/Analog-Wandlers gekoppelt ist, jede der (ersten und zweiten) integrierten Schaltungen eine erste bzw. eine zweite Verstärkerstufe mit einem invertierenden und einem nicht invertierenden Eingang und einem Ausgang und einem ersten bzw. einem zweiten Kondensator enthält, die zwischen dem invertierenden Eingang und dem Ausgang der ersten bzw. dem zweiten Verstärkerstufe gekoppelt



- sind, wobei die erste und die zweite integrierte Schaltung zur Durchführung eines Integrationsschritts unter der Steuerung eines dem Steuersignaleingang zugeführten Steuersignals dient,
- 5 einer Steuereinheit mit einem Eingang und wenigstens einem ersten und einem zweiten Ausgang, die mit dem Steuersignaleingang der ersten bzw. der zweiten integrierten Schaltung gekoppelt sind, wobei der Eingang der Steuereinheit zum Empfangen von n-Bit-Digitalsignalen zur Umsetzung dient, worin zum Umsetzen des n-Bit-Digitalsignals die Steuereinheit zum Erzeugen eines ersten Steuersignals an ihrem ersten Ausgang, eines zweiten Steuersignals an ihrem zweiten Ausgang, eines dritten Steuersignals an ihrem ersten Ausgang und eines vierten Steuersignals an ihrem zweiten Ausgang in dieser Reihenfolge in Beantwortung des ihrem Eingang zugeführten n-Bit-Digitalsignals dient, dadurch gekennzeichnet, daß die Integratoren geschaltete Kondensatorintegratoren sind, und daß ein erstes Kondensatornetzwerk mit wenigstens zwei Kondensatoren zwischen dem Eingang des ersten Integrators und dem invertierenden Eingang der ersten Verstärkerstufe gekoppelt ist, wobei ein zweites Kondensatornetzwerk mit wenigstens zwei Kondensatoren zwischen dem Eingang des zweiten Integrators und dem invertierenden Eingang der zweiten Verstärkerstufe gekoppelt ist, wobei das erste Kondensatornetzwerk zum Koppeln einer Gesamtkapazität von $M1.Cref1$ und $M3.Cref1$ an den invertierenden Eingang der ersten Verstärkerstufe unter der Steuerung des ersten bzw. des dritten Steuersignals in einem vorgegebenen Zeitintervall dient, das zweite Kondensatornetzwerk zum Koppeln einer Gesamtkapazität von $M2.Cref2$ und $M4.Cref2$ an den invertierenden Eingang der zweiten Verstärkerstufe unter der Steuerung des zweiten bzw. des vierten Steuersignals in einem vorgegebenen Zeitintervall dient, und $Cref1$ und $Cref2$ festen Kapazitätswerten sind, und daß zum Umsetzen beliebiger Digitalsignale mit einer Wortlänge n gilt, daß $M2 + M4$ gleich einer Konstante (k) ist.
2. Digital/Analog-Wandler nach Anspruch 1 zum Umsetzen eines n-Bit-Digitalsignals, dadurch gekennzeichnet, daß die Konstante (k) gleich 2^p ist, worin $p \leq n$ ist.
3. Digital/Analog-Wandler nach Anspruch 2, dadurch gekennzeichnet, daß $M3 = 1$ ist, daß $M4$ der Wert entsprechend der von den p Bits mit niedrigster Wertigkeit des n-Bit-Digitalsignals gebildeten Binärzahl ist, und daß $M1$ der Wert entsprechend der von den $n-p$ Bits mit höchster Wertigkeit des n-Bit-Digitalsignals gebildeten Binärzahl ist.
- 10 4. Digital/Analog-Wandler nach Anspruch 1 oder 2, dadurch gekennzeichnet, daß ein dritter geschalteter Kondensatorintegrator mit einer dritten Verstärkerstufe, einem dritten Kondensator zwischen einem invertierenden Eingang und einem Ausgang dieser Verstärkerstufe und mit einem dritten Kondensatornetzwerk, das wenigstens zwei zwischen einem Eingang des dritten Integrators und dem invertierenden Eingang der Verstärkerstufe gekoppelte Kondensatoren enthält, in Reihe mit dem zweiten geschalteten Kondensatorintegrator geschaltet ist, wobei der dritte Integrator zur Durchführung eines Integrationsschritts unter der Steuerung eines Steuersignals an einem Steuersignaleingang des Integrators dient, die Steuereinheit zum Erzeugen eines Rückstellsignals zum Einstellen des Signals am Ausgang des ersten Integrators auf einen Anfangspegel in Beantwortung des n-Bit-Digitalsignals an ihrem Eingang und zum anschließenden Erzeugen eines ersten Ausgang zuzuführenden fünften Steuersignals dient, die Steuereinheit außerdem zum Erzeugen eines sechsten Steuersignals und eines achten Steuersignals zum Weiterleiten an einen dritten Ausgang in dieser Reihenfolge dient, der mit dem Steuersignaleingang des dritten Integrators gekoppelt ist und zum Erzeugen eines dem zweiten Ausgang zuzuführenden siebten Steuersignals nach dem sechsten Steuersignal und vor dem achten Steuersignal dient, wobei das erste Kondensatornetzwerk außerdem zum Koppeln einer Gesamtkapazität von $M5.Cref1$ an den invertierenden Eingang der ersten Verstärkerstufe unter der Steuerung des fünften Steuersignals für ein vorgegebenes Zeitintervall dient, das dritte Kondensatornetzwerk zum Koppeln einer Gesamtkapazität von $M6.Cref3$ und $M8.Cref3$ an den invertierenden Eingang der dritten Verstärkerstufe unter der Steuerung des sechsten bzw. des achten Steuersignals dient, und das zweite Kondensatornetzwerk zum Koppeln einer Gesamtkapazität von $M7.Cref2$ an den invertierenden Eingang der zweiten Verstärkerstufe unter der Steuerung des siebten Steuersignals dient, worin $Cref3$ eine feste Kapazitätswert darstellt.



5. Digital/Analog-Wandler nach Anspruch 4, dadurch gekennzeichnet, daß zum Umsetzen beliebiger Digitalsignale mit einer Wortlänge n gilt, daß $M6 + M8$ gleich einer Konstante (k') ist.
6. Digital/Analog-Wandler nach Anspruch 5 zum Umsetzen eines n -Bit-Digitalsignals, dadurch gekennzeichnet, daß die Konstante (k') gleich 2^q ist, worin $p + q \leq n$ ist.
7. Digital/Analog-Wandler nach Anspruch 6, dadurch gekennzeichnet, daß $M3 = M5 = M7 = 1$ ist, daß $M8$ der Wert entsprechend der von den q Bits mit niedrigster Wertigkeit des n -Bit-Digitalsignals gebildeten Binärzahl ist, und daß $M1$ der Wert entsprechend der von den $n-p-q$ Bits mit höchster Wertigkeit gebildeten Binärzahl und $M4$ der Wert entsprechend der von den restlichen p Bits des n -Bit-Digitalsignals gebildeten Binärzahl ist.
8. Digital/Analog-Wandler nach Anspruch 1, 2 oder 3, dadurch gekennzeichnet, daß n eine gerade Zahl und $p = n/2$ ist.
9. Digital/Analog-Wandler nach einem der Ansprüche 4 bis 7, dadurch gekennzeichnet, daß n eine durch 3 teilbare Zahl und $p = q = n/3$ ist.
10. Digital/Analog-Wandler nach Anspruch 4, dadurch gekennzeichnet, daß eine Parallelschaltung eines weiteren Schaltungselements und des Kondensators zwischen dem Invertierenden Eingang und dem Ausgang der ersten integrierten Schaltung gekoppelt ist, und daß das weitere Schaltungselement einen Steuersignaleingang zum Empfangen des Rückstellsignals besitzt.
11. Digital/Analog-Wandler nach einem der vorangehenden Ansprüche, dadurch gekennzeichnet, daß sämtliche Kondensatoren in einem Kondensatornetzwerk eine im wesentlichen gleiche Kapazität besitzen.
12. Digital/Analog-Wandler nach einem der Ansprüche 1 bis 10, dadurch gekennzeichnet, daß, wenn den Kondensatoren in einem Kondensatornetzwerk ein Index m (worin m eine ganze Zahl ist) zugegeben wird, wobei der Index 1 dem Kondensator mit der niedrigsten Kapazität und folgende Indizes den Kondensatoren mit einer jeweils höheren Kapazität zugeordnet werden, es gilt, daß das Kapazitätsverhältnis zwischen dem Kondensator mit dem Index i und dem mit dem Index $i + 1$ im wesentlichen gleich $1/2$ für jeden Wert von i ist, worin $1 \leq i \leq i_{m-1}$ ist und i_m der höchste Indexwert ist.
13. Digital/Analog-Wandler nach Anspruch 1, dadurch gekennzeichnet, daß die Gesamtkapazitäten $M2.Cref2$ und $M4.Cref2$ durch Teile im zweiten Kondensatornetzwerk gebildet werden, die einem dem anderen komplementär sind.
14. Digital/Analog-Wandler nach Anspruch 5, dadurch gekennzeichnet, daß die Gesamtkapazitäten $M6.Cref3$ und $M8.Cref3$ durch Teile im dritten Kondensatornetzwerk gebildet werden, die einem dem anderen komplementär sind.