

Description

This invention relates to an analog-to-digital (A-D) encoder for converting analog signals, particularly but not exclusively audio signals, to digital signals, and to a digital-to-analog (D-A) decoder for re-converting the digital signals to analog form.

Many digital systems have been proposed for transmitting electrical signals, such as in the delivery of audio signals from a broadcast centre to the consumer. One proposed system employs linear pulse code modulation (PCM) in which the quantizing step-sizes remain constant throughout the transmission. To preserve the quality of signals transmitted and in particular to retain the resolution for small signals, at least 13 bits per sample are required, while 14 or 16 bit systems are commonly used. For broadcasting of audio signals, the bandwidth is typically 15 kHz. Thus linear PCM systems require high bit rates of transmission (a minimum of about 32 kHz x 13 bits i.e. 416 kbit per second even without any provision for error identification or correction). A linear PCM system must also employ high precision components and is therefore expensive.

To reduce transmission bit rate, some conventional PCM systems have employed digital companding. While the transmission bit rate can be reduced somewhat, precision 13 or 14 bit converters must still be used and digital companding further adds complexity and cost to the circuitry. Hence linear or digitally companded PCM systems are unattractive for cost sensitive applications such as use in the home.

Delta modulation systems are attractive for signal transmission because of cost savings in their hardware; delta modulation systems employ simple circuits and do not require close component tolerance. Delta modulation systems are also inherently less disturbed by uncorrected transmission errors. Linear delta modulation systems however require much higher bit rates than PCM systems to achieve the same quality transmission and are therefore unattractive.

Bit-rate reduction has also been applied to delta modulation systems by varying the effective quantizing step-size. Such delta modulation systems are known as adaptive delta modulation (ADM) systems. Digital companding in multi-level PCM systems is performed usually by quantizing to the highest degree of resolution for small signals and then reducing the resolution for large amplitude signals. With ADM systems whose bit-streams have only two states, the adaptation is usually performed by directly altering the quantizing increment between those states either on an instantaneous (sample to sample) basis, on a block basis ("near-instantaneous") or at a syllabic rate.

In ADM, the adaptation can be considered equivalent to multiplication or division of the audio signal by the step-size. It is well known from modulation theory that the act of multiplying or dividing an analog signal by another signal will cause the resulting product signal to include modulation sidebands which contaminate the original analog signal. In an ADM encoder the digital output is a representation of this product signal. In order to eliminate these modulation sidebands and to reconstruct the original audio signal from the digital representation, a complementary process must be performed in the adaptive delta-demodulation, that is another multiplication or division. It is apparent that to reconstruct the audio perfectly, the multipliers or dividers in the encoder and decoder need to be 'perfect' (or at least identically imperfect) and the multiplicative signals must also be precisely equal. The mismatch inherent in real circuits will result in the reconstructed audio having a spectrum differing from the original. The frequencies of the spectral difference will depend on the spectrum of the modulating or control signals, and the amplitude of the differences will depend on the magnitude of the circuit mismatches.

In ADM systems employing instantaneous or near-instantaneous adaptation, the adaptation is usually output controlled (operating from the output bit stream). The control signals of such systems have spectral components ranging from D.C. to above the sampling frequency so that the systems may have acceptable performance for coding transient signals. However, during digital transmission, some individual control bits of such control signals will become much more significant than other bits, so that a small percentage of errors in transmitting the wide band control signals (caused for example by a random or burst error) which happen to hit these critical control bits will cause the received control signals to deviate significantly from their proper values. Because of such errors, the magnitude of the spurious spectral components in the received audio can become very large even if the circuits are perfect.

It is a characteristic of human hearing that spurious spectral information is much less audible if it is close in frequency to the desired audio signal. If the spurious energy lies far from the desired audio signal it is much more likely to be audible.

With an ADM system, the tolerance of the control signal tracking (encoder and decoder) and the multiplier precision can be relaxed somewhat if the spectrum of the control signal is constrained to contain only low frequency information. This is because a low frequency modulating signal produces new frequencies which are close to the original audio frequencies, and we can tolerate some of these new

frequencies in the decoded output since they will be masked by the audio signal.

Adaptation with relatively slow control signals is known as syllabic adaptation. A syllabic ADM system is much more appropriate for low cost high quality audio applications for the reasons mentioned above. Such a system is also more resistant to errors in transmission of the control signal since the audible effects will be less. However, reduction of control information bandwidth will cause the step-size control signal to be delayed relative to the analog input signal. Thus, the analog input signal will reach the A-D converter before the converter has completed or even started its adaptation in accordance with the control signal. In a high quality audio system, the bandwidth of the control signal cannot be narrower than a few kHz without causing noticeable or even intolerable distortion in the reproduced audio.

Syllabically adaptive delta modulation modifies the quantizing step-size to accommodate the time derivative or slope of the incoming signal. In an ideal syllabic ADM design, the step-size at each instant will be only slightly greater than the minimum needed thereby giving a minimum quantizing error and the best signal to noise ratio. However, to achieve comparable quality, even an ideal ADM system requires higher bit rates than a PCM system. If the bit rate of an ADM system is reduced to one comparable with that required for a PCM system, the noise modulation is unacceptable. The audibility of noise modulation accompanying low and middle frequency audio signals can be reduced by the use of fixed pre-emphasis and deemphasis. However, this is done only at the expense of increased noise modulation when the audio signal contains significant high frequencies. The increased noise modulation is particularly disturbing for low frequency noise in the presence of predominantly high frequency signals.

Conventional syllabically adaptive delta modulation systems with limited adapting bandwidth (slow response time) suffer from transient distortion. Because of the limited adapting bandwidth the system is in slope overload during the time required to respond to a sudden increase in signal level. While ADM systems which suffer brief transient distortion may be acceptable for communication purposes since speech intelligibility may be unaffected, such distortions cannot be tolerated for many applications, such as high quality audio.

The starting point of the present invention is thus an encoder as defined in the pre-characterizing part of claim 1 and known from US-A 3 497 624. This reference relates to a system in which changes in step size are made rapidly and thus suffers from the disadvantages of instantaneously adaptive coders, as discussed above.

One object of the present invention is to provide an A-D encoder which can combine absence of transient distortion with reduced noise modulation. A further object is to provide a D-A decoder for use with the encoder. The encoder and decoder are defined in claims 1 and 19 respectively.

The use of a delay circuit to compensate for the delay of a control signal smoothing circuit is known per se in other contexts. US-A 4 169 219 suggests this in relation to the control signal for a variable gain compressor or expander circuit. The present invention resides in the appreciation that suitably severe bandwidth limitation can render the control signal non-critical, and that delay of the signal to the converter to compensate for such limitation. Some mismatch between the timings of control signals in complementary encoders and decoders can be tolerated. The control signal can be transmitted so that the step-size deriving circuit is needed only in the encoder. The received control signal is subject to error (e.g. bit errors) but will nevertheless control the decoder satisfactorily because it is bandwidth limited therein. Moreover, as will be shown below, the decoder can be further simplified by effectively placing all delay circuits in the encoder.

US-A 3 631 520 describes an adaptive predictive coder in which the samples to be coded are delayed before the error signal which is coded to form the output is formed from the difference between the delayed samples and the output of an adaptive predictor. A computer generates various parameters controlling the predictive coding (duration of a pitch period of the applied signal, a gain factor to be applied to the error signal, etc.). These parameters are updated every 5 ms. The delay is provided to allow the time needed for computation so that the new parameters are ready ahead of the time at which they are needed. This known coder is not a syllabic device.

In particular, the decoder decodes a digital signal received from an encoder through a transmission medium where the digital signal includes the digital representation of an analog signal and step-size information, and the analog signal has been encoded in the encoder in accordance with the step-size information. The decoder may comprise means for bandwidth limiting the step-size information and converter means responsive to the digital representation of the analog signal and the bandwidth limited step-size information for generating an analog output signal. Thus the effect of uncorrected errors in step-size transmission is reduced. Preferably the step-size information is received by the decoder in advance of the corresponding digital representation of the analog signal by a predetermined, substantially fixed time interval. This compensates for the delay inherent in the bandwidth limitation of the step-size information in

the decoder, without the need for a delay circuit in the decoder.

Brief Description of the Drawings

Fig. 1 is a graphical illustration of the noise and distortion emerging from an ADM coder-decoder as a function of the step-size applied by the coder-decoder.

Fig. 2A is a block diagram for an encoder illustrating an embodiment of this invention.

Fig. 2B is a block diagram of a decoder illustrating the preferred embodiment of this invention.

Figs. 3A and 3B are graphical illustrations of respectively the pre-emphasis characteristics of the pre-processing circuit of Fig. 2A and the de-emphasis characteristics of the post-processing circuit of Fig. 2B.

Fig. 4 is a block diagram illustrating the preferred embodiment for a portion of the encoder of Fig. 2A.

Fig. 5 is a block diagram of a decoder containing the system definition of the decoder to illustrate the preferred embodiment of the invention.

Fig. 6 is a schematic circuit diagram for the circuit of Fig. 5 to illustrate the invention.

Detailed Description of the Preferred Embodiment

The noise and distortion emerging from an ADM encoder-decoder system (codec) depend on the audio input signal and the step-size, both of which are varying. Consider a codec handling a single sine wave. As a function of step-size, the output noise and distortion will vary as shown qualitatively in Fig. 1. In the region labelled A, the step-size is too large, which produces excessive quantizing noise. In region B the step-size is too small and the system is in overload which produces high noise and distortion. There is an optimum value of step-size for the particular input condition labelled C. For each short time segment of real audio there is a curve like that of Fig. 1, and an optimum step-size. In a conventional output controlled ADM system the step-size rarely achieves the optimum value, but remains in region A most of the time, moving into region B on signal transients. The object of this invention is to design an ADM system that operates as much as possible in region C, and that operates so that the delta modulator is fully loaded. This is possible because the step-size determination is done in the encoder and is input controlled as explained below.

Fig. 2A is a block diagram for an encoder illustrating an embodiment of this invention. As shown in Fig. 2A, an analog audio input signal 12 is passed through a low-pass filter 14 to determine the overall audio bandwidth of the analog input signal. Typically such bandwidth may be 15 kHz. The analog input signal is then passed through a pre-processing circuit 16 which is the subject of the companion application. The function of the pre-processing circuit 16 will be discussed below.

After being pre-processed the analog audio input signal is supplied to a step-size derivation circuit 18 and to a delay circuit 20. In one particular application the step-size derivation circuit 18 comprises a slope detector for detecting the time derivative or slope of the incoming audio input signal. The slope detector then generates a control signal indicative of the step-size to be used in the adaptive delta modulator 22. The control signal is limited by a bandwidth limitation circuit 24 and then applied to the adaptive delta modulator 22. A-D converter 26 converts the step-size control signal into a bit-stream of digital signals to convey step-size information. After being time delayed by delay circuit 20 the audio input signal is converted into a bit-stream of digital audio signals by adaptive delta modulator 22 in accordance with the step-size indicated by the bandwidth limited step-size control signal 45. The audio bit-stream and the step-size information bit-stream are then transmitted through a medium to a decoder which is shown in Fig. 2B. In one particular application encoder 10 is part of a broadcasting station transmitting the audio and step-size information bit-streams to decoders in consumer systems. The function of delay circuit 20 and bandwidth limitation circuit 24 will be discussed after a brief description of the decoder of Fig. 2B below.

Fig. 2B is a block diagram of a decoder illustrating the preferred embodiment of this invention. As shown in Fig. 2B decoder 40 comprises an adaptive delta demodulator 42 for receiving the digital audio bit-stream 30 transmitted through the medium and a D-A converter 44 for receiving the digital step-size information bit-stream 28. D-A converter 44 converts the digital bit-stream into an analog step-size control signal which is supplied to bandwidth limitation circuit 46. After being limited in bandwidth, the step-size control signal is applied to adaptive delta demodulator 42. Adaptive delta demodulator 42 generates an analog audio output signal from the audio bit-stream in accordance with bandwidth limited step-size control signal from bandwidth limitation 46. Bandwidth limitation circuit 24 of Fig. 2A limits the bandwidth of the step-size control signal applied to adaptive delta-modulator 22 so that the step-size cannot change abruptly from one sample to the next. Similarly, bandwidth limitation circuit 46 limits the bandwidth of the step-size control signal applied to adaptive delta-demodulator 42. Thus if the transmission medium introduces a bit error in the step-size information bit-stream, such an error, after being converted into analog form by D-A

converter 44, cannot introduce a major error in the step-size at adaptive delta demodulator 42. The effect of transmission errors is thereby reduced. Therefore, cheap non-precision components may be used to construct the converters 26, 44 and the transmission of the step-size information bit-stream is highly tolerant of bit errors.

5 The generation of a limited bandwidth step-size control signal will require a finite time. To compensate for such time, delay circuit 20 introduces a time delay so that the pre-processed analog audio input signal will reach adaptive delta modulator 22 at a time when the step-size control signal for such input signal is available from bandwidth limitation circuit 24. This is particularly advantageous when there are sudden changes in the slope of the input audio signal.

10 While in Figs. 2A and 2B the step-size information bit-stream 28 and audio bit-stream 30 are shown as being transmitted separately, it will be understood that the two bit-streams may be transmitted together in one single channel provided that the two bit-streams can be distinguished from each other. All three bit-streams 28, 30 and 82 may be transmitted in the same channel instead of in separate channels if they can be distinguished from each other.

15 By introducing a time delay through delay circuit 20 that also compensates for the time delay caused by the bandwidth limitation circuit 46 in the decoder, the audio bit-stream signals which are the digital representation of a particular analog signal reach the delta demodulator when the bandwidth limited step-size control signal is available from circuit 46. In such manner, the need for a delay circuit in the decoder to compensate for the time delay caused by the bandwidth limiting of the step-size control signal in the decoder is eliminated and the decoder circuit is simplified. This is particularly advantageous for lowering the cost of consumer decoder equipment.

20 The following discussion on the pre-processing circuit 16 and other associated circuit components is taken from our companion application entitled "Spectral Emphasis and De-emphasis Circuits". Since the step-size in the A-D and D-A conversions is variable, the noise amplitude will be modulated depending on the step-size and such noise modulation is undesirable in many applications such as in high quality audio equipment. To reduce noise modulation the above referenced application by Kenneth Gundry and Craig Todd discloses a technique embodied by pre-processing circuit 16 and post-processing circuit 96, combined with circuit components A-D converter 72 and digital delay 74 of Fig. 2A. The pre-processing circuit 16 comprises spectral analysis circuit 52, bandwidth limitation circuit 54, adaptive pre-emphasis circuit 56, and delay circuit 58, all of Fig. 2A. The post-processing circuit 96 comprises D-A converter 76, adaptive de-emphasis circuit 78 and bandwidth limitation circuit 80, all of Fig. 2B.

25 Spectral analysis circuit 52 analyzes the audio input signal to generate an emphasis control signal. The emphasis control signal generated is a function only of the spectrum of the input audio and is substantially independent of the amplitude of the input audio. The emphasis control signal is then limited by bandwidth limitation circuit 54 and applied to adaptive pre-emphasis circuit 56. Adaptive pre-emphasis circuit 56 boosts or boosts and bucks the different frequency components of the input audio signal by amounts which are functions of the emphasis control signal. The emphasis control signal is limited in bandwidth so that the frequency response of the adaptive pre-emphasis circuit 56 will not change suddenly from sample to sample. Bandwidth limitation circuit 80 reduces the effect of bit errors introduced by the transmission medium in a manner similar to bandwidth limitation circuit 46 described above.

30 In reference to Figs. 2A, 2B, delay circuit 58 introduces a time delay which permits the pre-emphasis circuit 56 to complete its adaptation before the audio input signal is supplied to the pre-emphasis circuit 56. The pre-processed audio input signal is supplied to delay circuit 20 and adaptive delta modulator 22 as described above. The emphasis control signal from spectral analysis circuit 52 is converted into a digital bit-stream carrying spectral information by A-D converter 72 and is delayed by digital delay 74 by a time period substantially equal to that of delay circuit 20.

35 Comparing the timing relationship of the audio and the spectral information bit-streams, an audio signal in the audio bit-stream has been delayed by delay circuits 58, 20, whereas the corresponding spectral information signal for such audio signal has been delayed by only the digital delay 74. Thus the net effect is that the audio is delayed relative to the corresponding spectral information by the time delay caused by delay 58, so that the spectral information reaches the decoder of Fig. 2B and the post-processing circuit 96 in advance of the corresponding audio signals and at the proper time to change the amplitudes of the various frequency components of the audio signal in a manner complementary to that of the adaptive pre-emphasis circuit 56. The further requirements for complementarity are discussed below. The time delay introduced in the encoder by circuit 58 compensates for the time delay caused by bandwidth limiting the spectral information in bandwidth limitation circuit 80 in the decoder.

40 If the audio and the corresponding spectral information were synchronous so that they reached the decoder and the post-processing circuit at the same time, the time delay caused by bandwidth limitation

circuit 80 would cause the audio to reach the adaptive de-emphasis 78 before the bandwidth limited de-emphasis control signal was available for controlling the de-emphasis. A delay circuit would then be required in the decoder to delay the audio so that the audio would reach the de-emphasis 78 at the appropriate time. By introducing a timing discrepancy between the audio and the corresponding spectral information in the encoder in the manner discussed above, the need for a delay circuit in the decoder equipment is eliminated and the cost of the decoder is reduced.

One of the purposes of the encoder-decoder system of Figs. 2A and 2B is to transmit an analog audio signal through a medium so that the analog audio output signal recovered after the transmission is substantially the same as the input audio. To accomplish this purpose, the adaptive delta modulator 22 in the encoder of Fig. 2A and the adaptive delta demodulator 42 are substantially complementary to each other. In addition, the step-size control signals applied to the modulator 22 and demodulator 42 are substantially the same and are applied to the modulator and demodulator with substantially the same timing relationship with respect to the corresponding audio signals so that the modulation and demodulation applied are complementary. In other words, if the step-size control signal for an audio signal is applied at a time t before or after the audio signal reaches the modulator 22, the step-size control signal should reach the demodulator 42 also at substantially time t before or after the audio signal reaches the demodulator. This assures that the modulation and demodulation applied are substantially complementary. Similarly, the pre-processing and post-processing circuits are also substantially complementary to each other; the emphasis and de-emphasis control signals are substantially the same and have substantially the same timing relationship with respect to the audio for the application of pre-emphasis and de-emphasis so that the pre-emphasis and de-emphasis applied are substantially complementary.

After the above requirements for complementarity are generally met, however, the encoder-decoder system is highly tolerant of timing errors. Since the step-size, pre-emphasis and de-emphasis control signals can only change slowly in the encoder and decoder, the adaptive modulation and demodulation together with the pre-emphasis and de-emphasis applied by the encoder and decoder can only change slowly. Thus mismatch in timing relationship of the type explained above and of the order of a few percent of the bandwidth limitation rise times will not cause the modulation and demodulation to deviate significantly from being complementary. Similarly mismatch in timing relationship of such order of magnitude will not cause the pre-emphasis and de-emphasis applied to deviate significantly from being complementary.

The characteristics of adaptive pre-emphasis and de-emphasis circuits 56, 78 are illustrated in Figs. 3A, 3B. It will be understood that the specific frequencies and gains in Figs. 3A, 3B and in the discussion below are for illustrative purposes only and that the characteristics of circuits 56, 78 are not limited thereby. In some respects, the pre-emphasis and de-emphasis characteristics are similar to the well known type of "sliding band" circuits, which reduce high frequency noise by way of a filter with a variable corner frequency. As the signal level increases, the filter corner frequencies of such "sliding band" circuits slide continuously and upwardly to narrow the band boosted and cut. Examples of such circuits are found in US-PS Re 28,426; US-PS 4,072,914 and US-PS 3,934,190.

The pre-emphasis characteristic of circuit 56 also has a variable frequency indicated at 86a, 88a, 90a, 92a, 94a and 96a of the pre-emphasis characteristic curves 86, 88, 90, 92, 94 and 96 respectively of Fig. 3A. The de-emphasis curves 84'-96' of Fig. 3B are complementary to curves 84-96 respectively and also have variable frequencies 86a'-96a'. Such variable frequencies also continuously shift as a function of the input audio. However, unlike the "sliding band" circuits, the continuous shifting is determined, not by the level of high frequency signals but by the spectral content of the input audio in a manner described below. In the above referenced "sliding band" circuits, the signal components with frequencies higher than the variable corner frequency are boosted (or cut) and those with frequencies lower than the corner frequency remain unchanged. While signals with frequencies higher than the variable frequency are also boosted by circuit 56 as shown in Fig. 3A, for each of curves 90 through 96, there is a spectral region in which signals are bucked. Similarly there is a spectral region for each of de-emphasis curves 90'-96' in which signals are boosted. The detailed characteristics of circuit 56 are described below.

It is assumed first, for the purpose of discussion, that the predominant signal components of the input audio are concentrated in a certain region of the frequency spectrum. When the audio input signal comprises mostly low and middle frequency energy e.g. concentrated in the frequency region below 500 Hz, adaptive pre-emphasis circuit 56 adopts the response labelled 84, boosting only signals with frequencies above 500 Hz; the predominant signals with frequencies below 500 Hz remain substantially unchanged. When the audio signal from the adaptive delta-demodulator 42 reaches adaptive de-emphasis circuit 78 the high frequency components of the quantizing noise will be reduced by adaptive de-emphasis circuit 78 which will have a characteristic 84' complementary to curve 84 as shown in Figs. 3A and 3B. High frequency noise above 500 Hz is thereby reduced sufficiently that audible noise modulation becomes much

diminished. Low and medium frequency noise below 500 Hz is masked by the signal.

As the frequency of the input audio signal rises so that the predominant signal components are concentrated between about 500 Hz and 2 kHz, the emphasis control signal from the spectral analysis circuit 52 causes the frequency response of adaptive pre-emphasis circuit 56 to slide from 84 to 86 or 88. Such dynamic action of the adaptive pre-emphasis circuit prevents undesirable increases in the step-size of the adaptive delta-modulator but still allows the subsequent complementary de-emphasis to reduce noise at frequencies above those of the input signal. Low frequency noise is not yet an audible problem.

The frequency responses of the shape 84, 86, 88 (that is, sliding high frequency boost) are satisfactory for noise reduction when the predominant spectral components of the input audio signal are below 2 or 3 kHz. Noise at frequencies above these predominant spectral components is reduced as described above; lower frequency noise is masked by the signal. When the predominant spectral components of the input audio signal are at high frequencies (e.g. above 3 kHz) such sliding boost responses may no longer be satisfactory for noise reduction, since low and medium frequency noise is no longer masked by the signal. Under these signal conditions the effect of high frequency boost would be to increase the step-size employed in the adaptive delta modulator 22 and demodulator 42, resulting in an increase in wide-band quantizing noise. The subsequent complementary high frequency cut would not reduce the low frequency part of this increased noise. Thus low frequency noise would be modulated by changes in the high frequency components of the input audio signal. Under such conditions, it is desirable to convert the high frequency boost of adaptive pre-emphasis circuit 56 for the spectral region where the predominant signal components of the input audio are concentrated into a cut such as the dips shown as portions 90b, 92b, 94b, 96b of respective curves 90, 92, 94 and 96 in Fig. 3A. Therefore, as the frequencies of the predominant spectral components of the input audio signal rise, the frequency response of adaptive emphasis circuit 56 will slide past the curves 84, 86 and 88 to curves 90, 92, 94 and 96.

When the predominant signal components are concentrated in high frequencies such as around 5 kHz, high frequency noise around 5 kHz is masked. Noise at still higher frequencies may not be masked and it may be desirable to reduce such noise while also reducing low frequency noise in the manner described above. Thus the curves 90, 92, 94 and 96 at frequencies above the variable frequency retain the shape of a high frequency shelf. The complementary de-emphasis curves 84'-96' corresponding to respective pre-emphasis curves 84-96 are shown in Fig. 3B, and have variable frequencies 86a'-96a' which are substantially the same as those of the pre-emphasis curves. De-emphasis curves 90'-96' have peaks 90b'-96b' corresponding to dips 90b-96b of the pre-emphasis curves of Fig. 3A.

The overall effect of the curves 90-96 can now be described. Pre-emphasis curves with dips at the spectral regions of the predominant signal components will reduce the step-size and hence the broad-band noise emerging from the encoder-decoder system. The subsequent de-emphasis peaks 90b', 92b', 94b' and 96b' will pick out the wanted predominant signal components and restore them to their original amplitudes. The de-emphasis will also buck the signals at frequencies above the variable frequencies to reduce very high frequency noise. Thus the reduced low frequency noise level is retained, high frequency noise is masked and very high frequency noise is reduced.

In the above discussion, it has been assumed that the predominant signal components of the input audio are concentrated in a certain region of the frequency spectrum. Such an input signal is in fact the most critical case. When the signal spectral components are more distributed, their masking properties cover more of the noise, and the shapes of the pre-emphasis curves are less critical. If the signal spectral components are distributed in two regions of the frequency spectrum, the pre-emphasis curve will resemble the curve for the case where the spectral components are concentrated in a region between such two regions.

Bandwidth limitation circuits 24, 46, 54 and 80 limit the step-size and spectral control signals to within bandwidths of a few tens or low hundreds of Hz; hence the control signals can have rise times of a few milliseconds. The delay introduced by delay circuits 20, 58 is therefore chosen to be substantially equal to the rise times of the control signals as determined by the bandwidth limiting. Suitable values are in the range 5 to 20 milliseconds. The control A-D and D-A converters 26, 44, 72 and 76 may be simple delta or delta-sigma modulators and demodulators operating at a few kilobits per second. In television sound applications a convenient value is half the horizontal frequency, about 7.8 kHz.

For convenience in instrumentation and better tracking between encoder and decoder, the signal entering bandwidth limitation 24 in the encoder 10 may be derived from the information bit-stream 28 instead of the output of step-size derivation 18. Such a configuration is illustrated in Fig 4, with adaptive delta modulator 22, limitation circuit 24 and A-D converter 26 rearranged as shown. A local D-A converter 100 converts the digital step-size information bit-stream 28 into an analog step-size control signal. In reference to Fig 4, where the A-D converter 26 uses delta-sigma modulation and the local D-A converter

100 is already contained within the A-D converter, no extra local D-A converter 100 will be necessary. Similarly the spectral analysis information supplied to adaptive pre-emphasis circuit 56 may be derived from the spectral information bit-stream 82 before delay is introduced by delay circuit 74. This is again advantageous if A-D converter 72 uses delta-sigma modulation.

5 Instead of using a bandwidth limiting circuit 46 for limiting the bandwidth of step-size control signal applied to the adaptive delta-demodulator, D-A converter 44 may contain the bandwidth limitation. Similarly, bandwidth limitation circuit 80 may be eliminated if D-A converter 76 is similarly bandwidth limited.

10 Since it is desirable that the effect of a bit error should be a gain error of similar logarithmic magnitude for both large and small step-sizes, it is preferable to design the A-D converter 26 and D-A converter 44 so that the digital bit-stream 28 conveys the logarithm of the step-size. Similarly, the spectral information bit-stream preferably conveys the logarithm of the spectral information. In embodiments in which logarithmic and exponential circuits are inconvenient, it may be more practical to convey some other non-linear function of the step-size, such as the square root or the cube-root; such functions will not give perfectly uniform gain errors over the dynamic range of the system, but the extent of the variation will be much less than that

15 resulting from a linear function.

For the same reasons discussed above for transmission of audio information, it is desirable to design an encoder-decoder system which conveys step-size information and spectral information at low bit rates of transmission and which can be implemented at low cost. In choosing the scheme for A-D and D-A conversion for converters 26, 44, 72 and 76 it is desirable to choose one that allows a low bit rate for the transmission of step-size information. Preferably, such bit rate is small compared to the bit rate for transmission of audio data. The A-D or D-A conversion performed in converters 26, 72 and 44, 76 can be one of many schemes, including PCM, delta modulation or delta-sigma modulation. While a PCM system requires a low bit rate, expensive converters must be used so that it is undesirable to use PCM in the converters. Delta-sigma modulation requires a somewhat higher bit rate (on the order of 5 to 10 kbit/sec)

20 than PCM but it can be implemented simply and at low cost. Furthermore, the bit rate required for delta-sigma modulation is still low compared with the bit rate for the transmission of audio data (on the order of 200 to 300 kbit/sec). Therefore, delta-sigma modulation is used in the preferred embodiment discussed below. A description of delta-sigma modulation can be found in Delta Modulation Systems, Pentech Press Limited, London, 1975 by Raymond Steele.

30 Fig. 5 is a block diagram for a decoder system illustrating the preferred embodiment of the invention; the characteristics of most of the circuit blocks are defined for the system in Fig. 5. The system is particularly suitable for consumer use. The adaptive delta demodulator or audio decoder 42 comprises a pulse height modulator 202 and a leaky integrator 204. Pulse height modulator 202 multiplies the step-size control signal V_{ss} by +1 or -1 in accordance with the audio data bit stream, and supplies the result to the leaky integrator 204. The leak time constant may be approximately 0.5 milliseconds which corresponds to a cut-off frequency of approximately 300 Hz. The integrator integrates the resulting signal to produce an analog audio signal. At frequencies below the frequency corresponding to the leak time constant, the system is strictly not delta but delta-sigma modulation.

35 In reference to Fig. 2A, the adaptive delta modulator 22 also includes a leaky integrator (not shown) with a cut-off frequency which is about the same as the one in the decoder. The step-size derivation means 18 may be a slope detector which responds to the pre-processed input audio signal by deriving a control signal indicative of the slopes of the signal components of the audio input with frequencies above the cut-off frequency and the amplitudes of the signal components with frequencies below the cut-off frequency.

40 In the preferred embodiment, the step-size or slope data are transmitted by delta-sigma modulation and in the form of the logarithm of the required step-size or slope. The slope data are therefore decoded in the slope decoder 205 by passage through a low pass filter 206 (corresponding to D-A converter 44 and bandwidth limitation 46 of Fig. 2B), which determines the bandwidth (and hence the rise-time) and ripple of the slope voltage. In the preferred embodiment, a 3-pole low pass filter is employed which causes the step-size control signal V_{ss} to have a rise time of about 10 milliseconds corresponding to a bandwidth of about

45 50 Hz. The slope voltage is then applied to an exponentiator 208 or anti-log. circuit, which may be, for example, a bipolar transistor. If the normalized mean level of the bit stream (or the duty-cycle measured over the rise-time of the low pass filter) is written as y , then

$$V_{ss} = V_o \exp ky$$

55 where V_o and k are constants suitable for the particular implementation

If a practical value of k is $10 \ln 2$, this definition gives an increase of 6 dB in step-size for every increase of 0.1 in y . Since y is confined to a range of 0 to 1, the resultant maximum possible range of V_{ss} is 60 dB.

The transmission of slope information in logarithm form reduces the dynamic range conveyed in the slope data bit-stream from about 50 dB to about 19 dB, and spreads the effect of bit errors more uniformly across the dynamic range. Since Vss is confined by the low pass filter 206 to a bandwidth of about 50 Hz, bit errors lead to slow random amplitude modulation of the output audio. The audible disturbance produced by errors in the slope data bit-stream may be negligible. It has been observed that uncorrected bit error rates of up to 1 in 100 or so produce nearly imperceptible disturbance of music or speech.

The low pass filter thus converts the digital slope data into analog data and limits its bandwidth. Low pass filter 206 therefore performs both the functions of both the D-A converter 44 and bandwidth limitation 46 of Fig. 2B. In reference to Figs. 2A, 2B and 5, delay means 20 introduces such delay that the slope data are received by filter 206 before the corresponding audio data are received by the pulse height modulator 202. Such time difference compensates for the rise time of about 10 milliseconds of Vss. In such manner, the need for a delay circuit in the decoder is eliminated.

Fig. 3B illustrates a set of de-emphasis curves which are complementary to those of the pre-emphasis curves of Fig. 3A. There are many ways to synthesize responses of this nature. The sliding band de-emphasis 78 defined in Fig. 5 shows one practical implementation of the de-emphasis characteristic. The system definitions for all the circuit blocks in Fig. 5 together with one set of values of the constants giving satisfactory results are listed below:

leaky integrator 204

$$\frac{1}{1 + sT_o}$$

3-pole L.P. filter 206, 214

$$\left(\frac{1}{1 + sT_4} \right)^3$$

exponentiator 208
(slope decoder)

$$V_o \exp ky$$

exponentiator 216
(spectrum data)

$$f_o \exp kx$$

sliding band de-emphasis 78

$$\left[\frac{10sT_1}{1+sT_1} + \frac{1+sT_2}{1+sT_3} \right]^{-1}$$

fixed de-emphasis 118

$$\frac{1}{1+sT_5}$$

s is the complex frequency

$T_o = 0.5$ milliseconds

T_1 is variable so that the variable frequency of the sliding band de-emphasis f_1 is given by:

$$f_1 = 1/(2\pi T_1) = f_o \exp kx$$

$T_2 = 5$ microseconds

$T_3 = 50$ microseconds

$T_4 = 2$ milliseconds

$T_5 = 25$ microseconds

$f_0 = 4$ kHz

5 V_0 is scaling factor to suit the design of the audio decoder.

x and y are the normalized mean levels of their respective bit-streams, i.e. the proportion of 1's measured over the smoothing time of the 3-pole L.P. filter.

$k = 10 \ln 2 = 6.93$

10 The spectrum decoder 212 comprising 3-pole filter 214 and exponentiator 216 is substantially the same as the slope decoder. It finds the normalized mean level x of the spectrum data input which conveys the logarithm of the variable frequency of the desired sliding band de-emphasis f_1 defined above, f_1 being different from the variable frequencies 86a-96a, 86a'-96a' of Figs. 3A, 3B. The spectrum decoder generates the exponent or anti-log. of the mean level and applies the resulting voltage or current to the sliding band de-emphasis 78. The emphasis control signal is even less affected by bit errors in transmission than the
15 slope data control signal.

In delta modulation systems the sampling frequency is vastly greater than the minimum required by information theory. Non-audio spectral components in the output are at frequencies well above the audio band and only an elementary low pass filter such as filter 118 is necessary.

20 Fig. 6 is a schematic circuit diagram showing a possible implementation of the system of Fig. 5. As shown in Fig. 6, the sliding band de-emphasis circuit 78 employs a main path 78a with fixed characteristics in parallel with a further path 78b with variable characteristics. The variable characteristics of the further path are controlled by the resistance of a variable resistance 252, which in turn is controlled by the emphasis control signal from spectrum decoder 212. There is no systematic compression or expansion of the dynamic range; the further path is controlled ultimately by the spectrum of the input audio.

25 In reference to Fig. 2B, by limiting the bandwidths of the step-size and emphasis control signals, the characteristics of the delta demodulator 42 and de-emphasis 78 can only change slowly. Because they have slowly changing characteristics, the delta demodulator and de-emphasis are thereby rendered linear or quasi-linear. It makes little difference whether the demodulation is performed ahead of the de-emphasis or vice versa. This linear or quasi-linear feature of the decoder system is even clearer in the case of the
30 preferred embodiment in Fig. 5. Four processes are performed on the audio bit stream: pulse height modulation, leaky integration, sliding band de-emphasis and fixed de-emphasis. All four are linear or quasi-linear processes so that they can be performed in any order.

In Fig. 5, the pulse height modulator 202 can be a relatively simple circuit since it is required only to switch the sign of voltage V_{ss} depending on the state of the audio bit-stream. Thus the modulator 202 may
35 be made at low cost for consumer decoders.

However, multiplying the audio data by the step-size control signal at a different point, say after sliding band de-emphasis but before fixed de-emphasis, may have the advantage that quality of the audio output is improved. This may be desirable for applications such as in broadcast stations and other professional equipment. While the multiplication will have to be performed by a circuit more complex and therefore
40 costlier than the type of pulse height modulator adequate for the arrangement of Fig. 5, the improvement in quality for professional applications may be well worth the additional cost. Multiplying the audio data at a different point is permissible because the four processes are effectively linear as explained above. All such possible arrangements of the four processes are within the scope of this invention.

45 Instead of using a single 3-pole filter in the slope and spectrum decoders 205, 212, it is possible to use a two pole filter instead if an additional single pole filter is used to filter the output of exponentiators 208, 216. Thus the filtering can be split into two steps: one before the exponentiation and the other one after. Any arrangement of filters may be used as long as the filter for filtering the slope or spectrum data before the exponentiation restricts the ripple in the filter output to a few percent of its mean value.

This invention together with the invention of the companion application referenced above reduce the
50 transmission bit rate of the audio bit-stream to that comparable with or somewhat less than the bit rate required for a companded PCM system with comparable performance. The transmission bit rates for the encoder-decoder system of this invention may be in the region of 200 or 300 kbit per second. The transmission of spectral and step-size information may require about 10 or 20 kbit per second and does not add significantly to the total transmission bit rate required for the encoder-decoder system of this invention.

55 The encoder-decoder system of Figs. 2A and 2B, however, retains the advantages of delta modulation systems. The invention reduces and in many applications eliminates disturbing effects of bit errors. It and its components have high tolerance of errors. The receiving equipment (decoder) is inexpensive. The system is efficient in usage of channel capacity so that more excess capacity will exist for flexibility to add

additional channels or more bandwidth will be available to other signals such as video signals. The transmission equipment (encoder) does not require special attention or require the use of non-complementary signal processing.

It will be apparent to those skilled in the art that the principles described herein are applicable not only to adaptive delta-modulation, but to other adaptive A-D and D-A coding systems, such as delta-sigma modulation, double integration delta-modulation, and PCM systems with variable reference voltages.

While the invention has been described for the processing and transmission of audio signals, it will be understood that it may be used for the processing and transmission of other signals as well.

10 Claims

1. An encoder for converting an analog input signal to a digital signal, comprising a step-size circuit (18) for deriving, from the analog input signal, a control signal with a restricted bandwidth and indicative of a continuously variable conversion step-size, and a first converter (22) for converting the analog input signal to a digital signal, the converter being responsive to the control signal so that the digital signal will be generated in accordance with the variable step-size, characterised by compensation means to compensate for the slow rise time of the control signal caused by its restricted bandwidth and comprising a delay circuit (20) to introduce a time delay to the analog input signal before it reaches the first converter (22).
2. An encoder according to Claim 1, characterised in that the control signal indicates the step-size required for minimum quantizing error in the first converter (22).
3. An encoder according to Claim 1 or 2, characterised in that the converter (22) is an adaptive delta modulator.
4. An encoder according to claim 3, characterised in that the adaptive delta modulator (22) includes a leaky integrator with a cut-off frequency.
5. An encoder according to claim 4, characterised in that the cut-off frequency is about 300 Hz.
6. An encoder according to claim 4 or 5, characterised in that the step-size circuit (18) is a slope detector which derives the control signal from the slopes of the signal components of the analog input signal with frequencies above the cut-off frequency and from the amplitudes of the signal components of the analog input signal with frequencies below the cut-off frequency.
7. An encoder according to any of claims 1 to 5, characterised in that the step-size circuit (18) is a slope detector.
8. An encoder according to any of claims 1 to 7, characterised in that the step-size circuit (18) includes a bandwidth limitation circuit (24) for limiting the bandwidth of the control signal to the restricted bandwidth.
9. An encoder according to any of claims 1 to 8, further characterised by a second analog to digital converter (26) for converting the control signal into a digital step-size information bit-stream suitable for transmission.
10. An encoder according to claim 9, characterised in that the first converter (22) is responsive to the control signal in analog form and by a digital to analog converter (100) deriving the analog control signal from the step-size information bit-stream.
11. An encoder according to claim 9 or 10, characterised in that the digital step-size information bit-stream represents a non-linear function of the step-size.
12. An encoder according to claim 11, characterised in that the non-linear function is logarithmic.
13. An encoder according to claim 11, characterised in that the non-linear function is the square-root.

additional channels or more bandwidth will be available to other signals such as video signals. The transmission equipment (encoder) does not require special attention or require the use of non-complementary signal processing.

It will be apparent to those skilled in the art that the principles described herein are applicable not only to adaptive delta-modulation, but to other adaptive A-D and D-A coding systems, such as delta-sigma modulation, double integration delta-modulation, and PCM systems with variable reference voltages.

While the invention has been described for the processing and transmission of audio signals, it will be understood that it may be used for the processing and transmission of other signals as well.

10 Claims

1. An encoder for converting an analog input signal to a digital signal, comprising a step-size circuit (18) for deriving, from the analog input signal, a control signal with a restricted bandwidth and indicative of a continuously variable conversion step-size, and a first converter (22) for converting the analog input signal to a digital signal, the converter being responsive to the control signal so that the digital signal will be generated in accordance with the variable step-size, characterised by compensation means to compensate for the slow rise time of the control signal caused by its restricted bandwidth and comprising a delay circuit (20) to introduce a time delay to the analog input signal before it reaches the first converter (22).
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3. An encoder according to Claim 1 or 2, characterised in that the converter (22) is an adaptive delta modulator.
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8. An encoder according to any of claims 1 to 7, characterised in that the step-size circuit (18) includes a bandwidth limitation circuit (24) for limiting the bandwidth of the control signal to the restricted bandwidth.
9. An encoder according to any of claims 1 to 8, further characterised by a second analog to digital converter (26) for converting the control signal into a digital step-size information bit-stream suitable for transmission.
10. An encoder according to claim 9, characterised in that the first converter (22) is responsive to the control signal in analog form and by a digital to analog converter (100) deriving the analog control signal from the step-size information bit-stream.
11. An encoder according to claim 9 or 10, characterised in that the digital step-size information bit-stream represents a non-linear function of the step-size.
12. An encoder according to claim 11, characterised in that the non-linear function is logarithmic.
13. An encoder according to claim 11, characterised in that the non-linear function is the square-root.



14. An encoder according to claim 11, characterised in that the non-linear function is the cube-root.
15. An encoder according to any of claims 9 to 14, characterised in that the second analog to digital converter (26) is a delta-sigma modulator.
- 5 16. An encoder-decoder system for converting an analog input signal to a digital signal and for recovering an analog output signal from the received digital signal, the system comprising a step-size circuit (28) for deriving, from the analog input signal, a first control signal with a restricted bandwidth and indicative of a variable conversion step-size, a first converter (22) for converting the analog input signal to the
10 digital signal, the converter being responsive to the first control signal so that the digital signal will be generated in accordance with the variable step-size, a second converter (42) responsive to the received digital signal and to a second step-size control signal matching the first control signal to generate the analog output signal, characterised by a delay circuit (20) preceding the first converter (22) and compensating for the slow rise time of the first control signal arising by virtue of its restricted
15 bandwidth, and in that the second control signal is derived from the first control signal transmitted along with the said digital signal.
17. An encoder-decoder system according to claim 16, wherein the first and second control signals are in analog form, characterised by means (26) for converting the first control signal into a step-size information bit-stream, and means (44) for converting the received step-size information bit-stream into the second control signal.
18. An encoder-decoder system according to claim 17, characterised by means (46) for restricting the
20 bandwidth of the second control signal and in that the said digital signal is transmitted with a delay relative to the said information bit-stream to compensate for the slow response of the second control signal arising by virtue of its restricted bandwidth.
19. A digital to analog decoder for use in conjunction with an encoder according to claim 1, comprising a
25 converter (42) responsive to the received digital signal and to step-size control information transmitted along with said received digital signal to generate an analog output signal, characterised in that the decoder comprises a deriving circuit (44, 46) for deriving the step-size control signal from said step-size control information for controlling the conversion in converter (42), and in that said circuit includes means (46) imposing bandwidth restriction and hence a slow rise time of the control signal.
- 30 20. A decoder according to claim 19, characterised in that the bandwidth restricting means (46) limit the step-size control signal to such a bandwidth that the converter (42) has substantially linear characteristics.
21. A decoder according to claim 19 or 20, characterised in that the deriving circuit includes a second
35 converter (44) for converting the said information in digital form to an analog control signal which is subject to the bandwidth restriction.
22. A decoder according to any of claims 19 to 21, characterised in that the restricted bandwidth is about 50 Hz.
- 40 23. A decoder according to any of claims 19 to 21, characterised in that the bandwidth restricting means (46) has a rise time which is substantially in the range of 5 to 20 milliseconds.
24. A decoder according to claim 21, characterised in that the second converter (44) includes a low pass
45 filter (206) for restricting the bandwidth of the step-size control signal.
25. A decoder according to claim 24, characterised in that the low pass filter (206) comprises three single pole filters each with a time constant of about 2 milliseconds.
- 50 26. A decoder according to claim 24, wherein the step-size information is in the form of the logarithm of the slope of the analog input signal, further characterised by an exponentiator (208) for exponentiating the bandwidth limited step-size control signal transmitted in logarithm form.
- 55



27. A decoder according to claim 25 and claim 26, characterised in that the low pass filter (206) is arranged so that a two pole filter precedes and a single pole filter follows the exponentiator (208).
28. A decoder according to claim 26, characterised in that the ripple at the input to the exponentiator (208) is restricted to a few percent of its mean level.
29. A decoder according to any of claims 24 to 28, characterised in that the low pass filter (206) also acts as a delta-sigma demodulator for demodulating the received control signal
30. A decoder according to claim 19, 20 or 21, characterized in that the digital signal received by the decoder comprises a single bit stream where the digital signal and the step-size information are transmitted in the bit stream in a manner that allows them to be distinguished from each other.
31. A decoder according to claim 19, 20 or 21, characterised in that the digital signal and the step-size information are transmitted in separate bit streams.
32. A decoder according to any of claims 19 to 21, characterised in that the converter (42) comprises an adaptive delta demodulator.
33. A decoder according to any of claims 19 to 21, characterised in that the converter (42) comprises a delta demodulator and means for changing the level of the output analog signal as a function of the step-size control signal, for generating the analog output signal.
34. A decoder according to claim 33, characterised in that the level changing means adjusts the step-size of the delta demodulator (42) as a function of the control signal.
35. A decoder according to claim 33, characterised in that the step-size applied by the delta demodulator (42) is substantially fixed and wherein the level changing means applies a variable gain to the output of the delta demodulator to modulate the analog output signal level.
36. A decoder according to any of claims 19 to 21, characterised in that the converter (42) includes a leaky integrator (204) and a pulse height modulator (202) responsive to the step-size information to modulate the level of the analog output signal, for generating the analog output signal from the digital representation of the analog input signal.
37. A decoder according to claim 36, characterised in that the leaky integrator (204) has a time constant of about 0.5 ms.
38. An encoder according to claim 1, characterised in that the step-size circuit (18) is such that the first control signal has a rise time of at least about 1 millisecond.

Revendications

1. Codeur pour convertir un signal analogique d'entrée en un signal numérique, comprenant un circuit de valeur de discontinuité (18) pour obtenir, à partir du signal analogique d'entrée, un signal de commande avec une largeur de bande limitée et représentatif d'une valeur de discontinuité de conversion variable en continu, et un premier convertisseur (22) pour convertir le signal analogique d'entrée en un signal numérique, le convertisseur répondant au signal de commande de façon que le signal numérique soit produit en conformité avec la valeur de discontinuité variable,
- caractérisé par un moyen de compensation afin de compenser le lent temps de montée du signal de commande provoqué par sa largeur de bande limitée et comportant un circuit à retard (20) pour introduire un retard pour le signal analogique d'entrée avant qu'il atteigne le premier convertisseur (22).
2. Convertisseur selon la revendication 1, caractérisé en ce que le signal de commande indique la valeur de discontinuité requise pour une erreur de quantification minimum dans le premier convertisseur (22).
3. Codeur selon la revendication 1 ou 2, caractérisé en ce que le convertisseur (22) est un modulateur delta adaptatif.



4. Codeur selon la revendication 3, caractérisé en ce que le modulateur delta adaptatif (22) comprend un intégrateur de fuite avec une fréquence de coupure.
5. Codeur selon la revendication 4, caractérisé en ce que la fréquence de coupure est environ 300 Hz.
- 5 6. Codeur selon la revendication 4 ou 5, caractérisé en ce que le circuit de valeur de discontinuité (18) est un détecteur de pente qui obtient le signal de commande à partir des pentes des composantes du signal analogique d'entrée avec des fréquences supérieures à la fréquence de coupure et à partir des amplitudes des composantes du signal analogique d'entrée avec des fréquences inférieures à la fréquence de coupure.
- 10 7. Codeur selon l'une quelconque des revendications 1 à 5, caractérisé en ce que le circuit de valeur de discontinuité (18) est un détecteur de pente.
- 15 8. Codeur selon l'une quelconque des revendications 1 à 7, caractérisé en ce que le circuit de valeur de discontinuité (18) comporte un circuit (24) de limitation de largeur de bande afin de limiter la largeur de bande du signal de commande à la largeur de bande limitée.
- 20 9. Codeur selon l'une quelconque des revendications 1 à 8, caractérisé en outre par un second convertisseur analogique-numérique (26) afin de convertir le signal de commande en un train de bits numériques d'information sur la valeur de discontinuité pour transmission.
- 25 10. Codeur selon la revendication 9, caractérisé en ce que le premier convertisseur (22) répond au signal de commande sous forme analogique, et par un convertisseur numérique-analogique (100) obtenant le signal analogique de commande à partir du train des bits d'information sur la valeur de discontinuité.
- 30 11. Codeur selon la revendication 9 ou 10, caractérisé en ce que le train des bits d'information sur la valeur de discontinuité numérique représente une fonction non linéaire de la valeur de discontinuité.
- 35 12. Codeur selon la revendication 11, caractérisé en ce que la fonction non linéaire est logarithmique.
13. Codeur selon la revendication 11, caractérisé en ce que la fonction non linéaire est la racine carrée.
14. Codeur selon la revendication 11, caractérisé en ce que la fonction non linéaire est la racine cubique.
- 40 15. Codeur selon l'une quelconque des revendications 9 à 14, caractérisé en ce que le second convertisseur analogique-numérique (26) est un modulateur delta-sigma.
- 45 16. Système de codeur-décodeur pour convertir un signal analogique d'entrée en un signal numérique pour récupérer un signal analogique de sortie à partir du signal numérique reçu, le système comprenant un circuit de valeur de discontinuité (18) pour obtenir, à partir du signal analogique d'entrée, un premier signal de commande avec une largeur de bande limitée et représentatif d'une valeur de discontinuité de conversion variable, un premier convertisseur (22) pour convertir le signal analogique d'entrée en ledit signal numérique, le convertisseur répondant au premier signal de commande pour que le signal numérique soit produit en conformité avec la valeur de discontinuité variable, un second convertisseur (42) répondant au signal numérique reçu et à un second signal de commande de valeur de discontinuité adaptant le premier signal de commande pour produire le signal analogique de sortie, caractérisé par un circuit à retard (20) précédant le premier convertisseur (22) et compensant le lent temps de montée du premier signal de commande dû à sa largeur de bande limitée, et en ce que le second signal de commande est obtenu à partir du premier signal de commande transmis en même temps que ledit signal numérique.
- 50 17. Système de codeur-décodeur selon la revendication 16, dans lequel les premier et second signaux de commande sont sous forme analogique, caractérisé par un moyen (26) pour convertir le premier signal de commande en un train de bits d'information sur la valeur de discontinuité, et un moyen (44) pour convertir le train reçu de bits d'information sur la valeur de discontinuité en ledit second signal de commande.
- 55



18. Système de codeur-décodeur selon la revendication 17, caractérisé par un moyen (46) pour limiter la largeur de bande du second signal de commande et en ce que ledit signal numérique est transmis avec un retard par rapport audit train de bits d'information afin de compenser la lente réponse du second signal de commande due à sa largeur de bande limitée.

19. Décodeur numérique en analogique pour emploi en conjonction avec un codeur selon la revendication 1, comprenant un convertisseur (42) répondant au signal numérique reçu et à l'information sur la commande de la valeur de discontinuité transmise en même temps que ledit signal numérique reçu afin de produire un signal analogique de sortie, caractérisé en ce que le décodeur comprend un circuit d'obtention (44, 46) pour obtenir le signal de commande de la valeur de discontinuité à partir de ladite information sur la commande de la valeur de discontinuité afin de commander la conversion dans le convertisseur (42), et en ce que ledit circuit comprend un moyen (46) imposant une limitation à la largeur de bande et par conséquent un lent temps de montée du signal de commande.

20. Décodeur selon la revendication 19, caractérisé en ce que le moyen (46) de limitation de largeur de bande limite le signal de commande de la valeur de discontinuité à une largeur de bande telle que le convertisseur (42) présente une caractéristique sensiblement linéaire.

21. Décodeur selon la revendication 19 ou 20, caractérisé en ce que le circuit d'obtention comprend un second convertisseur (44) pour convertir ladite information de forme numérique en un signal de commande analogique qui est soumis à la limitation de la largeur de bande.

22. Décodeur selon l'une quelconque des revendications 19 à 21, caractérisé en ce que la largeur de bande limitée est d'environ 50 Hz.

23. Décodeur selon l'une quelconque des revendications 19 à 21, caractérisé en ce que le moyen (46) de limitation de largeur de bande a un temps de montée qui est sensiblement compris dans la plage de 5 à 20 millisecondes.

24. Décodeur selon la revendication 21, caractérisé en ce que le convertisseur (44) comprend un filtre passe-bas (206) pour limiter la largeur de bande du signal de commande de la valeur de discontinuité.

25. Décodeur selon la revendication 24, caractérisé en ce que le filtre passe-bas (206) comprend trois filtres à un seul pôle, chacun avec une constante de temps d'environ 2 millisecondes.

26. Décodeur selon la revendication 24, dans lequel l'information sur la valeur de discontinuité se présente sous la forme du logarithme de la pente du signal analogique d'entrée, caractérisé en outre par un exponentiateur (208) afin de procéder à une exponentiation du signal de commande de la valeur de discontinuité limité en largeur de bande qui est transmis sous forme logarithmique.

27. Décodeur selon la revendication 25 et la revendication 26, caractérisé en ce que le filtre passe-bas (206) est disposé de façon qu'un filtre à deux pôles précède l'exponentiateur (208) et qu'un filtre à un seul pôle le suit.

28. Décodeur selon la revendication 26, caractérisé en ce que le ronflement à l'entrée de l'exponentiateur (208) est limité à quelques pourcents de son niveau moyen.

29. Décodeur selon l'une quelconque des revendications 24 à 28, caractérisé en ce que le filtre passe-bas (206) agit aussi en démodulateur delta-sigma pour démoduler le signal de commande reçu.

30. Décodeur selon la revendication 19, 20 ou 21, caractérisé en ce que le signal numérique reçu par le décodeur comprend un seul train de bits dans lequel le signal numérique et l'information sur la valeur de discontinuité sont transmis dans le train de bits d'une manière telle qu'elle leur permet d'être distingués l'un de l'autre.

31. Décodeur selon la revendication 19, 20, ou 21, caractérisé en ce que le signal numérique et l'information sur la valeur de discontinuité sont transmis dans des trains de bits séparés.



32. Décodeur selon l'une quelconque des revendications 19 à 21, caractérisé en ce que le convertisseur (42) comprend un démodulateur delta adaptatif.

33. Décodeur selon l'une quelconque des revendications 19 à 21, caractérisé en ce que le convertisseur (42) comprend un démodulateur delta et un moyen pour changer le niveau du signal analogique de sortie en fonction du signal de commande de la valeur de discontinuité, afin de produire le signal analogique de sortie.

34. Décodeur selon la revendication 33, caractérisé en ce que le moyen de changement de niveau ajuste la valeur de discontinuité du modulateur delta (42) en fonction du signal de commande.

35. Décodeur selon la revendication 33, caractérisé en ce que la valeur de discontinuité appliquée par le démodulateur delta (42) est sensiblement fixe, et dans lequel le moyen de changement de niveau applique un gain variable à la sortie du démodulateur delta afin de moduler le niveau du signal analogique de sortie.

36. Décodeur selon l'une quelconque des revendications 19 à 21, caractérisé en ce que le convertisseur (42) comprend un intégrateur de fuite (204) et un modulateur (202) de hauteur d'impulsion répondant à l'information sur la valeur de discontinuité afin de moduler le niveau du signal analogique de sortie, pour produire le signal analogique de sortie à partir de la représentation numérique du signal analogique d'entrée.

37. Décodeur selon la revendication 36, caractérisé en ce que l'intégrateur de fuite (204) a une constante de temps d'environ 0,5 ms.

38. Décodeur selon la revendication 1, caractérisé en ce que le circuit de valeur de discontinuité (18) est tel que le premier signal de commande a un temps de montée d'au moins environ 1 milliseconde.

Patentansprüche

1. Codierer zur Umsetzung eines analogen Eingangssignals in ein digitales Signal, umfassend eine Schrittgrößenschaltung (18) zur Ableitung, von dem analogen Eingangssignal, eines Steuersignals mit einer begrenzten Bandbreite, das eine kontinuierlich veränderbare Umsetzungsschrittgröße angibt, und einen ersten Umsetzer (22) zur Umsetzung des analogen Eingangssignals in ein digitales Signal, der auf das Steuersignal anspricht, sodaß das digitale Signal nach Maßgabe der veränderlichen Schrittgröße erzeugt wird, gekennzeichnet durch eine Kompensationseinrichtung zur Kompensation der von seiner begrenzten Bandbreite herrührenden langsamen Anstiegszeit des Steuersignals, die eine Verzögerungsschaltung (20) umfaßt, die das analoge Eingangssignal einer Zeitverzögerung unterzieht, bevor es den ersten Umsetzer (22) erreicht.

2. Codierer nach Anspruch 1, dadurch gekennzeichnet, daß das Steuersignal die Schrittgröße angibt, die für einen minimalen Quantisierungsfehler im ersten Umsetzer (22) erforderlich ist.

3. Codierer nach Anspruch 1 oder 2, dadurch gekennzeichnet, daß der Umsetzer (22) ein adaptiver Deltamodulator ist.

4. Codierer nach Anspruch 3, dadurch gekennzeichnet, daß der adaptive Deltamodulator (22) einen Leckintegrator mit einer Grenzfrequenz aufweist.

5. Codierer nach Anspruch 4, dadurch gekennzeichnet, daß die Grenzfrequenz etwa 300 Hz. beträgt.

6. Codierer nach Anspruch 4 oder 5, dadurch gekennzeichnet, daß die Schrittgrößenschaltung (18) ein Neigungsdetektor ist, der das Steuersignal aus den Neigungen der Signalkomponenten des analogen Eingangssignals mit Frequenzen oberhalb der Grenzfrequenz und von den Amplituden der Signalkomponenten des analogen Eingangssignals mit Frequenzen unterhalb der Grenzfrequenz ableitet.

7. Codierer nach einem der Ansprüche 1 bis 5, dadurch gekennzeichnet, daß die Schrittgrößenschaltung (18) ein Neigungsdetektor ist.



8. Codierer nach einem der Ansprüche 1 bis 7, dadurch gekennzeichnet, daß die Schrittgrößenschaltung (18) eine Bandbreitenbegrenzungsschaltung (24) zur Begrenzung der Bandbreite des Steuersignals auf eine beschränkte Bandbreite enthält.
- 5 9. Codierer nach einem der Ansprüche 1 bis 8, ferner gekennzeichnet durch einen zweiten Analog-Digital-Umsetzer (26) zur Umsetzung des Steuersignals in eine für die Übertragung geeignete digitale Schrittgrößeninformationsbitfolge.
- 10 10. Codierer nach Anspruch 9, dadurch gekennzeichnet, daß der erste Umsetzer (22) auf das Steuersignal in analoger Form anspricht, und durch einen Digital-Analog-Umsetzer (100), der das analoge Steuersignal aus der Schrittgrößeninformationsbitfolge ableitet.
11. Codierer nach Anspruch 9 oder 10, dadurch gekennzeichnet, daß die digitale Schrittgrößeninformationsbitfolge eine nicht-lineare Funktion der Schrittgröße repräsentiert.
- 15 12. Codierer nach Anspruch 11, dadurch gekennzeichnet, daß die nicht-lineare Funktion logarithmisch ist.
13. Codierer nach Anspruch 11, dadurch gekennzeichnet, daß die nicht-lineare Funktion die Quadratwurzel ist.
- 20 14. Codierer nach Anspruch 11, dadurch gekennzeichnet, daß die nicht-lineare Funktion die Kubikwurzel ist.
15. Codierer nach einem der Ansprüche 9 bis 14, dadurch gekennzeichnet, daß der zweite Analog-Digital-Umsetzer (26) ein Deltasigmamodulator ist.
- 25 16. Codier-Decodier-System zur Umsetzung eines analogen Eingangssignals in ein digitales Signal und zur Wiedergewinnung eines analogen Ausgangssignals aus dem empfangenen digitalen Signal, umfassend eine Schrittgrößenschaltung (18) zur Ableitung, aus dem analogen Eingangssignal, eines ersten Steuersignals mit einer begrenzten Bandbreite, das eine variable Umsetzungsschrittgröße angibt, einen ersten Umsetzer (22) zur Umsetzung des analogen Eingangssignals in das digitale Signal, wobei der Umsetzer auf das erste Steuersignal anspricht, so daß das digitale Signal nach Maßgabe der variablen Schrittgröße erzeugt wird, einen zweiten Umsetzer (42), der auf das empfangene digitale Signal und ein zweites Schrittgrößensteuersignal, das an das erste Schrittgrößensteuersignal angepaßt ist, anspricht, um das analoge Ausgangssignal zu erzeugen, gekennzeichnet durch eine Verzögerungsschaltung (20) die dem ersten Umsetzer (22) vorgeschaltet ist und die durch seine begrenzte Bandbreite entstehende langsame Anstiegszeit des ersten Steuersignals kompensiert, und daß das zweite Steuersignal von dem ersten Steuersignal abgeleitet wird, das zusammen mit dem digitalen Signal übertragen wird.
- 30 17. Codier-Decodier-System nach Anspruch 16, bei dem das erste und das zweite Steuersignal analoge Signale sind, gekennzeichnet durch eine Einrichtung (26) zur Umsetzung des ersten Steuersignals in eine Schrittgrößeninformationsbitfolge, und eine Einrichtung (44) zur Umsetzung der empfangenen Schrittgrößeninformationsbitfolge in das zweite Steuersignal.
- 40 18. Codier-Decodiersystem nach Anspruch 17, gekennzeichnet durch eine Einrichtung (46) zur Begrenzung der Bandbreite des zweiten Steuersignals und dadurch, daß das digitale Signal mit einer Verzögerung relativ zu der Informationsbitfolge übertragen wird, damit die langsame Antwort des zweiten Steuersignals, die von dessen begrenzter Bandbreite herrührt, kompensiert wird.
- 45 19. Digital-Analog-Decodierer zur Verwendung in Verbindung mit einem Codierer nach Anspruch 1, umfassend einen Umsetzer (42), der auf das empfangene digitale Signal und die Schrittgrößensteuerinformation, die zusammen mit dem empfangenen Digitalsignal übertragen wird, anspricht, um ein analoges Ausgangssignal zu erzeugen, dadurch gekennzeichnet, daß der Decodierer eine Ableitungsschaltung (44, 46) zur Ableitung des Schrittgrößensteuersignals aus der Schrittgrößensteuerinformation zur Steuerung der Umsetzung in dem Umsetzer (42) enthält, und daß die Schaltung eine Einrichtung (46) enthält, die eine Bandbreitenbegrenzung und damit eine langsame Anstiegszeit des Steuersignals bewirkt.
- 50 20. Decodierer nach Anspruch 19, dadurch gekennzeichnet, daß die Bandbreitenbegrenzungseinrichtung
- 55



(46) das Schrittgrößensteuersignal auf eine solche Bandbreite begrenzt, daß der Umsetzer (42) im wesentlichen lineare Charakteristiken aufweist.

21. Decodierer nach Anspruch 19 oder 20, dadurch gekennzeichnet, daß die Ableitungsschaltung einen zweiten Umsetzer (44) zur Umsetzung der Information in digitaler Form in ein analoges Steuersignal enthält, das der Bandbreitenbegrenzung unterworfen wird.
22. Decodierer nach einem der Ansprüche 19 bis 21, dadurch gekennzeichnet, daß die begrenzte Bandbreite etwa 50 Hz beträgt.
23. Decodierer nach einem der Ansprüche 19 bis 21, dadurch gekennzeichnet, daß die Bandbreitenbegrenzungseinrichtung (46) eine Anstiegszeit aufweist, die im wesentlichen im Bereich von 5 bis 20 ms liegt.
24. Decodierer nach Anspruch 21, dadurch gekennzeichnet, daß der zweite Umsetzer (44) ein Tiefpaßfilter (206) zur Begrenzung der Bandbreite des Schrittgrößensteuersignals enthält.
25. Decodierer nach Anspruch 24, dadurch gekennzeichnet, daß der Tiefpaßfilter (206) drei Einpol-Filter umfaßt, von jedes eine Zeitkonstante von 2 ms aufweist.
26. Decodierer nach Anspruch 24, bei dem die Schrittgrößeninformation in der Form des Logarithmus der Neigung des analogen Eingangssignal ist, ferner gekennzeichnet durch einen Exponentiator (208) zur Potenzierung des in logarithmischer Form übertragenen bandbreitenbegrenzten Schrittgrößensteuersignals.
27. Decodierer nach Anspruch 25 und Anspruch 26, dadurch gekennzeichnet, daß das Tiefpaßfilter (206) so angeordnet ist, daß ein Zweipolfilter dem Exponentiator (208) vorangeht und ein Einpolfilter folgt.
28. Decodierer nach Anspruch 26, dadurch gekennzeichnet, daß die Welligkeit am Eingang des Exponentiators (208) auf einige wenige Prozent seines mittleren Pegels beschränkt ist.
29. Decodierer nach einem der Ansprüche 24 bis 28, dadurch gekennzeichnet, daß das Tiefpaßfilter (206) zugleich als ein Deltasignademodulator zur Demodulation des empfangenen Steuersignals dient.
30. Decodierer nach Anspruch 19, 20 oder 21, dadurch gekennzeichnet, daß das von dem Decodierer empfangene digitale Signal eine Einzelbitfolge enthält, wobei das digitale Signal und die Schrittgrößeninformation in der Bitfolge in einer Weise übertragen werden, die ihre Unterscheidung voneinander erlaubt.
31. Decodierer nach Anspruch 19, 20 oder 21, dadurch gekennzeichnet, daß das digitale Signal und die Schrittgrößeninformation in gesonderten Bitfolgen übertragen werden.
32. Decodierer nach einem der Ansprüche 19 bis 21, dadurch gekennzeichnet, daß der Umsetzer (42) einen adaptiven Deltademodulator umfaßt.
33. Decodierer nach einem der Ansprüche 19 bis 21, dadurch gekennzeichnet, daß der Umsetzer (42) einen Deltademodulator und eine Einrichtung zur Änderung des Pegels des analogen Ausgangssignals als Funktion des Schrittgrößensteuersignals zur Erzeugung des analogen Ausgangssignals umfaßt.
34. Decodierer nach Anspruch 33, dadurch gekennzeichnet, daß die Pegeländerungseinrichtung die Schrittgröße des Deltademodulators (42) als Funktion des Steuersignals einstellt.
35. Decodierer nach Anspruch 33, dadurch gekennzeichnet, daß die vom dem Deltademodulator (42) angewendete Schrittgröße im wesentlichen fest ist, wobei die Pegeländerungseinrichtung das Ausgangssignal des Deltademodulators einer variablen Verstärkung unterzieht, um den Pegel des analogen Ausgangssignals zu modulieren.
36. Decodierer nach einem der Ansprüche 19 bis 21, dadurch gekennzeichnet, daß der Umsetzer (42) einen Leckintegrator (204) und einen Pulshöhenmodulator (202) enthält, die auf die Schrittgrößeninfor-



mation ansprechen, um den Pegel des analogen Ausgangssignals zu modulieren, damit das analoge Ausgangssignal aus der digitalen Repräsentation des analogen Eingangssignals erzeugt wird.

37. Decodierer nach Anspruch 36, dadurch gekennzeichnet, daß der Leckintegrator (204) eine Zeitkonstante von etwa 0,5 ms aufweist.

38. Codierer nach Anspruch 1, dadurch gekennzeichnet, daß die Schrittgrößenschaltung (18) so ausgebildet ist, daß das erste Steuersignal eine Anstiegszeit von wenigstens etwa 1 ms aufweist.

