What is claimed is:

1. A semiconductor memory device comprising:

a memory cell array including a plurality of dynamic memory cells;

an error correction code engine (an ECC engine);

an input/output gating circuit (an I/O gating circuit) connected between the ECC engine and the memory cell array;

an error information register configured to store an error address and a first syndrome, the error address and the first syndrome being associated with a first error bit in a first codeword stored in a first page of the memory cell array; and

a control logic circuit configured to control the ECC engine, the I/O gating circuit and the error information register based on an address and a command from an external memory controller,

wherein the control logic circuit is further configured to, based on the first codeword being read again and including a second error bit which is different from the first error bit, recover a second syndrome associated with the second error bit by using the first syndrome stored in the error information register and sequentially correct the first error bit and the second error bit.

2. The semiconductor memory device of claim 1, wherein the ECC engine is further configured to sequentially correct the first error bit and the second error bit based on the first syndrome and the second syndrome.

3. The semiconductor memory device of claim 2, wherein the control logic circuit is further configured to control the ECC engine to recover the second syndrome by performing

an XOR operation based on the first syndrome and a third syndrome, and

wherein the third syndrome is associated with a third error bit which is mis-corrected due to the first error bit and the second error bit.

4. The semiconductor memory device of any one of claims 1 to 3, wherein the ECC engine is further configured to correct a single error bit.

5. The semiconductor memory device of any one of claims 1 to 4, wherein the error information register is further configured to store a row address and a column address associated with the first codeword.

6. The semiconductor memory device of claim 5, wherein the control logic circuit is further configured to reset a row of the error information register in which the error address and the first syndrome associated with the first error bit are stored based on a new write data being stored in the first page.

7. The semiconductor memory device of any one of claims 1 to 6, wherein the error information register comprises:

an error information table configured to store a row address, a column address and the first syndrome, in association with the first codeword;

a table pointer configured to provide a table pointing signal corresponding to the error information table based on the address; and

a resetter configured to reset contents stored in the error information table based on a control signal being received from the control logic circuit.

8. The semiconductor memory device of any one of claims 1 to 7, wherein the ECC engine includes:

an ECC encoder configured to perform ECC encoding on a main data from the external memory controller to generate parity bits to be stored in the first page; and

an ECC decoder configured to perform ECC decoding on the main data in the first codeword as read from the first page by using the parity bits to generate the first syndrome, and recover the second syndrome by using the first syndrome.

9. The semiconductor memory device of claim 8, wherein the ECC decoder includes:

a syndrome generation circuit configured to generate a syndrome by using the first codeword as read from the first page;

an error locator configured to generate an error position signal indicating a position of the first error bit or the second error bit based on the syndrome or a recovered syndrome;

a data corrector configured to correct the first error bit or the second error bit based on the error position signal to output a corrected main data;

a selection circuit configured to select one from among the first syndrome and a ground voltage as a selected output based on a selection signal; and

an XOR gate to perform an XOR operation on the syndrome and the selected output to provide the error locator with the syndrome or the recovered syndrome.

10. The semiconductor memory device of claim 9, wherein the error locator is further configured to provide an error generation signal to the control logic circuit based on the syndrome including the first error bit, and

wherein the control logic circuit is further configured to store a row address and a column address of the first codeword associated with the first error bit in the error information register as the error address.

11. The semiconductor memory device of claim 9 or claim 10, wherein the data corrector is further configured to store the syndrome in the error information register as the first syndrome when the syndrome includes the first error bit.

12. The semiconductor memory device of any one of claims 9 to 11, wherein the syndrome generation circuit comprises:

a check bit generator configured to generate check bits based on the main data in the first codeword as read from the first page; and

a syndrome generator configured to generate the syndrome by comparing corresponding bits of the parity bits in the first codeword and the check bits.

13. The semiconductor memory device of any one of claims 1 to 12, wherein the control logic circuit is further configured to store the error address and the first syndrome in a portion of the memory cell array.

14. The semiconductor memory device of any one of claims 1 to 13, comprising:

first group dies including at least one buffer die; and

second group dies including a plurality of memory dies, the plurality of memory dies stacked on the first group dies and conveying data through a plurality of through silicon via lines (a plurality of TSV lines),

wherein at least one of the plurality of memory dies includes the memory cell array

and the ECC engine, and the ECC engine is further configured to generate transmission parity bits using a transmission data to be sent to the first group dies, and

wherein the at least one buffer die includes a via-ECC engine configured to correct a transmission error using the transmission parity bits when the transmission error is detected from the transmission data received through the plurality of TSV lines.

15. The semiconductor memory device of claim 14, wherein the semiconductor memory device is a high-bandwidth memory (HBM).

16. The semiconductor memory device of claim 14 or claim 15, wherein the ECC engine is further configured to correct error output from the plurality of memory dies before the transmission data is sent to the at least one buffer die.

17. A memory system comprising:

at least one semiconductor memory device; and

a memory controller configured to control the at least one semiconductor memory device, wherein the at least one semiconductor memory device includes:

a memory cell array including a plurality of dynamic memory cells;

an error correction code engine (an ECC engine);

an input/output gating circuit (an I/O gating circuit) connected between the ECC engine and the memory cell array;

an error information register configured to store an error address and a first syndrome, the error address and the first syndrome being associated with a first error bit in a first codeword stored in a first page of the memory cell array; and

a control logic circuit configured to control the ECC engine, the I/O gating circuit

and the error information register based on an address and a command from the memory controller,

wherein the control logic circuit is further configured to control, when the first codeword is read again from the first page and includes a second error bit different from the first error bit, the ECC engine to recover a second syndrome associated with the second error bit by using the first syndrome stored in the error information register and sequentially correct the first error bit and the second error bit.

18. The memory system of claim 17, wherein the ECC engine is further configured to sequentially correct the first error bit and the second error bit based on the first syndrome and the second syndrome as recovered.

19. A method of operating a semiconductor memory device including a memory cell array, the method of operating the semiconductor memory device comprising:

performing, in an error correction code engine (an ECC engine), ECC decoding on a first codeword as read from a memory location of the memory cell array, the first codeword corresponding to an access address;

storing an error address and a first syndrome in an error information register based on a first error bit being detected in the first codeword, the error address and the first syndrome being associated with the first error bit;

recovering, in the ECC engine, a second syndrome associated with a second error bit by using the first syndrome stored in the error information register based on the first codeword being read again from the memory location and including the second error bit which is different from the first error bit; and

correcting, in the ECC engine, the first error bit and the second error bit by using the

first syndrome and the second syndrome.

20. The method of operating the semiconductor memory device of claim 19, wherein the memory cell array includes a plurality of dynamic memory cells, and

wherein the ECC engine is further configured to separate the first error bit and the second error bit generated in the first codeword by lapse to time and configured to sequentially correct the first error bit and the second error bit.