

CLAIMS

1. A method of forming a semiconductor packaging structure, the method comprising:
 - forming a plurality of semiconductor packages, each semiconductor package comprising a semiconductor die and a mold encapsulation structure covering at least a portion of the semiconductor die;
 - arranging the plurality of semiconductor packages to form a vertical stacked arrangement with a mold portion comprising a plurality of mold encapsulation structures, the mold portion extending from a first side of the vertical stacked arrangement to a second side of the vertical stacked arrangement opposite the first side;
 - forming a first via on the mold portion at the first side of the vertical stacked arrangement after the vertical stacked arrangement is formed;
 - forming a second via on the mold portion at the second side of the vertical stacked arrangement after forming the first via; and
 - forming an electrically conductive filled via extending through the mold portion from the first side of the vertical stacked arrangement to the second side of the vertical stacked arrangement by depositing a suitable electrically conductive material in the first via and in the second via;
 - wherein a diameter of the electrically conductive filled via at the first side of the vertical stacked arrangement is greater than a diameter of the electrically conductive filled via along an intervening plane of the vertical stacked arrangement, the intervening plane between the first side of the vertical stacked arrangement and the second side of the vertical stacked arrangement;
 - and
 - wherein a diameter of the electrically conductive filled via at the second side of the vertical stacked arrangement is greater than the diameter of the electrically conductive filled via along the intervening plane of the vertical stacked arrangement.

2. The method according to claim 1,
wherein each semiconductor package further comprises a redistribution layer over the semiconductor die.
3. The method according to claim 2,
wherein the redistribution layer extends from over the semiconductor die to over the mold encapsulation structure.
4. The method according to claim 2,
wherein the redistribution layer comprises one or more electrically conductive lines.
5. The method according to claim 4,
wherein the one or more electrically conductive lines are in electrical connection with the electrically conductive filled via.
6. The method according to claim 1,
wherein forming the vertical stacked arrangement comprises applying adhesive to adhere neighbouring semiconductor packages of the vertical stacked arrangement.
7. The method according to claim 1,
wherein forming the first via comprises laser drilling the mold portion at the first side of the vertical stacked arrangement.
8. The method according to claim 1,
wherein forming the second via comprises laser drilling the mold portion at the second side of the vertical stacked arrangement.
9. The method according to claim 1,

wherein the electrically conductive filled via comprises a first tapered portion extending from the first side of the vertical stacked arrangement to the intervening plane of the vertical stacked arrangement; and

wherein the electrically conductive filled via comprises a second tapered portion extending from the second side of the vertical stacked arrangement to the intervening plane of the vertical stacked arrangement.

10. The method according to claim 1,
wherein the suitable electrically conductive material is deposited in the first via and the second via by electroplating.
11. A semiconductor packaging structure comprising:
a vertical stacked arrangement comprising a plurality of semiconductor packages, each semiconductor package comprising a semiconductor die and a mold encapsulation structure covering at least a portion of the semiconductor die;
wherein the vertical stacked arrangement comprises a mold portion comprising a plurality of mold encapsulation structures, the mold portion extending from a first side of the vertical stacked arrangement to a second side of the vertical stacked arrangement opposite the first side;
wherein the mold portion comprises an electrically conductive filled via extending through the mold portion from the first side of the vertical stacked arrangement to the second side of the vertical stacked arrangement, the electrically conductive filled via comprising a suitable electrically conductive material;
wherein a diameter of the electrically conductive filled via at the first side of the vertical stacked arrangement is greater than a diameter of the electrically conductive filled via along an intervening plane of the vertical stacked arrangement, the intervening plane between the first side of the vertical stacked arrangement and the second side of the vertical stacked arrangement;
and

wherein a diameter of the electrically conductive filled via at the second side of the vertical stacked arrangement is greater than the diameter of the electrically conductive filled via along the intervening plane of the vertical stacked arrangement.

12. The semiconductor packaging structure according to claim 11,
wherein the vertical stacked arrangement further comprises a redistribution layer between the semiconductor dies of neighbouring semiconductor packages of the vertical stacked arrangement.
13. The semiconductor packaging structure according to claim 12,
wherein the redistribution layer extends from between the semiconductor dies to between the mold encapsulation structures of neighbouring semiconductor packages of the vertical stacked arrangement.
14. The semiconductor packaging structure according to claim 12,
wherein the redistribution layer comprises one or more electrically conductive lines.
15. The semiconductor packaging structure according to statement 14,
wherein the one or more electrically conductive lines are in electrical connection with the electrically conductive filled via.
16. The semiconductor packaging structure according to claim 11,
wherein the vertical stacked arrangement further comprises an adhesive layer between neighbouring semiconductor packages of the vertical stacked arrangement.
17. The semiconductor packaging structure according to claim 16,

wherein the adhesive layer between neighbouring semiconductor packages of the vertical stacked arrangement is configured to adhere the neighbouring semiconductor packages.

18. The semiconductor packaging structure according to claim 11,
wherein the intervening plane of the vertical stacked arrangement, the first side of the vertical stacked arrangement, and the second side of the vertical stacked arrangement are substantially parallel to one another.
19. The semiconductor packaging structure according to claim 11,
wherein the electrically conductive filled via comprises a first tapered portion extending from the first side of the vertical stacked arrangement to the intervening plane of the vertical stacked arrangement; and
wherein the electrically conductive filled via comprises a second tapered portion extending from the second side of the vertical stacked arrangement to the intervening plane of the vertical stacked arrangement.
20. The semiconductor packaging structure according to claim 11,
wherein the suitable electrically conductive material is copper.