WHAT IS CLAIMED IS:

1. A Fin field-effect transistor (FinFET) device comprising:

a substrate;

first and second source/drain (S/D) regions of a first conductivity type disposed on the substrate;

a fin channel structure of semiconductor material disposed on the substrate and extending between the first and second S/D regions, the fin channel structure including a first fin portion, a second fin portion, and a channel portion, the channel portion of a second conductivity type;

a gate structure disposed over the channel portion, the gate structure including a gate dielectric and a gate electrode; and

wherein the fin channel structure comprises first and second angled sidewalls.

2. The FinFET device in accordance with Claim 1 wherein the fin channel structure has a trapezoidal cross-section shape.

3. The FinFET device in accordance with Claim 1 wherein

surfaces of the first and second angled sidewalls have (111) surface orientation.

4. The FinFET device in accordance with Claim 3 wherein a top surface of the fin channel structure has a (100) surface orientation.

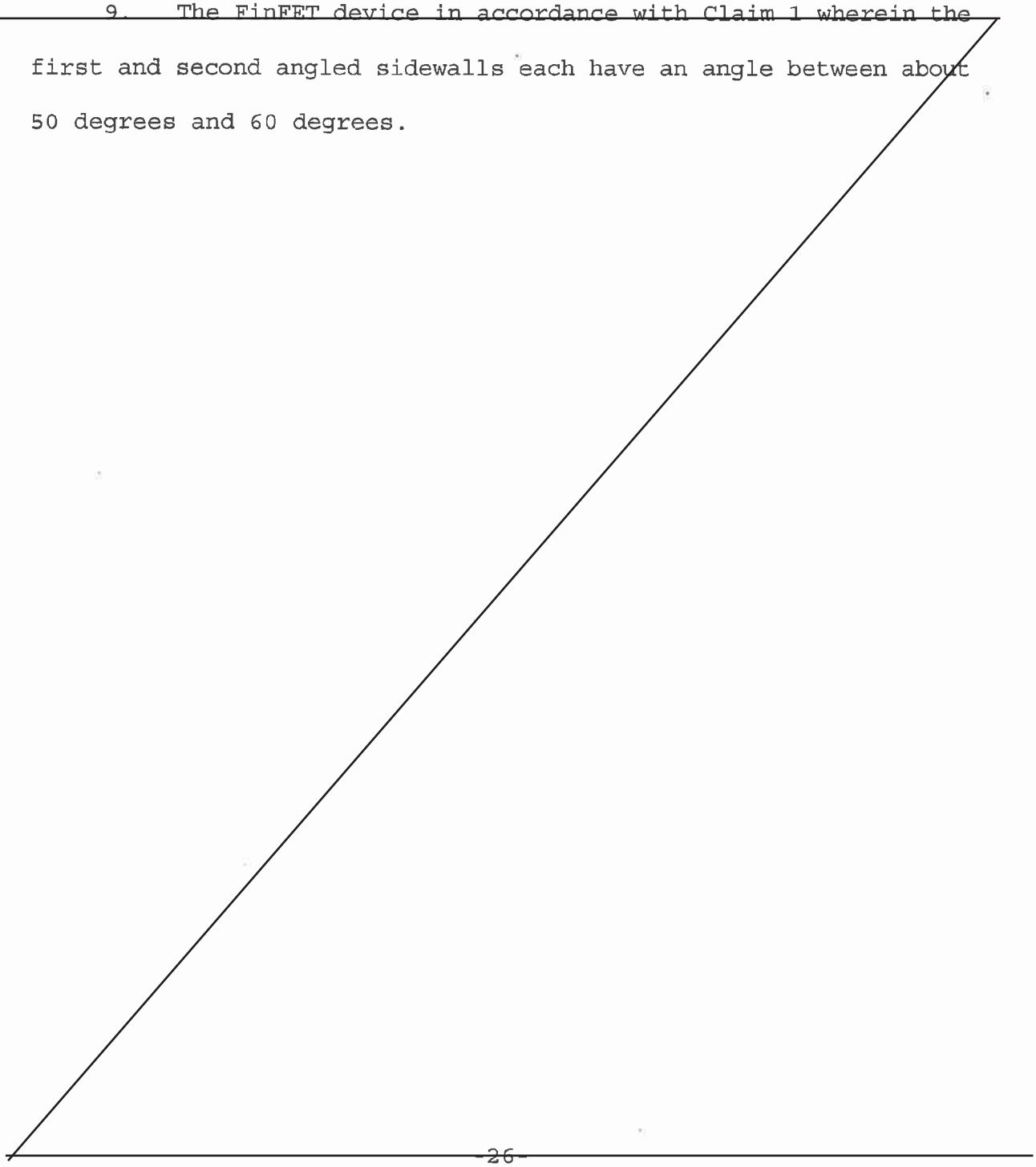
5. The FinFET device in accordance with Claim 3 wherein the channel portion has a (100) channel orientation.

6. The FinFET device in accordance with Claim 3 wherein the first and second angled sidewalls each have an angle between about 50 degrees and 60 degrees.

7. The FinFET device in accordance with Claim 3 wherein the gate dielectric comprises high-K dielectric material.

8. The FinFET device in accordance with Claim 1 wherein the first and second angled sidewalls each have an angle between about 40 degrees and 65 degrees.

9. The FinFET device in accordance with Claim 1 wherein the first and second angled sidewalls each have an angle between about 50 degrees and 60 degrees.



10. A p-channel Fin field-effect transistor (FinFET) device comprising:

a substrate;

first and second source/drain (S/D) regions of p-type conductivity disposed on the substrate;

a fin channel structure of semiconductor material disposed on the substrate and extending between the first and second S/D regions, the fin channel structure including a first fin portion, a second fin portion, and a channel portion of n-type conductivity, and having a top surface and two sidewalls each having a sidewall surface;

a gate structure disposed over the top surface of the channel portion, the gate structure including a gate dielectric and a gate electrode; and

wherein the two sidewall surfaces of the channel portion have a (111) surface orientation and the top surface of the channel portion has a different surface orientation.

11. The FinFET device in accordance with Claim 10 wherein the fin channel structure has a trapezoidal cross-section shape.

12. The FinFET device in accordance with Claim 12 wherein each of the two sidewall surfaces have an angle of between about 40 degrees and 65 degrees.

13. The FinFET device in accordance with Claim 12 wherein each of the two sidewall surfaces have an angle between about 50 degrees and 60 degrees.

14. The FinFET device in accordance with Claim 13 wherein the gate dielectric comprises hafnium oxide.

15. The FinFET device in accordance with Claim 12 wherein the top surface of the fin channel structure has a (100) surface orientation.

16. A method of fabricating a p-channel Fin field-effect transistor (Fin FET), the method comprising:

providing a substrate of semiconductor material having a (100) surface orientation;

forming a mask layer on the substrate and exposing portions of the substrate;

selectively removing exposed portions of the substrate to form a fin channel structure having sloped sidewalls, the sloped sidewalls having a (111) surface orientation;

forming a gate dielectric layer over at least a portion of the fin channel structure; and

forming a gate electrode layer over the gate dielectric layer.

17. The method in accordance with Claim 16 wherein selectively removing further comprises etching using at least one of a TMAH solution or ammonium hydroxide.

18. The method in accordance with Claim 17 wherein selectively removing further comprises forming each of the sloped sidewalls having an angle between about 40 and 65 degrees.

19. The method in accordance with Claim 16 wherein the fin channel structure has a trapezoidal cross-section shape with a top surface having a (100) surface orientation.

20. The method in accordance with Claim 19 wherein selectively removing further comprises forming each of the sloped sidewalls having an angle between about 50 and 60 degrees.

What is claimed is:

1. A method of fabricating a p-channel Fin field-effect transistor (Fin FET), the method comprising:

providing a substrate of semiconductor material having a (100) surface orientation disposed on an insulator;

forming a mask layer on the substrate and exposing portions of the substrate;

selectively removing exposed portions of the substrate to form a fin channel structure having sloped sidewalls, the sloped sidewalls having a (111) surface orientation, the formed fin channel structure having a top surface adjacent the mask layer and a bottom surface adjacent the insulator, and wherein the bottom surface has a width greater than a width of the top surface;

forming a gate dielectric layer over at least a portion of the fin channel structure; and

forming a gate electrode layer over the gate dielectric layer.

2. The method in accordance with claim 1 wherein selectively removing further comprises etching using at least one of a TMAH solution or ammonium hydroxide.

3. The method in accordance with claim 2 wherein selectively removing further comprises forming each of the sloped sidewalls having an angle between about 40 and 65 degrees.

4. The method in accordance with claim 1 wherein the fin channel structure has a trapezoidal cross-section shape with a top surface having a (100) surface orientation.

5. The method in accordance with claim 4 wherein selectively removing further comprises forming each of the sloped sidewalls having an angle between about 50 and 60 degrees.

6. A method of fabricating a p-channel Fin field-effect transistor (FinFET), the method comprising:

providing a substrate having a semiconductor material disposed on an insulating layer, the semiconductor material having a (100) surface orientation;

forming a mask layer on the semiconductor material and exposing portions of the semiconductor material;

selectively removing exposed portions of the semiconductor material having exposed surfaces of (100) surface orientation using a wet etch process to form a fin channel structure, the formed fin channel structure having sloped sidewalls, the sloped sidewalls having a (111) surface orientation;

forming a gate dielectric layer over at least a portion of the fin channel structure; and

forming a gate electrode layer over the gate dielectric layer.

7. The method in accordance with claim 6 wherein selectively removing further comprises etching using at least one of a TMAH solution or ammonium

hydroxide.

8. The method in accordance with claim 7 wherein selectively removing further comprises forming each of the sloped sidewalls having an angle between about 40 and 65 degrees.

9. The method in accordance with claim 8 wherein the formed fin channel structure has a bottom surface adjacent the insulator, and wherein the bottom surface has a width greater than a width of a top surface of the formed fin channel structure.

10. The method in accordance with claim 6 wherein the fin channel structure has a trapezoidal cross-section shape with a top surface having a (100) surface orientation.

11. The method in accordance with claim 6 wherein selectively removing further comprises forming each of the sloped sidewalls having an angle between about 50 and 60 degrees.

12. A method of fabricating a Fin field-effect transistor (FinFET), the method comprising:

providing a substrate of semiconductor material having a (100) surface orientation;

forming a mask layer on the substrate to expose portions of the substrate, the exposed portions having exposed surfaces with the (100) surface orientation;

selectively removing, using a wet etch process, the exposed portions of the substrate to form a fin channel structure, the formed fin channel structure having sloped sidewalls, the sloped sidewalls having a (111) surface orientation;

forming a gate dielectric layer over at least a portion of the fin channel structure; and

forming a gate electrode layer over the gate dielectric layer.

13. The method in accordance with claim 12 wherein selectively removing further comprises wet etching using at least one of a TMAH solution or ammonium hydroxide.

14. The method in accordance with claim 13 wherein selectively removing further comprises forming each of the sloped sidewalls having an angle between about 40 and 65 degrees.

15. The method in accordance with claim 14 wherein the formed fin channel structure has a bottom portion and a top portion, and the bottom portion has a width greater than the top portion.

16. The method in accordance with claim 12 wherein the fin channel structure has a trapezoidal cross-section shape with a top surface having a (100) surface orientation.

17. The method in accordance with claim 16 wherein selectively removing

further comprises forming each of the sloped sidewalls having an angle between about 40 and 65 degrees.

18. The method in accordance with claim 12 wherein the formed fin structure has a top surface with a first width between the sloped sidewalls and a bottom surface having a second width between the sloped sidewalls, and wherein the first width is less than the second width.