A METHOD TO FABRICATE DUAL-METAL CMOS TRANSISTORS FOR SUB-0.1 μm ULSI INTEGRATION

ABSTRACT

A new method for forming a dual-metal gate CMOS transistors is described. An NMOS and a PMOS active area of a semiconductor substrate are separated by isolation regions. A nitride layer is deposited overlying a gate dielectric layer and patterned to form a first dummy gate in each of the active areas. First ions are implanted to form source/drain regions in each of the active areas not covered by the first dummy gates. The first dummy gates are isotropically etched to form second dummy gates thinner than the first dummy gates. Second ions are implanted to form lightly doped source/drain regions in each of the active areas not covered by the second dummy gates. Dielectric spacers are formed on sidewalls of the second dummy gates and the source/drain regions are silicided. A dielectric layer is deposited and planarized to the second dummy gates. Thereafter, the second dummy gates are removed, leaving gate openings in the dielectric layer. A mask is formed over the PMOS active area. A first metal layer is deposited in the gate opening in the NMOS active area and planarized to the mask. The mask is removed. A second metal layer is deposited in the gate opening in the PMOS active area. The first and second metal layers are polished away to the dielectric layer thereby completing formation of dual-metal gate CMOS transistors in the fabrication of an integrated circuit.

Fig. 21