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(54) SEMICONDUCTOR DEVICE MANUFACTURE

(71) We, PHILIPS ELECTRONIC AND ASSOCIATED INDUSTRIES LIMITED, of Abacus House, 33 Gutter Lane, London, E.C.2, a British Company, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to semiconductor devices and methods of manufacturing a semiconductor device.

A known semiconductor device comprises a semiconductor body having at least one circuit element with at least three regions of which first and second regions have a first conductivity type and are separated by a third region which has a second conductivity type opposite to the first type. A pattern of insulating material is inset at least over a part of its thickness in the semiconductor body from a major surface of said body. The whole periphery of a portion of said body is bounded by part of the inset pattern. This bounded portion of the body adjoins said major surface and has located therein the whole of said first and third regions and at least a part of said second region. The inset pattern is adjoined by said third region along at least a part of its periphery and by said part of said second region along the whole of its periphery in said bounded portion of the body. The said third region which is of the second conductivity type is separated from the major surface at least partly by said first region.

Such a semiconductor device in which the circuit element is a transistor is described in our British Patent No. 1,208,574, and has important advantages. For example, the *p-n* junction between the region of the second conductivity type serving as a base and the second region of the first conductivity type serving as a collector is substantially flat and is laterally bounded by the pattern while avoiding strong curvature of the junction near its edge. This has a favourable influence on the electric properties of the transistor.

In manufacturing such a semiconductor device in an integrated circuit, the starting material is often a high-ohmic semiconductor substrate of *p*-type conductivity on which a semiconductor layer of *n*-type conductivity is deposited epitaxially. If so desired, *n*-type doping material may be provided on the substrate before the epitaxial deposition in order to form the semiconductor body a so-called buried collector layer.

By local oxidation of the epitaxial layer, the inset pattern of insulating material is then formed and regions of the *p*- and of the *n*-conductivity type, namely the base and the emitter of the transistor, are then successively formed by diffusion in the semiconductor portion bounded laterally by the pattern.

It has been found experimentally that during the formation of the inset pattern by oxidation of the epitaxial layer, the doping material characteristic of the *n*-type conductivity in the epitaxial layer is often only slightly absorbed into the formed oxide and is even forced into the substrate as a result of which this can be locally overdoped and channelling can occur between circuit elements in adjacent bounded portions separated by the inset pattern.

Furthermore, a concentration of the doping material from the epitaxial layer at the boundary with the inset layer can adversely affect a diffused base region formed to adjoin the pattern along its whole periphery, since an edge region of the resulting base is less strongly of the *p*-type conductivity than is a central part of the base.

In addition, doping materials which cause the *p*-type conductivity in the semiconductor material are often absorbed to a considerable extent by the inset pattern, as a result of which the base becomes thinner at least at its boundary with the inset pattern.

If subsequently an emitter of the *n*-type is diffused in the bounded portion to adjoin the inset pattern, the edge region of the base

[Price 33p]

Price 75p

is often overdoped as a result of which shortcircuit occurs between the emitter and the collector. Such a shortcircuit easily occurs in certain processes to obtain the inset pattern as will be described in detail below.

The described problems of channelling and shortcircuit may also occur, for example, when the starting material is a *p*-type epitaxial layer on a *p*-type substrate. Channelling and shortcircuit may occur in this case in that *n*-type channels can be induced in *p*-type regions adjoining the oxide by positive charges in the oxide or at the semiconductor-oxide interface. Such channelling is promoted in that instead of forcing the doping material into the epitaxial layer, the *p*-type doping material is absorbed to a considerable extent from the epitaxial layer by the oxide as it grows.

According to a first aspect of the present invention there is provided a semiconductor device comprising a semiconductor body having at least one circuit element with at least three regions of which first and second regions have a first conductivity type and are separated by a third region which has a second conductivity type opposite to the first type, and a pattern of insulating material inset at least over a part of its thickness in the semiconductor body from a major surface of said body, the whole periphery of a portion of said body being bounded by part of the inset pattern, which bounded portion of the body adjoins said major surface and has located therein the whole of said first and third regions and at least a part of said second region, the inset pattern being adjoined by said third region along at least a part of its periphery and by said part of said second region along the whole of its periphery in said bounded portion of the body, said third region being separated from the major surface at least partly by said first region, and the inset pattern, at least at the area where it adjoins the bounded portion in the semiconductor body, being entirely embedded in an adjoining zone having a concentration of doping material characteristic of the second conductivity type, said concentration being smaller than the maximum concentration of the doping material determining the first conductivity type in said second region of the first conductivity type, said concentration being sufficiently large to prevent, in regions of the second conductivity type at the area of the zone, electrical connection between regions of the first conductivity type.

Doping material is to be understood herein to also include a mixture of doping materials which cause the same conductivity type. With such an adjoining zone, overdoping of a semiconductor substrate during the oxidation of, for example, an epitaxial layer and channelling between bounded portions separated by the pattern can be prevented and a so-called channel stopper be formed.

Therefore, the semiconductor device according to the invention preferably is an integrated circuit, in which the semiconductor body comprises a substrate and an epitaxial layer, said second region of the first conductivity type comprises a buried layer, and the concentration of the doping material in said adjoining zone is smaller than the concentration of the doping material determining the first conductivity type in the buried layer.

It will be obvious that in the semiconductor device according to the invention the zone adjoining the pattern and the said regions partly coincide.

In one important form the concentration of the doping material characteristic of the second conductivity type in the adjoining zone is smaller than the maximum concentration of the doping material determining the first conductivity type in said first region of the first conductivity type, and the said first region at least over a part of its periphery adjoins the inset pattern. Due to the adjoining zone, shortcircuit between the two regions of the first conductivity type can be prevented. The manufacture of this form of the device is comparatively simple, since no accurate alignment step relative to the region of the second conductivity type is necessary for providing said first region, and the mask opening for diffusion of said first region can even be partly laid over the pattern. Thus, no space need be reserved on the major surface for inaccuracies in the alignment step for providing said first region, as a result of which space is saved and the semiconductor device can be made smaller. A further advantage is that the two *p-n* junctions between the regions of the circuit element can be of approximately the same dimensions. This permits more freedom in the choice as to which of the two regions of the first conductivity type may serve as the emitter and which as the collector of a transistor. Said third region of the second conductivity type may serve as the base.

Said first region may adjoin the inset pattern over part of its periphery and said third region which is of the second conductivity type may adjoin the major surface in two places separated from each other by the said first region. As a result of this, for example, a bipolar transistor having two base contacts or a so-called junction field-effect transistor can be obtained.

In another form, the semiconductor device may be constructed so that multi-emitter or multi-collector systems are obtained.

In another form, adjacent portions bounded by the insert pattern have a common region with a high concentration of a doping material, *via* which circuit elements in these

adjacent bounded portions can be conductively connected. In order to obtain certain circuits, the common region in one bounded portion may serve as the emitter and in the adjacent bounded portion as the collector.

If said first region of the first conductivity type throughout its periphery extends adjacent the inset pattern, space will generally be reserved on the major surface for connection to the region of the second conductivity type. If the concentration of the doping material characteristic of the second conductivity type in the adjoining zone is larger than the maximum concentration of the doping material determining the first conductivity type in said first region of the first conductivity type, the zone adjoining the pattern may be provided at the major surface with a contact for the region of the second conductivity type.

A zone adjoining the pattern may be used for contacting a semiconductor body of the second conductivity type, for example of a substrate on which an epitaxial layer is provided. For that purpose, the semiconductor body preferably has another bounded portion which adjoins the major surface and is founded at least along a part of its periphery and throughout its thickness by a part of the inset pattern in the semiconductor body, which inset pattern part is entirely embedded in an adjoining zone having a concentration of a doping material causing the second conductivity type at least in the part of the adjoining zone which is situated in this other bounded portion, and the substrate is contacted at the major surface *via* the part of the adjoining zone in this other bounded portion of the body.

According to a second aspect of the present invention there is provided a method of manufacturing a semiconductor device comprising a semiconductor body having at least one circuit element with at least three regions of which first and second regions have a first conductivity and are separated by a third region which has a second conductivity type opposite to the first type, and a pattern of insulating material inset at least over a part of its thickness in the semiconductor body from a major surface of said body, the whole periphery of a portion of said body being bounded by part of the inset pattern, which bounded portion of the body adjoins said major surface and has located therein the whole of said first and third regions and at least a part of said second region, the inset pattern being adjoined by said third region along at least a part of its periphery and by said part of said second region the whole of its periphery in so far as it is located in said bounded portion of the body, said third region being separated from the major surface at least partly by said first region, said inset pattern being formed by oxidation of the semiconductor at apertures in an oxidation resistant masking layer provided on the major surface of the body, in which method the semiconductor body is subjected to a treatment in which doping material characteristic of the second conductivity type in the semiconductor body is diffused to form a zone adjoining the pattern and having a concentration of said doping material which is smaller than the maximum concentration of the doping material determining the first conductivity type in the said second region of the first conductivity type and which is sufficiently large to prevent in regions of the second conductivity type at the area of the zone electrical connection between regions of the first conductivity type.

The masking layer may first be used for obtaining a doping pattern characteristic of the second conductivity in the semiconductor body, after which the masking layer is used for masking during oxidation of the doping pattern to obtain the inset pattern embedded in the adjoining zone having said doping material characteristic of the second conductivity type.

In this method the inset pattern consists of oxide of the semiconductor material, for example silicon oxide. The oxidation-resistant masking layer consists, for example, of silicon nitride or of a double layer of silicon oxide and silicon nitride which, besides against oxidation, also masks against diffusioin. In the choice of the concentration of the doping material in the doping pattern, the distribution of said doping material between the oxide pattern to be formed and the semiconductor material and the desirable concentration of the doping material in the various embodiments of the semiconductor device to be manufactured should of course be taken into account.

One is not restricted to the diffusion of the doping to obtain the adjoining zone preceding the oxidation.

Thus, the inset may first be formed by oxidation after which the zone of the second conductivity type adjoining the pattern is obtained by diffusion of aluminium or gallium as said doping material characteristic of the second conductivity type. In this variation the fact is used that aluminium and gallium can diffuse comparatively rapidly through silicon oxide.

When gallium or aluminium is used as a doping material which can cause the second conductivity type, the oxidation-resistant masking layer may be used as a diffusion-mask. However, these doping materials are preferably diffused after removing the masking layer. It will be obvious that in this case the concentration of the gallium and/or the aluminium in the adjacent zone is smaller than the maximum concentration of the doping material determining the first conductivity

type in said first region of the first conductivity type. Aluminium or gallium is preferably diffused after saaid first region of the first conductivity type has been formed in the semiconductor body.

The diffusion of the adjacent zone may be carried out simultaneously and with the same doping materials as a diffusion to obtain a region of the second conductivity type, for example, a base region or a contact region of, for example, a semiconductor body.

Embodiments of the first and second aspects of the invention will now be described by way of example, with reference to the accompanying drawings, in which:—

Figure 1 is a diagrammatic partial cross-sectional view and a partial perspective view of a part of a first semiconductor device in accordance with the invention;

Figure 2 is a diagrammatic partial cross-sectional view and partial perspective view of a part of another semiconductor device in accordance with the invention;

Figure 3 is a diagrammatic cross-sectional view of a part of a semiconductor device in an early stage of the manufacture;

Figure 4 is a diagrammatic cross-sectional view of a detail of the part shown in Figure 3 in a later stage of the manufacture using a method not in accordance with the present invention;

Figures 5 and 6 are diagrammatic cross-sectional views of the part shown in Figure 3 and a detail thereof, respectively, in later successive stages of manufacture by means of the method in accordance with the present invention, and

Figures 7 and 8 are diagrammatic cross-sectional views of the part shown in Figure 1 in successive stages of manufacture by means of a method in accordance with the present invention.

The first example of a semiconductor body to be described is an integrated circuit a part of which is shown in Figure 1. It comprises a semiconductor body 1 of *p*-conductivity type comprising as a circuit element a transistor having two regions 2 and (4, 5) of the *n*-conductivity type separated by a region 3 of the *p*-conductivity type.

An inset pattern (6, 7, 8) of insulating material is present in the semiconductor body 1 and extends from a major surface 9 of the semiconductor body 1 in said body. The semiconductor body has a portion 10 which adjoins the major surface 9 and is bounded along its whole periphery and throughout its whole thickness by the inset pattern 6, 7. In the bounded portion 10 region 2 of the *n*-conductivity type and the region 3 of the *p*-conductivity type are provided entirely and the other *n*-conductivity type region (4, 5) is provided partly. Both the region (4, 5) in so far as it is provided in the bounded portion 10 and the region 3 adjoin along the whole of their periphery the inset pattern 6, 7. The region 3 is separated partly from the major surface 9 by the region 2.

The inset pattern (6, 7, 8) in the semiconductor body is entirely embedded in an adjacent zone (11, 12, 13) having a concentration of a doping material characteristic of the *p*-conductivity type, which concentration is smaller than the maximum concentration of the doping material determined the *n*-conductivity type in region (4, 5). The concentration is also sufficiently large to prevent in *p*-type region 3 or *p*-type body 1 at the area of the zone (11, 12, 13) electrical connection between regions of the *n*-conductivity type, for example between the regions 2 and (4, 5).

In Figure 1 the boundary of the zone (11, 12, 13) in the semiconductor body is denoted partly in a solid and partly in a broken line. In the case of a broken line, the conductivity type of the regions is not varied by the presence of the zone, in the case of a solid line it is varied. So in this example the *p*-type region 3 is locally extended as it were by a *p*-type edge of the *n*-type part 4 of the *n*-type region 4, 5. The part 18 of the adjacent zone 11 serves as a so-called "channel stopper" with respect to a circuit element not shown in an adjacent bounded portion of the body. Such adjacent bounded portions can be isolated from each other by means of such channel stoppers.

In the embodiment shown in Figure 1, the concentration of the doping material characteristic of the *p*-conductivity type in the adjacent zone (11, 12, 13) is smaller than the maximum concentration of the doping material determining the *n*-conductivity type in region 2 of the *n*-conductivity type, and the region 2 adjoins over a part of its periphery the inset pattern (6, 7).

The regions 2 and 3 can be contacted via the major surface 9 at the bounded portion 10, while the region (4, 5) can be contacted via the same major surface at a second bounded portion 14.

The adjoining zone can be used for contacting a semiconductor substrate body of the *p*-conductivity type of the semiconductor device at the major surface. The semiconductor body has another bounded portion 15 which adjoins the major surface 9 and which is bounded at least along a part of its periphery and throughout its thickness by a part 8 of the inset pattern. The said part 8 is fully embedded in the semiconductor body in an adjacent zone 13. The zone 13 has a concentration of a doping material causing the *p*-conductivity type in the part 16 of the adjoining zone 13. *Via* the part 16 of the adjoining zone 13 in the other layer-shaped part 15, the semiconductor substrate body 1 is contacted at the major surface 9. Contacting is carried out, for example, on

a low-ohmic contact zone 17 of the *p*-conductivity type.

A second embodiment is shown in Figure 2. In this embodiment also the circuit element is a transistor. The semiconductor body 25 comprises an inset pattern 26, 27, a bounded portion 28 in which the regions 21 and (22, 23) of the *n*-type (the latter partly), and the region 24 of the *p*-type of the transistor are present.

The inset pattern 26, 27 is embedded in an adjacent zone (29, 30) in the same manner as described in the preceding embodiment. In this embodiment the region 24 of the *p*-type only over a part of its periphery adjoins the inset pattern 26, as a result of which the other *n*-type region (22, 23) in the bounded part 28 is contacted, if desired by means of a low-ohmic contact zone 31 of the *n*-type.

In a corresponding manner as in the preceding embodiment, the semiconductor substrate body 25 in this case also may be contacted at the major surface 32.

In manufacturing such semiconductor devices, an oxidation-resistant masking layer 37, 38 having apertures 39 at the area where the inset pattern is to be formed is provided on the major surface 35 (see Figure 3) of a semiconductor body of silicon.

It will now be described how in certain processes to obtain inset patterns not in accordance with the present invention short-circuit may occur between regions of the circuit element to be formed in the semiconductor body.

The masking layer 37, 38 often consists of a silicon oxide layer 38 and a silicon nitride layer 37. After providing the apertures 39 in the masking layer, recesses 40 are etched in the semiconductor body. During the oxidation of the silicon body 36 at the area of the recesses 40, oxidation occurs also at the edge of the apertures below the silicon oxide layer 38, as a result of which an inset oxide pattern is formed after the removal of the masking layer 37, 38, the shape of the edge 41 of which pattern is shown in Figure 4.

If in a usual manner a shallow region 43 of the *p*-type is diffused in the *n*-type layer-shaped part 44 *via* the major surface 35, an oxide layer 45 is also formed at the major surface 35. Upon removing the oxide layer 45, the part 42 shown in broken lines of the inset oxide pattern 41 may also be removed. It will be obvious from Figure 4 that the *p-n* junction 46 may be exposed so that in a subsequent diffusion of a doping material to obtain an *n*-type region short-circuit occurs between said region and the original layer-shaped part 44. In the method according to the present invention, the short-circuit described is prevented in that the semiconductor body 36 is subjected to a treatment in which a doping material characteristic of the second conductivity type in the semiconductor body 36 is diffused in a zone 61 adjoining the pattern 41.

In a variation of the method according to the invention, such a shortcircuit is preferably prevented in that the masking layer 37, 38 is used, prior to the oxidation, for masking during diffusion of the *p*-type doping material in the semiconductor body 36 to obtain a doping pattern 51, 52 (see Figure 5), after which the masking layer is used for masking during oxidation of the doping pattern 51, 52 to obtain the inset pattern 41 and the adjoining zone 61 of the *p*-conductivity type (see Figure 6).

In this method the *p-n* junction 46 is not exposed upon removing the oxide layer 45. In another variation of the method according to the invention, the above-described short-circuit is prevented in that after the formation of the inset pattern 41 by oxidation, the zone 61 of the *p*-type adjoining the pattern 41 is obtained by diffusion of aluminium or gallium as a *p*-type doping material.

For reasons of simplicity the shape details of the inset oxide pattern are shown in Figures 4 and 6 only, and the *n*-type buried layer 5 or 23 is not shown in Figures 3 to 6.

The structure shown in Figure 1 can be manufactured as follows in accordance with the present invention. Starting material is a *p*-type semiconductor body 1 in the form of a silicon wafer having a thickness of 200 μ and a resistivity of 2 ohm.cm and serving as a substrate on which an *n*-type arsenic-containing epitaxial layer 4 having a thickness of 2 μ and a resistivity of 0.5 ohm.cm. is deposited (see Figure 7). A low ohmic *n*-type region 5 having a maximum concentration of arsenic of 5.10^{19} atoms/cc is formed in a usual manner in the epitaxial layer and the remaining substrate part of the semiconductor body, for example, by the local deposition, prior to the epitaxy, on the semiconductor body of an arsenic source which during the subsequent epitaxial process diffuses both in the semiconductor body and in the epitaxial layer while forming the low-ohmic *n*-type region 5.

An oxidation-resistant masking layer 71, 72 consisting of a silicon nitride layer 71 of 0.2 μ thickness and a silicon oxide layer 72 of 0.05 μ thickness having apertures 74 are then provided on a major surface 73.

The masking layer 71, 72 is first used for etching the silicon body in which approximately 1 μ deep recesses 76 are formed and is then used for the diffusion of boron in the epitaxial layer 4 to obtain the doping pattern 75. For that purpose a boron source is formed in a usual manner by heating for 5 minutes at 975°C in a boron oxide-containing vapour current. The masking layer 71, 72 is then used to mask during oxidation (see

Figure 8) of the doping pattern 75 to obtain the 2.2 μ deep inset pattern (6, 7, 8), which extends slightly deeper in the semiconductor body 1 than the thickness of the epitaxial layer 4, and the approximately 1.5 μ deep adjoining zone 11, 12, 13 of the p-type having a boron concentration of approximately 5.10^{17} atoms/ccm. The oxidation is carried out by passing steam of 1 atmosphere over the silicon body for 16 hours at 1000°C after which the masking layer 71, 72 is removed.

The semiconductor device shown in Figure 1 can now be obtained in a simple manner since diffusion of doping materials to obtain the regions 3 and 17 (for example simultaneously) and the region 2 may be carried out without it being necessary for masks to be aligned accurately relative to the inset pattern. By a usual diffusion process, the region 3 has, for example, an average concentration of boron of 10^{18} atoms/cc and is 1 μ deep. The region 2 has a concentration of phosphorus of 10^{20} atoms/cc and is 0.6 μ deep. In the part 14, the other region 4, 5 can be contacted by a deep diffusion of phosphorus with 10^{20} atoms/cc. It is also achieved that no separate mask need be used for diffusing the regions 3 and 17.

The regions of the circuit element and the semiconductor body can be contacted at the major surface of the semiconductor body *via* contact zones.

In a corresponding manner, a semiconductor device as shown in Figure 2 can be manufactured. This device also has the advantages of simple alignment steps together with the presence of channel stoppers between circuit elements in adjacent bounded parts 28 or between regions (e.g. 21 and 23) of a circuit element.

The structure shown in Figure 8 may also be manufactured by forming the inset pattern 6, 7, 8 after providing the masking layer 71, 72 (see Fig. 7) but before providing the doping pattern 75. Gallium or aluminium is then diffused, for example, while using the masking layer 71, 72.

In the case of diffusion of aluminium, the silicon body is provided in a tray of aluminium oxide, which can be closed with an aluminium oxide lid. An alloy of 10% by weight of aluminium with 90% by weight of silicon is contained in the tray. Upon heating at 1000°C for 60 minutes in a stream of hydrogen, aluminium is diffused in the silicon body over a depth of approximately 1 μ.

In the case in which gallium is diffused, silicon powder is used which contains 10^{18} atoms gallium per cc and heating is carried out in vacuum at 1100°C for 20 minutes. The diffusion depth of the gallium is also approximately 1 μ.

By diffusion of gallium or aluminium the zone 11, 12, 13 of the p-type adjoining the pattern is formed, the maximum concentration of the doping material in the zone is in both diffusion processes 5.10^{17} atoms/cc. Aluminium or gallium is preferably diffused after the masking layer 71, 72 has been removed. The advantage of this is that first the one region of the first conductivity type and the region of the second conductivity type can be obtained by diffusion. These latter two diffusion treatments might disturb an already obtained diffusion profile of the rather rapidly diffusing gallium.

Therefore, gallium or aluminium is preferably diffused after the region 2 or 21 of the first conductivity type has been formed in the semiconductor body.

In a further preferred embodiment, the adjoining zone and the region of the opposite conductivity type are formed simultaneously in the semiconductor body. This saves a diffusion step.

Diffusion of Al or Ga may of course also be used to obtain the structure shown in Figure 2.

It will be obvious that many modifications are possible within the scope of the invention. For example, instead of the p-type semiconductor body described in the embodiments, the starting material may be an n-type semiconductor body. The semiconductor bodies may be provided with p-type epitaxial layers instead of with n-type epitaxial layers. Instead of etching recesses prior to the oxidation described, the oxidation may also be carried out in two steps, in which the formed oxide is removed after the first step. The circuit element may be, for example, a p-n-p-n transistor. The inset pattern may also be inset only partly in the semiconductor body, which is the case, for example, when the oxidation is not interrupted by a step in which the already formed oxide is removed or when the body is not etched previously to oxidation.

Instead of a silicon nitride layer, the masking layer may comprise an aluminium oxide layer.

In all the cases, space-saving structures may be obtained for the manufacture of which special alignment steps can often be avoided.

WHAT WE CLAIM IS:—

1. A semiconductor device comprising a semiconductor body having at least one circuit element with at least three regions of which first and second regions have a first conductivity type and are separated by a third region which has a second conductivity type opposite to the first type, and a pattern of insulating material inset at least over a part of its thickness in the semiconductor body from a major surface of said body, the whole periphery of a portion of said body

Figure 8) of the doping pattern 75 to obtain the 2.2 μ deep inset pattern (6, 7, 8), which extends slightly deeper in the semiconductor body 1 than the thickness of the epitaxial layer 4, and the approximately 1.5 μ deep adjoining zone 11, 12, 13 of the *p*-type having a boron concentration of approximately 5.10^{17} atoms/ccm. The oxidation is carried out by passing steam of 1 atmosphere over the silicon body for 16 hours at 1000°C after which the masking layer 71, 72 is removed.

The semiconductor device shown in Figure 1 can now be obtained in a simple manner since diffusion of doping materials to obtain the regions 3 and 17 (for example simultaneously) and the region 2 may be carried out without it being necessary for masks to be aligned accurately relative to the inset pattern. By a usual diffusion process, the region 3 has, for example, an average concentration of boron of 10^{18} atoms/cc and is 1 μ deep. The region 2 has a concentration of phosphorus of 10^{20} atoms/cc and is 0.6 μ deep. In the part 14, the other region 4, 5 can be contacted by a deep diffusion of phosphorus with 10^{20} atoms/cc. It is also achieved that no separate mask need be used for diffusing the regions 3 and 17.

The regions of the circuit element and the semiconductor body can be contacted at the major surface of the semiconductor body *via* contact zones.

In a corresponding manner, a semiconductor device as shown in Figure 2 can be manufactured. This device also has the advantages of simple alignment steps together with the presence of channel stoppers between circuit elements in adjacent bounded parts 28 or between regions (e.g. 21 and 23) of a circuit element.

The structure shown in Figure 8 may also be manufactured by forming the inset pattern 6, 7, 8 after providing the masking layer 71, 72 (see Fig. 7) but before providing the doping pattern 75. Gallium or aluminium is then diffused, for example, while using the masking layer 71, 72.

In the case of diffusion of aluminium, the silicon body is provided in a tray of aluminium oxide, which can be closed with an aluminium oxide lid. An alloy of 10% by weight of aluminium with 90% by weight of silicon is contained in the tray. Upon heating at 1000°C for 60 minutes in a stream of hydrogen, aluminium is diffused in the silicon body over a depth of approximately 1 μ.

In the case in which gallium is diffused, silicon powder is used which contains 10^{18} atoms gallium per cc and heating is carried out in vacuum at 1100°C for 20 minutes. The diffusion depth of the gallium is also approximately 1 μ.

By diffusion of gallium or aluminium the zone 11, 12, 13 of the *p*-type adjoining the pattern is formed, the maximum concentration of the doping material in the zone is in both diffusion processes 5.10^{17} atoms/cc. Aluminium or gallium is preferably diffused after the masking layer 71, 72 has been removed. The advantage of this is that first the one region of the first conductivity type and the region of the second conductivity type can be obtained by diffusion. These latter two diffusion treatments might disturb an already obtained diffusion profile of the rather rapidly diffusing gallium.

Therefore, gallium or aluminium is preferably diffused after the region 2 or 21 of the first conductivity type has been formed in the semiconductor body.

In a further preferred embodiment, the adjoining zone and the region of the opposite conductivity type are formed simultaneously in the semiconductor body. This saves a diffusion step.

Diffusion of Al or Ga may of course also be used to obtain the structure shown in Figure 2.

It will be obvious that many modifications are possible within the scope of the invention. For example, instead of the *p*-type semiconductor body described in the embodiments, the starting material may be an *n*-type semiconductor body. The semiconductor bodies may be provided with *p*-type epitaxial layers instead of with *n*-type epitaxial layers. Instead of etching recesses prior to the oxidation described, the oxidation may also be carried out in two steps, in which the formed oxide is removed after the first step. The circuit element may be, for example, a *p-n-p-n* transistor. The inset pattern may also be inset only partly in the semiconductor body, which is the case, for example, when the oxidation is not interrupted by a step in which the already formed oxide is removed or when the body is not etched previously to oxidation.

Instead of a silicon nitride layer, the masking layer may comprise an aluminium oxide layer.

In all the cases, space-saving structures may be obtained for the manufacture of which special alignment steps can often be avoided.

WHAT WE CLAIM IS:—

1. A semiconductor device comprising a semiconductor body having at least one circuit element with at least three regions of which first and second regions have a first conductivity type and are separated by a third region which has a second conductivity type opposite to the first type, and a pattern of insulating material inset at least over a part of its thickness in the semiconductor body from a major surface of said body, the whole periphery of a portion of said body

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being bounded by part of the inset pattern, which bounded portion of the body adjoins said major surface and has located therein the whole of said first and third regions and at least a part of said second region, the inset pattern being adjoined by said third region along at least a part of its periphery and by said part of said second region along the whole of its periphery in said bounded portion of the body, said third region being separated from the major surface at least partly by said first region, and the inset pattern, at least at the area where it adjoins the bounded portion in the semiconductor body, being entirely embedded in an adjoining zone having a concentration of doping material characteristic of the second conductivity type, said concentration being smaller than the maximum concentration of the doping material determining the first conductivity type in said second region of the first conductivity type, said concentration being sufficiently large to prevent in regions of the second conductivity type at the area of the zone electrical connection between regions of the first conductivity type.

2. A semiconductor device as claimed in Claim 1, in which the semiconductor device is an integrated circuit, the semiconductor body comprises a substrate and an epitaxial layer, said second region of the first conductivity type comprises a buried layer, and the concentration of the doping material in said adjoining zone is smaller than the concentration of the doping material determining the first conductivity type in the buried layer.

3. A semiconductor device as claimed in Claim 1 or Claim 2, in which the concentration of the doping material characteristic of the second conductivity type in said adjoining zone is smaller than the maximum concentration of the doping material determining the first conductivity type in said first region of the first conductivity type, and said first region at least over a part of its periphery adjoins the inset pattern.

4. A semiconductor device as claimed in any of the preceding Claims, in which said first region over only part of its periphery adjoins the inset pattern, and the third region adjoins the major surface at plural places separated from each other by said first region.

5. A semiconductor device as claimed in any of the preceding Claims, in which the semiconductor body has another bounded portion which adjoins the major surface and is bounded at least along a part of its periphery and throughout its thickness by a part of the inset pattern in the semiconductor body which inset pattern part is entirely embedded in an adjoining zone having a concentration of doping material characteristic of the second conductivity type thereby forming in this other bounded portion a surface zone of the second conductivity type extending down to the substrate, and means contacting this surface zone.

6. A semiconductor device as claimed in Claim 5, in which the substrate is of second conductivity type, and the contact means at the surface effects a connection to the substrate via said adjoining zone in said other bounded portion of the body.

7. A method of manufacturing a semiconductor device comprising a semiconductor body having at least one circuit element with at least three regions of which first and second regions have a first conductivity type and are separated by a third region which has a second conductivity type opposite to the first type, and a pattern of insulating material inset at least over a part of its thickness in the semiconductor body from a major surface of said body, the whole periphery of a portion of said body being bounded by part of the inset pattern, which bounded portion of the body adjoins said major surface and has located therein the whole of said first and third regions and at least a part of said second region, the inset pattern being adjoined by said third region along at least a part of its periphery and by said part of said second region along the whole of its periphery in so far as it is located in said bounded portion of the body, said third region being separated from the major surface at least partly by said first region, said inset pattern being formed by oxidation of the semiconductor at apertures in an oxidation-resistant masking layer provided on the major surface of the body, in which method the semiconductor body is subjected to a treatment in which doping material characteristic of the second conductivity type in the semiconductor body is diffused to form a zone adjoining the pattern and having a concentration of said doping material which is smaller than the maximum concentration of the doping material determining the first conductivity type in the said second region of the first conductivity type and which is sufficiently large to prevent in regions of the second conductivity type at the area of the zone electrical connection between regions of the first conductivity type.

8. A method of manufacturing a semiconductor device as claimed in Claim 7, in which the masking layer is first used for obtaining a doping pattern characteristic of the second conductivity type in the semiconductor body, after which the masking layer is used for masking during oxidation of the doping pattern to obtain the inset pattern embedded in the adjoining zone having said doping material characteristic of the second conductivity type.

9. A method as claimed in Claim 8, in which prior to the diffusion step grooves are formed in the semiconductor body at the

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areas where the doping material characteristic of said second conductivity type is to be diffused.

10. A method of manufacturing a semiconductor device as claimed in Claim 7, in which first the inset pattern is formed by oxidation and the zone of the second conductivity type adjoining the pattern is subsequently obtained by diffusion of aluminium or gallium as said doping material characteristic of the second conductivity type.

11. A method as claimed in Claim 10, in which the aluminium or gallium is diffused after the oxidation masking layer has been removed.

12. A method as claimed in Claim 11, in which the aluminium or gallium is diffused after said first region of the first conductivity type has been formed in the semiconductor body.

13. A method as claimed in Claim 11 or Claim 12, in which said adjoining zone and said third region are formed simultaneously in the semiconductor body.

14. A semiconductor device, substantially as herein described with reference to Figure 1 of the accompanying drawings.

15. A semiconductor device, substantially as herein described with reference to Figure 2 of the accompanying drawings.

16. A method of manufacturing a semiconductor device, substantially as herein described with reference to Figures 1, 7 and 8 of the accompanying drawings.

17. A method of manufacturing a semiconductor device, substantially as herein described with reference to Figures 2, 5, and 6 of the accompanying drawings.

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