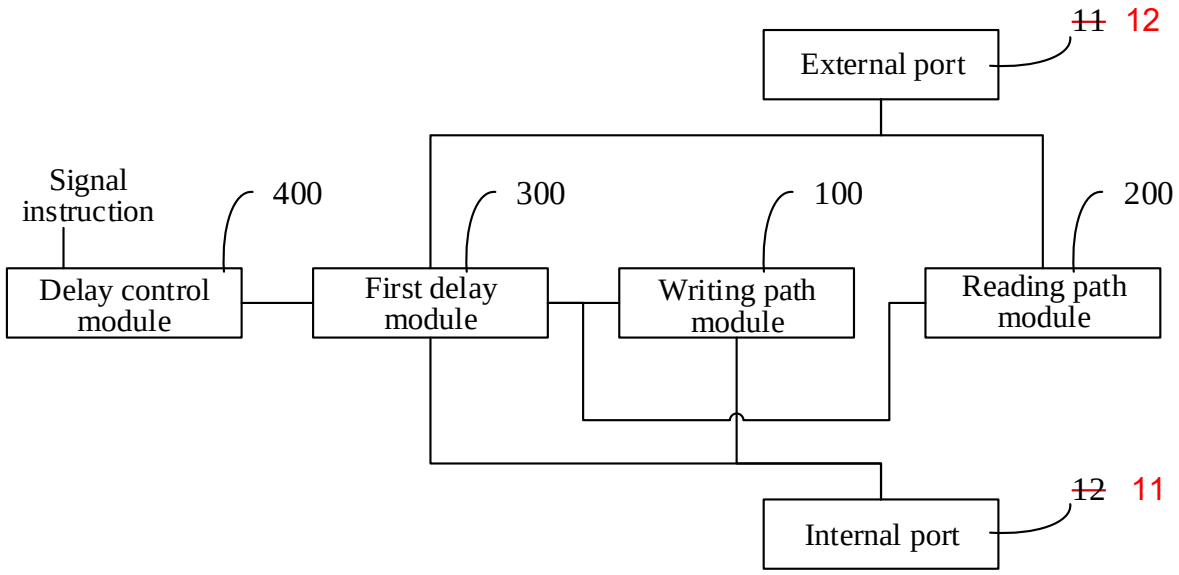

External port
11 12
Signal instruction
400
300
100
200
Delay control module
First delay module
Writing path module
Reading path module
12 11
Internal port

FIG. 1

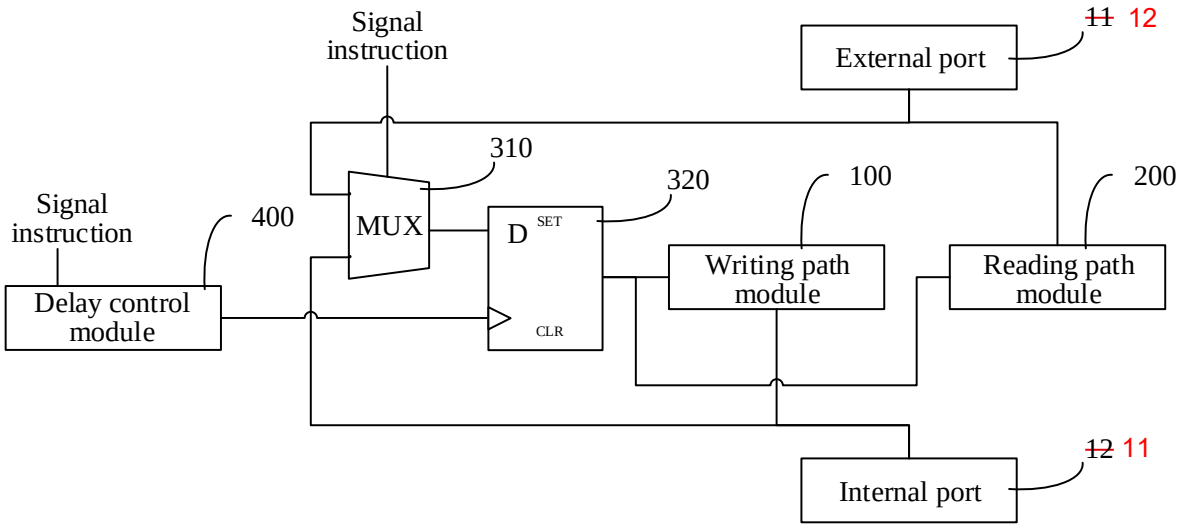

Signal instruction
External port
11 12
310
320
100
200
Signal instruction
400
MUX
D
SET
CLR
Writing path module
Reading path module
Delay control module
12 11
Internal port

FIG. 2

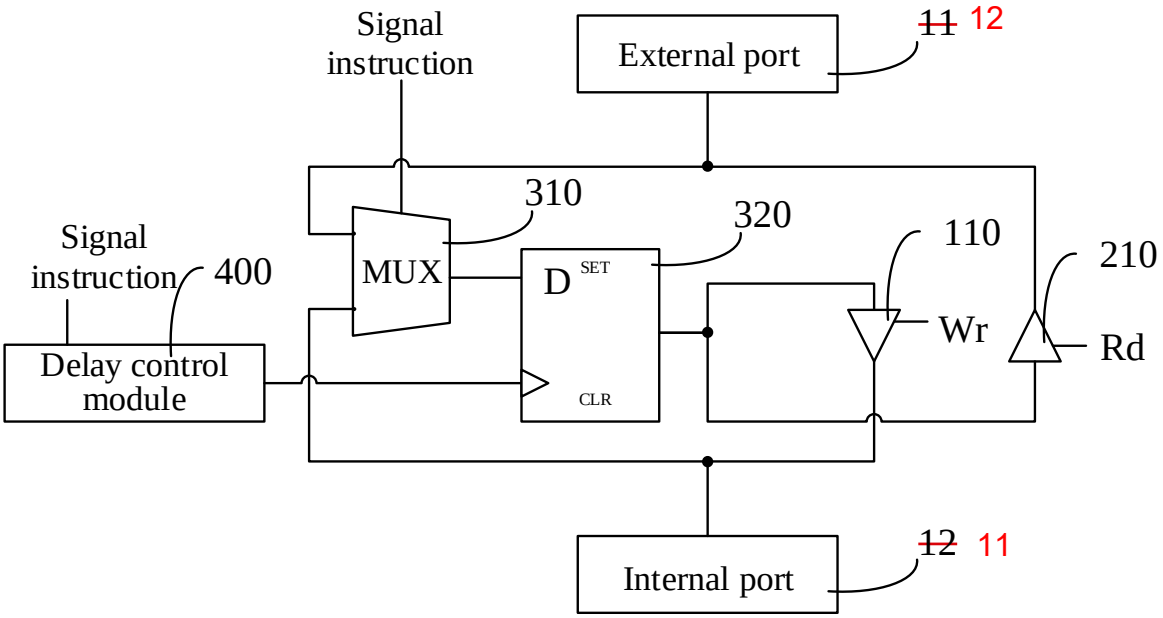

Signal instruction
External port
11 12
310
320
110
210
Signal instruction
400
MUX
D
SET
CLR
Wr
Rd
Delay control module
12 11
Internal port

FIG. 3

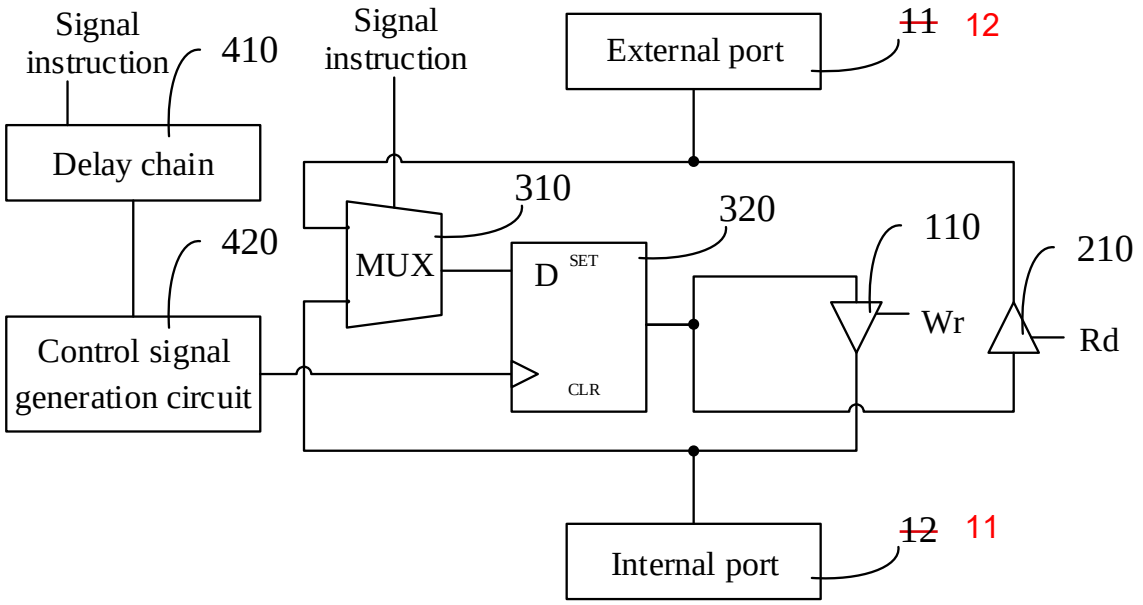

Signal instruction
410
Signal instruction
External port
11 12
Delay chain
310
320
110
210
420
MUX
D
SET
CLR
Wr
Rd
Control signal generation circuit
12 11
Internal port

FIG. 4

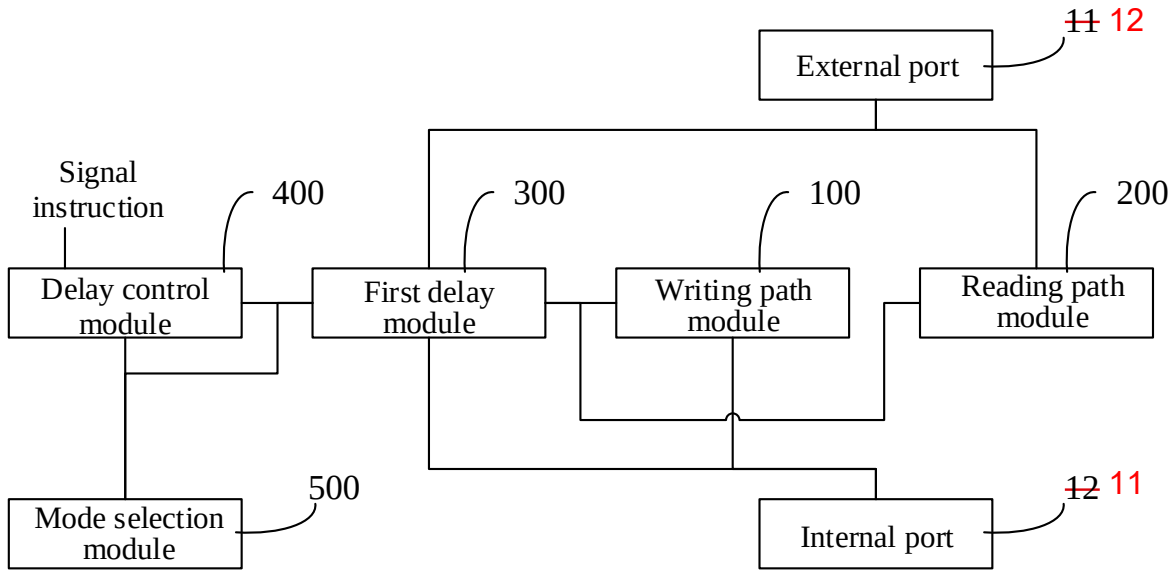

External port
~~11~~ 12
Signal instruction
400
300
100
200
Delay control module
First delay module
Writing path module
Reading path module
Mode selection module
500
Internal port
~~12~~ 11

FIG. 5

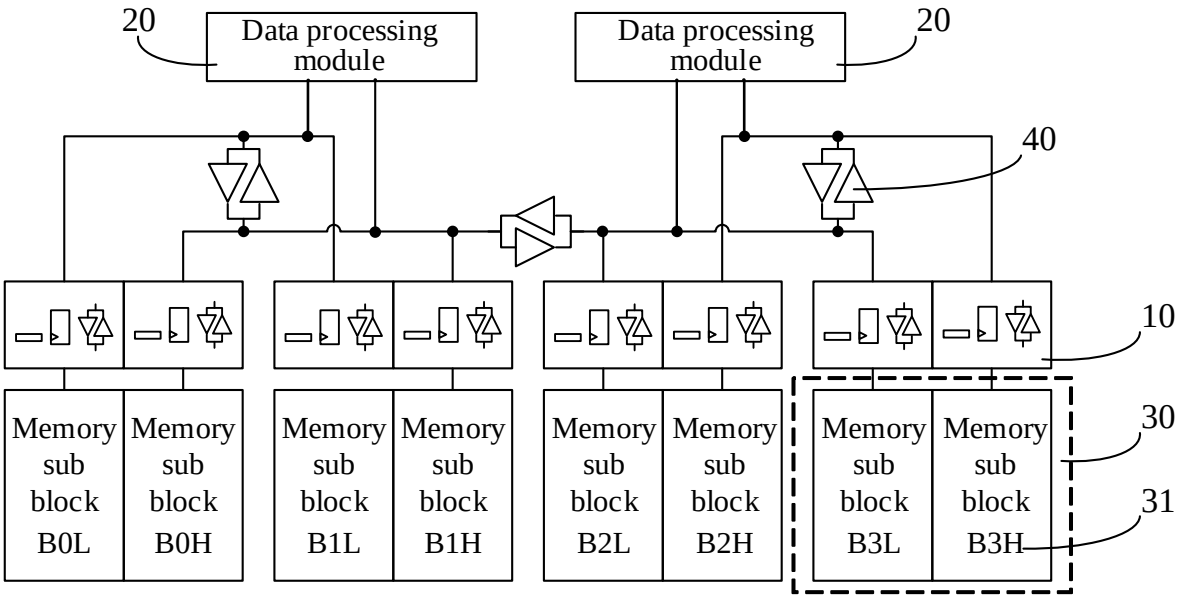

20
Data processing module
Data processing module
20
40
10
30
31
Memory sub block B0L
Memory sub block B0H
Memory sub block B1L
Memory sub block B1H
Memory sub block B2L
Memory sub block B2H
Memory sub block B3L
Memory sub block B3H

FIG. 6

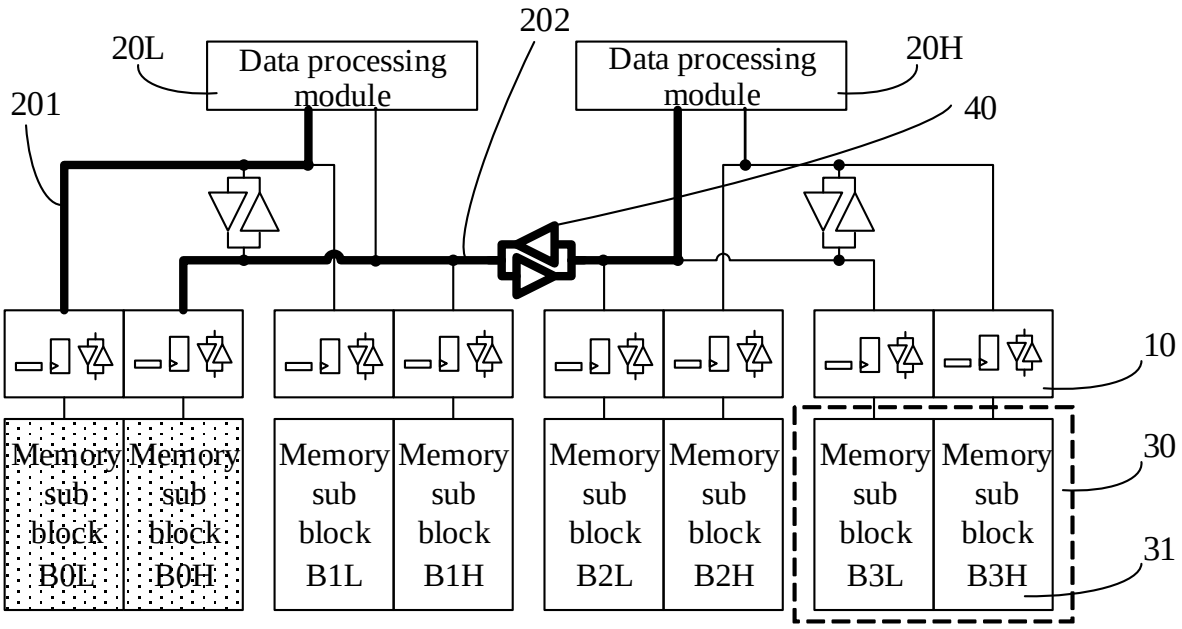

202
20L
Data processing module
Data processing module
20H
201
40
10
30
31
Memory sub block B0L
Memory sub block B0H
Memory sub block B1L
Memory sub block B1H
Memory sub block B2L
Memory sub block B2H
Memory sub block B3L
Memory sub block B3H

FIG. 7

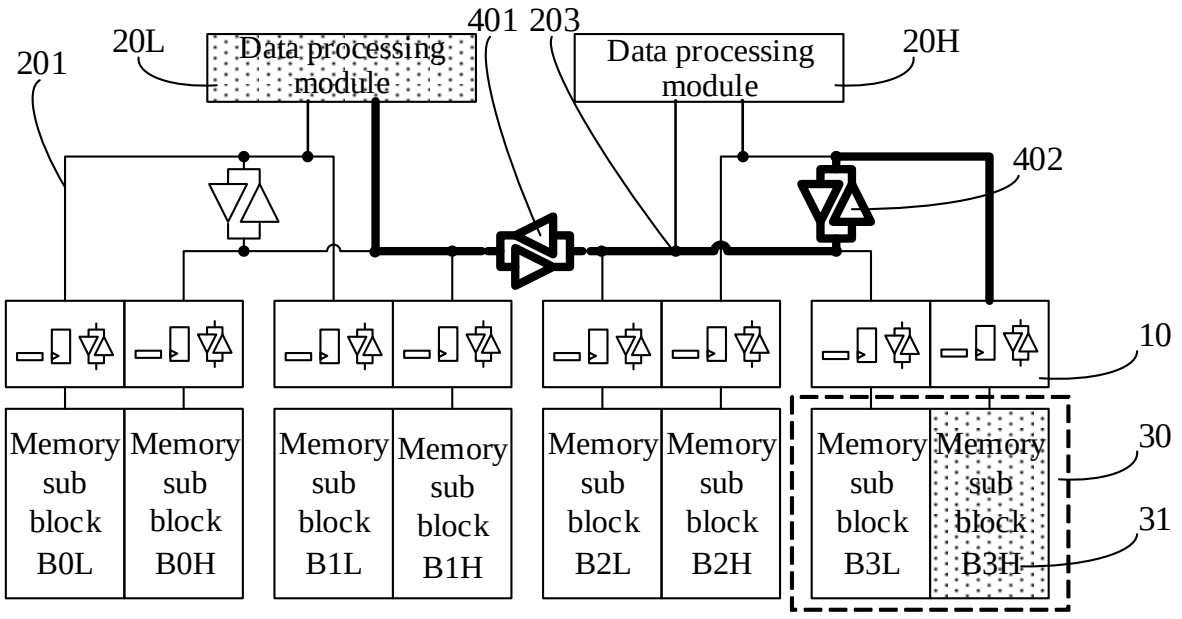

401
203
20L
Data processing module
Data processing module
20H
201
402
10
30
31
Memory sub block B0L
Memory sub block B0H
Memory sub block B1L
Memory sub block B1H
Memory sub block B2L
Memory sub block B2H
Memory sub block B3L
Memory sub block B3H

FIG. 8

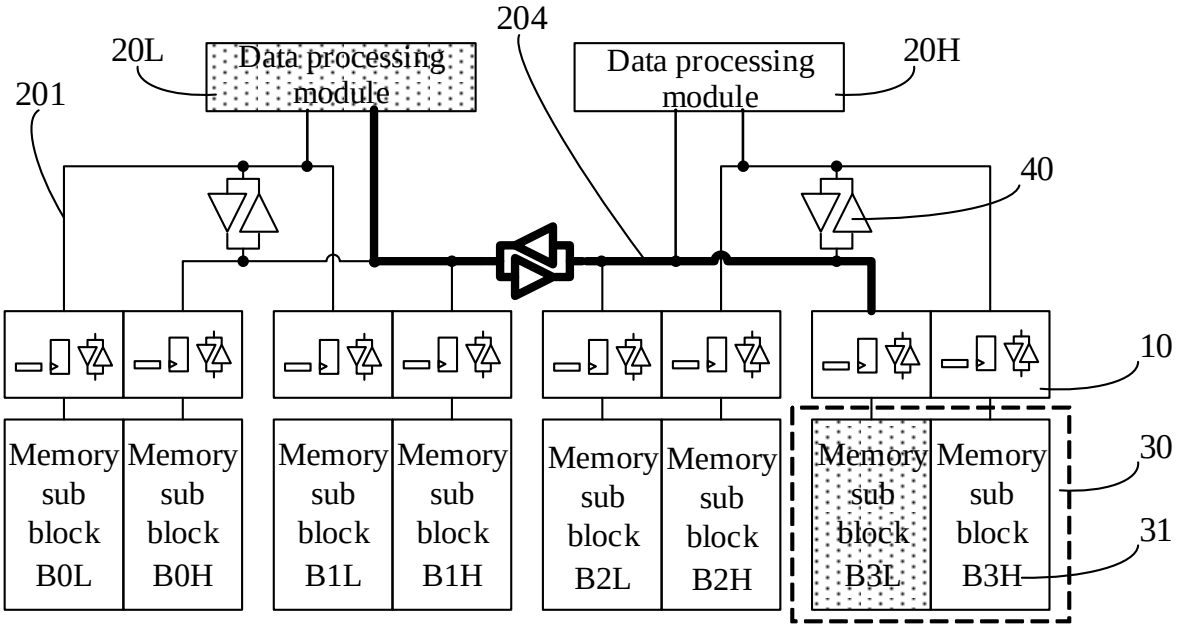

20L
Data processing module
204
Data processing module
20H
201
40
10
30
31
Memory sub block B0L
Memory sub block B0H
Memory sub block B1L
Memory sub block B1H
Memory sub block B2L
Memory sub block B2H
Memory sub block B3L
Memory sub block B3H

FIG. 9

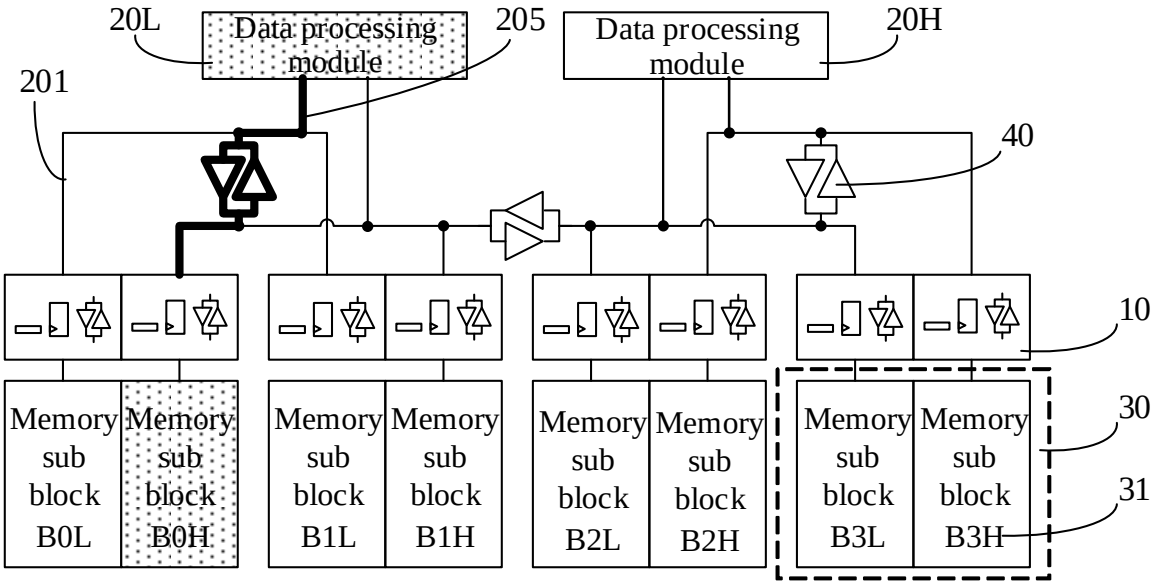

20L
Data processing module
205
Data processing module
20H
201
40
10
30
31
Memory sub block B0L
Memory sub block B0H
Memory sub block B1L
Memory sub block B1H
Memory sub block B2L
Memory sub block B2H
Memory sub block B3L
Memory sub block B3H

FIG. 10

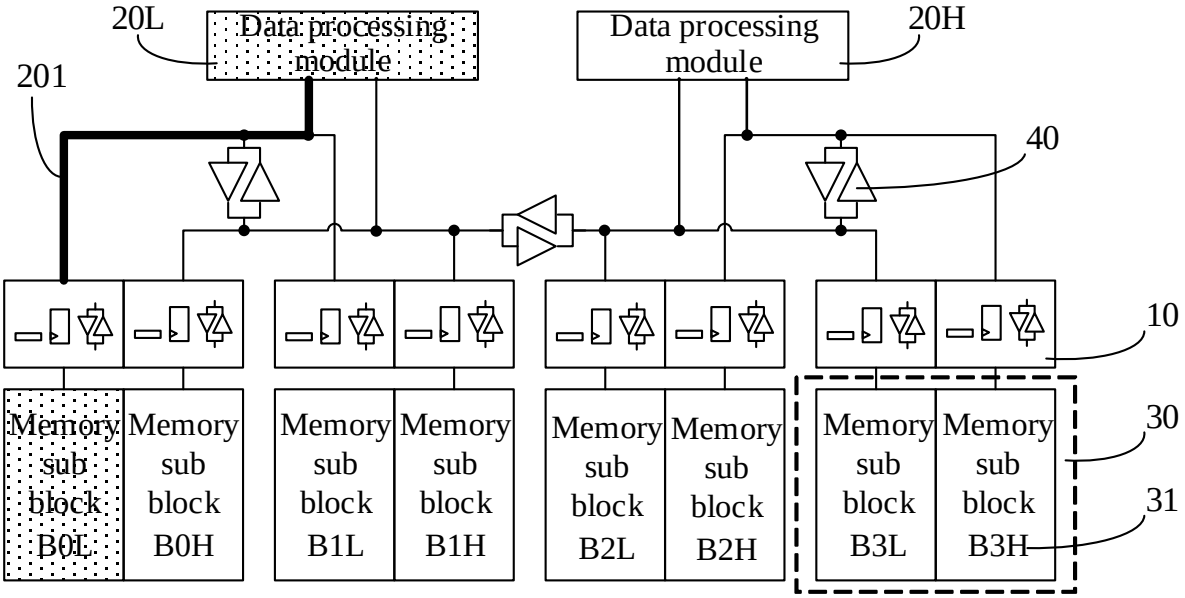

20L
Data processing module
Data processing module
20H
201
40
10
30
31
Memory sub block B0L
Memory sub block B0H
Memory sub block B1L
Memory sub block B1H
Memory sub block B2L
Memory sub block B2H
Memory sub block B3L
Memory sub block B3H

FIG. 11

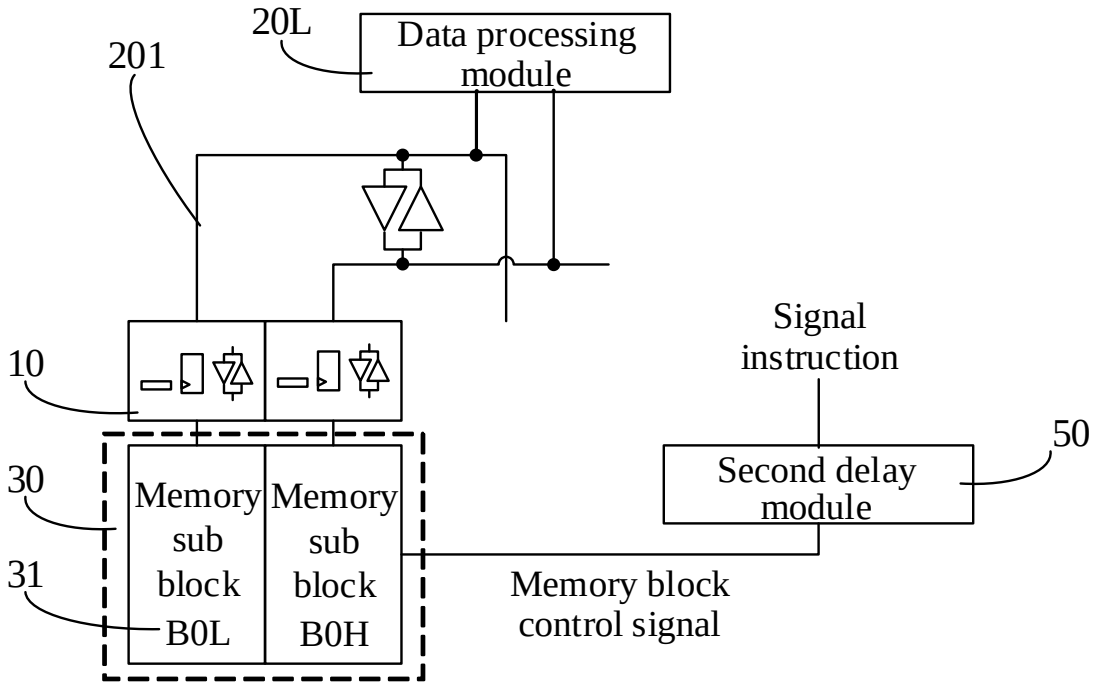

20L
Data processing module
201
10
Signal instruction
50
Second delay module
30
31
Memory sub block B0L
Memory sub block B0H
Memory block control signal

FIG. 12